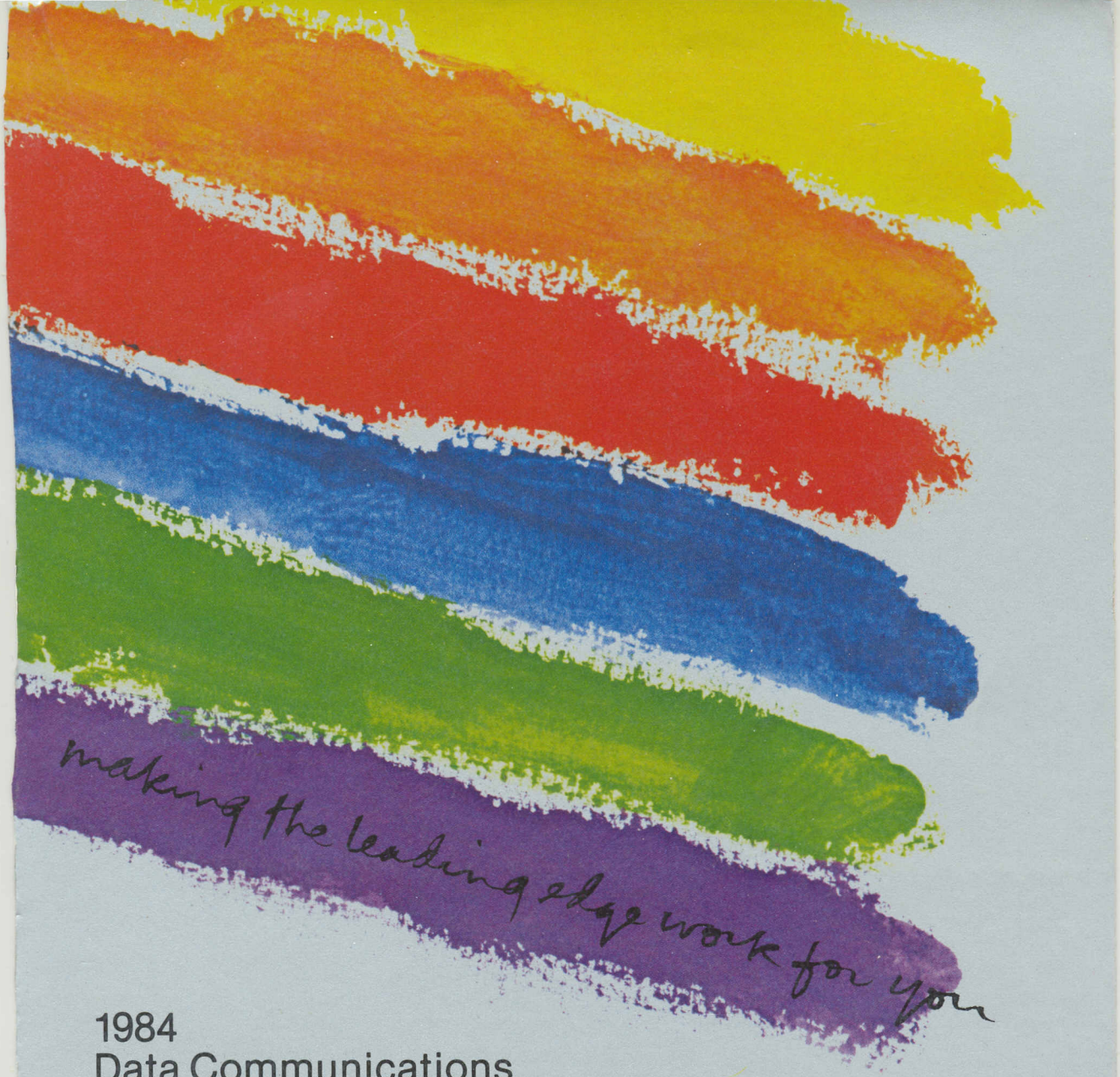


1984
Data Communications
Products Handbook

WESTERN DIGITAL
CORPORATION



WESTERN DIGITAL
CORPORATION
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Coritz

1984
Data Communications
Products Handbook

Making The Leading Edge Work For You.

This handbook is designed for you, the engineer. It's intended to be a useful tool, enabling you to make a preliminary evaluation of our products and later, with samples in hand, design our products into your own systems.

The data in these pages have been reviewed by our Marketing, Engineering, Manufacturing, and Quality groups. Now we would like you to review the information we've provided and tell us how we can improve it. Please feel free to suggest any changes, additions, or clarifications that occur to you. And don't hesitate to call to our attention any sins of omission or commission we may have made.

We're eager to help upgrade the quality of information our industry provides to its customers. So, please, help us. Direct your comments to:

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Advance Information: This product has not been produced in volume and is subject to functional and timing revisions. Prior to designing with the product, it is necessary to contact Western Digital Corporation for current information.

Preliminary: This product is in limited production and may be subject to change after device characterization has been completed. Prior to designing with the product, it is necessary to contact Western Digital Corporation for current information.

Data sheets without one of the above headings are in full production and intended for normal commercial applications. For military, extended temperature, burn-in, or hi-rel applications, contact Western Digital Corporation for information regarding further processing.

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WESTERN DIGITAL
CORPORATION

Quality/Reliability To Leading Edge Technology

QUALITY PROGRAM DESCRIPTION

The Quality Organization shown in Figure 2 assures compliance to design control, quality and reliability specifications, pursuant to corporate policy.

CORPORATE QUALITY POLICY

It is the policy of Western Digital Corporation that every employee be committed to quality excellence in producing products/processes which conform to acceptable requirements. The total quality program is managed and monitored by the quality assurance organization. Quality assurance is chartered to review marketing product requirements, qualify hardware and software designs, certify manufacturing operations and monitor performance/control conformance to product specifications.

Primary responsibility for execution for the quality program rests with functional organizations to design, produce and market high quality and high reliability products specified to our customers.

LSI QUALITY ASSURANCE PROGRAM HIGHLIGHTS

- LSI manufacturing assurance provisions are derived in part from MIL-M-38510 and MIL-STD-883B as applied to high grade commercial components.
- All process raw materials used in the Mask/Wafer fabrication and assembly operations are monitored by Material Assurance.
- Material Assurance maintains a thorough control of incoming material and has developed unique "use/stress tests" (look ahead sample build acceptance) which critical material must pass before acceptance.
- The Product Assurance Department continuously monitors the internal and external manufacturing flow (shown in Figure 1) and issues process control reports displaying detailed data and trends for the associated areas.
  - — Document control is an integral part of Product Assurance. All specifications are issued and controlled by this activity.
  - — The Western Digital Malaysian assembly operation uses specifications and quality control provisions controlled by Document Control. Indicators of Malaysia quality are reviewed weekly.
  - — Purchased FAB and assembly operations are individually qualified and are certified against standard specifications during vendor qualification and monitored against reliability criteria.
  - — Defect control within the process assures the highest levels of built-in reliability.
- Quality audits and gates are located throughout the manufacturing process in order to assure a stable process and thus, a quality product to our customers. Figure 1 illustrates the manufacturing/screening/inspection flow diagram and identifies the steps as they relate to the production of LSI devices.
- Testing assures quality margins through 100% testing by manufacturing and, in addition, all products must pass a specified AQL sample test performed by QA at maximum operating temperature as follows:

Outgoing Quality Levels

SUBGROUPS	INSPECTION LEVEL
Subgroup 1 — Final 100% Electrical Audit @ Max °C	0.5 AQL*
Subgroup 2 — Visual (Marking, Lead Integrity, Package, Verify customer shipper)	1.0 AQL
Subgroup 3 — Shipping Visual Audit	1.0 AQL

*The double sampling techniques used allow considerably better AQL's in most all cases.

- LSI devices are 100% tested on industry standard test systems like that shown below. Quality outgoing testing (auditing) is done on the Fairchild Sentry Series 20 where possible to allow better correlation with customers.



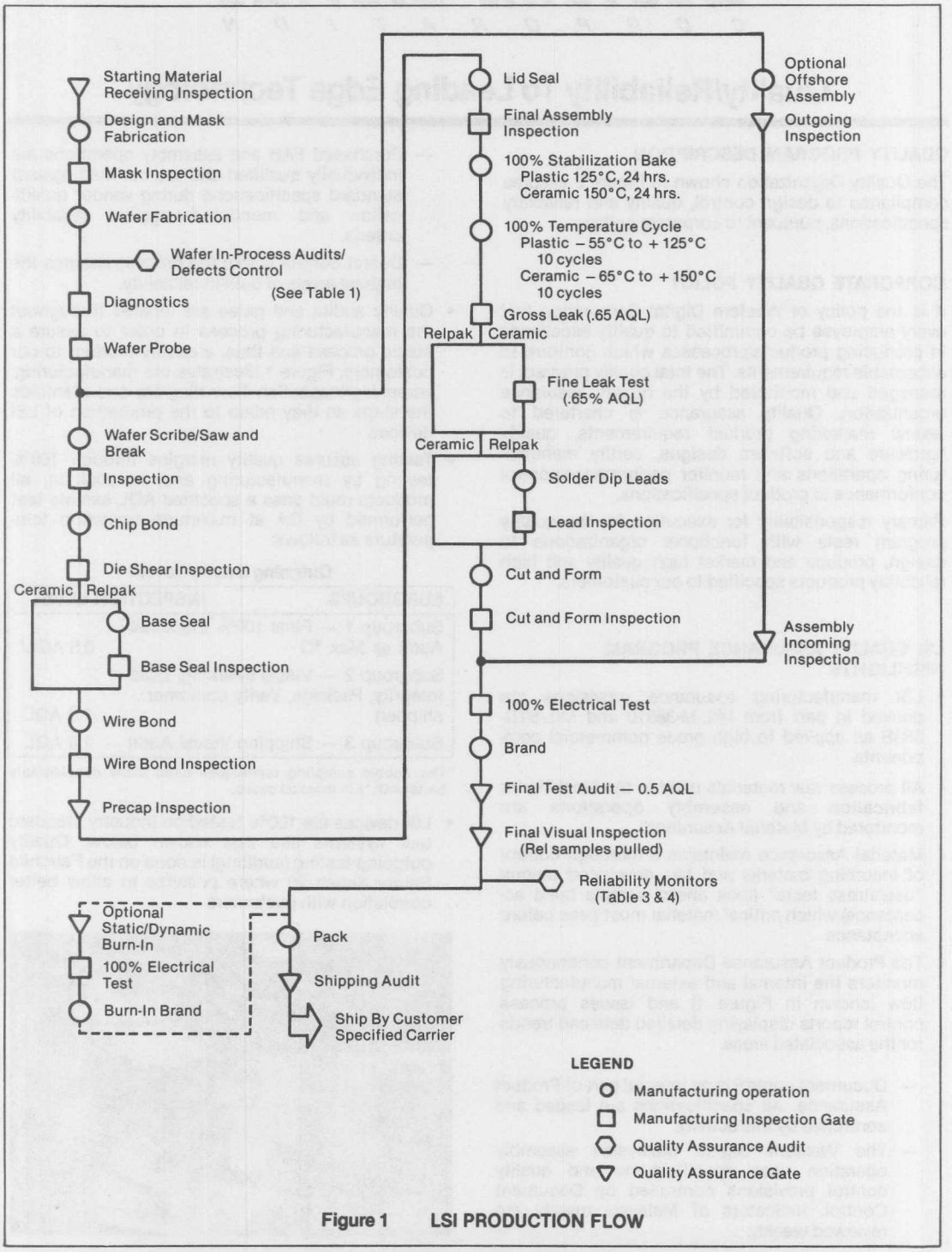
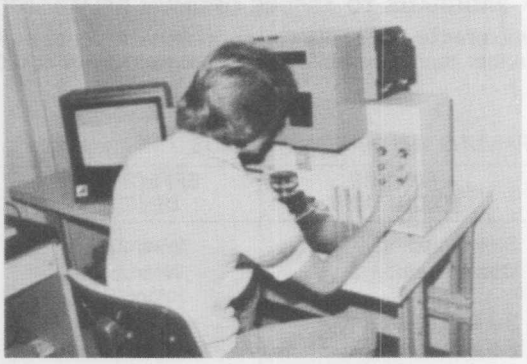
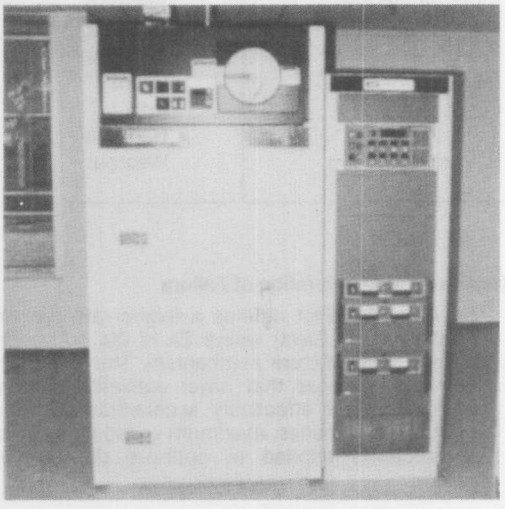


Figure 1 LSI PRODUCTION FLOW

Reliability Means Lasting Value





• DESIGNING FOR RELIABILITY

The production release procedure for an LSI device is designed to assure maximum reliability with a Quality checklist for:

- Test program qualifications
- Characterization report
- Field test (Beta Test) report
- Reliability Lifetest Qualifications
- Infrared Thermal Analysis
- Static Protection

All new devices and major process changes must pass reliability qualification before incorporation into production using the criteria defined in Tables 2-4. The infrared microscope shown on the right assures optimum burn-in temperatures and margins of safety. The dynamic burn-in system shown on the right is one of two custom designed systems which assure protective device isolation during burn-in.

• MAINTAINING RELIABILITY IN PRODUCTION

Process defects control are defined to continually measure built-in reliability, as measured by the following criteria:

TABLE 1

PROCESS RELIABILITY CONTROL	METHOD	CONDITION	SAMPLE*
Subgroup 1 — Defects Control			
a. Oxide Integrity	Non-destructive bubble test	Pinhole defect density	5 wafers
b. Polysilicon Integrity	SEM Analysis	Visual	5 wafers
Subgroup 2 — Electro-Migration Control			
Metal Step Coverage	MIL-STD-883 Method 2018	SEM Analysis	5 wafers
Subgroup 3 — Defect Density	Critical layers Field Gate Contact Metal	Visual of Photo defects (Defects/in^2)	8 wafers each layer
Subgroup 4 — Passivation/Insulation Integrity	MIL-STD-883 Method 2021	Visual of Pinhole defect density	Final Silox 5 wafers Intermediate 5 wafers

*Inspection intervals are defined by the in-line process control data reviewed on a lot-by-lot basis.

• PROGRAMS TO ASSURE OPTIMUM RELIABILITY

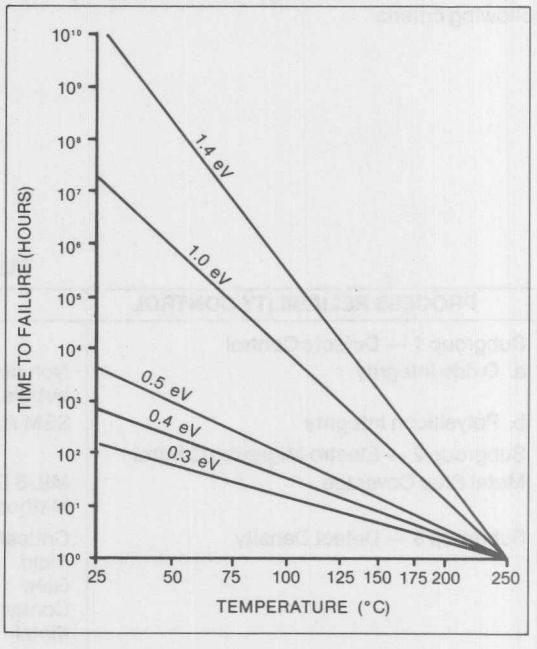
Improved levels of reliability are available under custom reliability programs using static and dynamic burn-in to further improve reliability. These programs focus on MOS failure mechanisms as follows:

FAILURE MECHANISMS IN MOS

FAILURE MECHANISM	EFFECT ON DEVICE	ESTIMATED ACTIVATION ENERGY	SCREENING METHOD
Slow Trapping	Wearout	1.0 eV	Static Burn-In
Contamination	Wearout/ Infant	1.4 eV	Static Burn-In
Surface Charge	Wearout	0.5-1.0 eV	Static Burn-In
Polarization	Wearout	1.0 eV	Static Burn-In
Electromigration	Wearout	1.0 eV	Dynamic Burn-In
Microcracks	Random	—	100% Temp. Cycling
Contacts	Wearout/ Infant	—	Dynamic Burn-In
Oxide Defects	Infant/ Random	0.3 eV	Dynamic Burn-In at max. voltage
Electron Injection	Wearout	—	Low Temp. Voltage Operating Life

Temperature Acceleration of Failure

The Arrhenius Plot defines a failure rate proportional to exp(– Ea/kt) where Ea is the activation energy for the failure mechanism. The figure on the right indicates that lower activation energy failures are **not** effectively accelerated by temperature alone; hense, maximum voltage operation is selectively applied to optimize the burn-in process.



Static Burn-In (125°C — 48 hours or 160 hours)

Provided on a sample basis for process monitor/control of 0.5 eV — 1.0 eV failure mechanisms. 100% static burn-in may be specified at an additional cost. However, static burn-in is considered only partially effective for internal LSI gates at logic "O" levels.

Dynamic Burn-In (Pattern test/125°C — 8 hours to 160 hours)

Accelerated functional dynamic operating life effectively controls internal MOS gate defects buried from external pin access. The input pattern is optionally pseudo-random or fixed pattern programmable to simulate 1000-3000 hours of field operation at maximum operating voltage(s).

High-Rel "K" Testing Program

General conformance to MIL-STD-883B method 5004.4, Class B with static Burn-In (Dynamic Burn-In may be specified as an option).

LSI RELIABILITY STANDARDS

TABLE 2 STANDARD RELIABILITY LEVELS

TEST	METHOD	CONDITION	FAILURE
Infant Mortality (see note)	Static Burn-In	125°C — 160 hrs.	<0.5%
Long Term Failure Rate	Dynamic Life Test	125°C — 1000 hrs.	<.05%/1000 hrs. @ 55°C 60% Confidence

*NOTE: Devices failing the infant mortality target remain on burn-in until acceptable failure rates are obtained.

TABLE 3 GROUP A DEVICE RELIABILITY MONITORS

TEST	METHOD	CONDITIONS	LTPD
Subgroup 1			
a. Internal Visual			15
b. Thermal Shock	1011	Test Failure Used (cond. B or C)	
c. Bond Strength	2011	Test Failures (cond. B)	
d. Die Shear Strength	2019	Test Failures	
Subgroup 2			
a. Seal — Gross Leak		Fluorocarbon detection 10^{-3} atm/cc/sec	15
b. Seal — Fine Leak	1014	Test Condition A	
Subgroup 3			
a. Rotating Steady State Life Test	1005	Static 160 hr. Burn-In 125°C plus 125°C Lifetest — 1000 hrs.	5
b. Electrical Parameters	—	Final electrical @ 25°C (with data @ 70°C)	

TABLE 4 GROUP B PACKAGE RELIABILITY MONITORS

TEST	METHOD	CONDITIONS	LTPD
Subgroup 1			
a. Thermal Shock	1011	Test Condition B or C	15
b. Temperature Cycling	1010	Test Condition B or C	
c. Seal — Gross Leak	—	Fluorocarbon detection 10^{-3} atm/cc/sec	
d. Seal — Fine Leak (ceramic)	1014	Test Condition A	
e. Electrical Parameters	—	Electrical at max -C	
f. 85/85 Moisture Resistance (plastic only)	—	85% RH/85°C for 1000 hours PDA = 10%	
g. Electrical Parameters	—	Final electrical @ 25°C	
Subgroup 2			
a. High Temp. Storage	1008	Test Condition B or C	
b. Mechanical Shock	2002	Test Condition B	15
c. Seal — Gross Leak	—	Fluorocarbon detection 10^{-3} atm/cc/sec	
d. Seal — Fine Leak (ceramic)	1014	Test Condition A	
e. Electrical Parameters	—	Final electrical @ 25°C/max. C	
Subgroup 3			
a. Lead Integrity	2004	Test Condition B2 (Lead Fatigue)	15
b. Seal — Gross Leak	—	Fluorocarbon detection 10^{-3} atm/cc/sec	
c. Seal — Fine Leak (ceramic)	1014	Test Condition A	

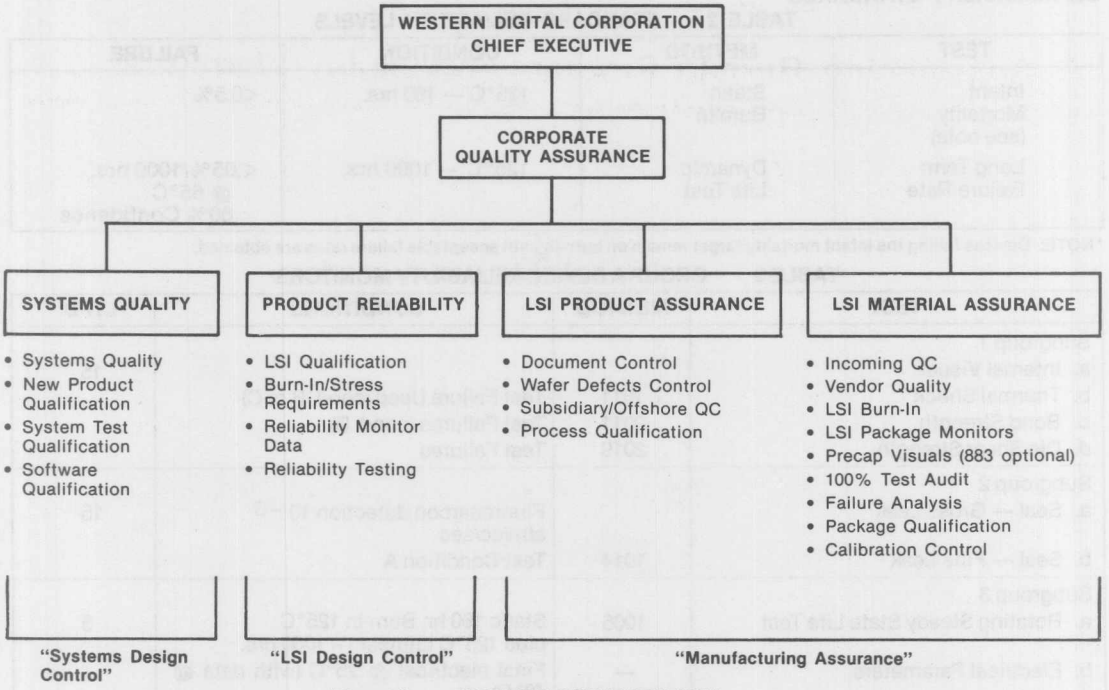


Figure 2 QUALITY ORGANIZATION

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Printed in U.S.A.

Announcing Burn-In Program Availability/Warranties

Western Digital now supports customer burn-in requirements for both static and dynamic burn-in under the strict control of the QA-Reliability organization.

This burn-in provides high performance 125°C static and dynamic burn-in for 8-160 hours to eliminate infant mortality and improve reliability. This process is executed using custom modified 32Bit AEHR test commercial burn-in equipment which provide monitored fixed pattern or pseudorandom burn-in with power supply and resistor device pin isolation.

LSI dynamic burn-in is verified in all cases by the design engineer for proper functioning. LSI Chip sets are also individually burned-in with dynamic equivalency to assure high performance bundled reliability.

The warranty on the program will optionally provide certificate of compliance to standard or custom designed burn-in programs and guarantee <.05%/Khrs failure rate.

CAUTION

Using outside burn-in methods not certified as acceptable by Western Digital may result in voided warranty, due to mishandling, junction temperature stress, or electrical damage. Further, since most burn-in houses do not support testing, catastrophic system condition can result in substantial damage before a problem is identified.

One consistent problem experienced with outside LSI burn-in houses can cause reliability problems; namely, parallelling totem pole MOS outputs, where the output states are not predictable, can cause a single (or a few) device(s) to sink all the current from the other devices on the burn-in tray — electromigration or current zaps are both possible.

Western Digital burn-in diagrams, dated after 1/1/82, must be used exactly as shown and will be provided upon request.

SEE YOUR LOCAL REPRESENTATIVE FOR COSTS AND ORDERING INFORMATION ON THIS NEW PROGRAM.

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Hi-Rel "K" Testing Program

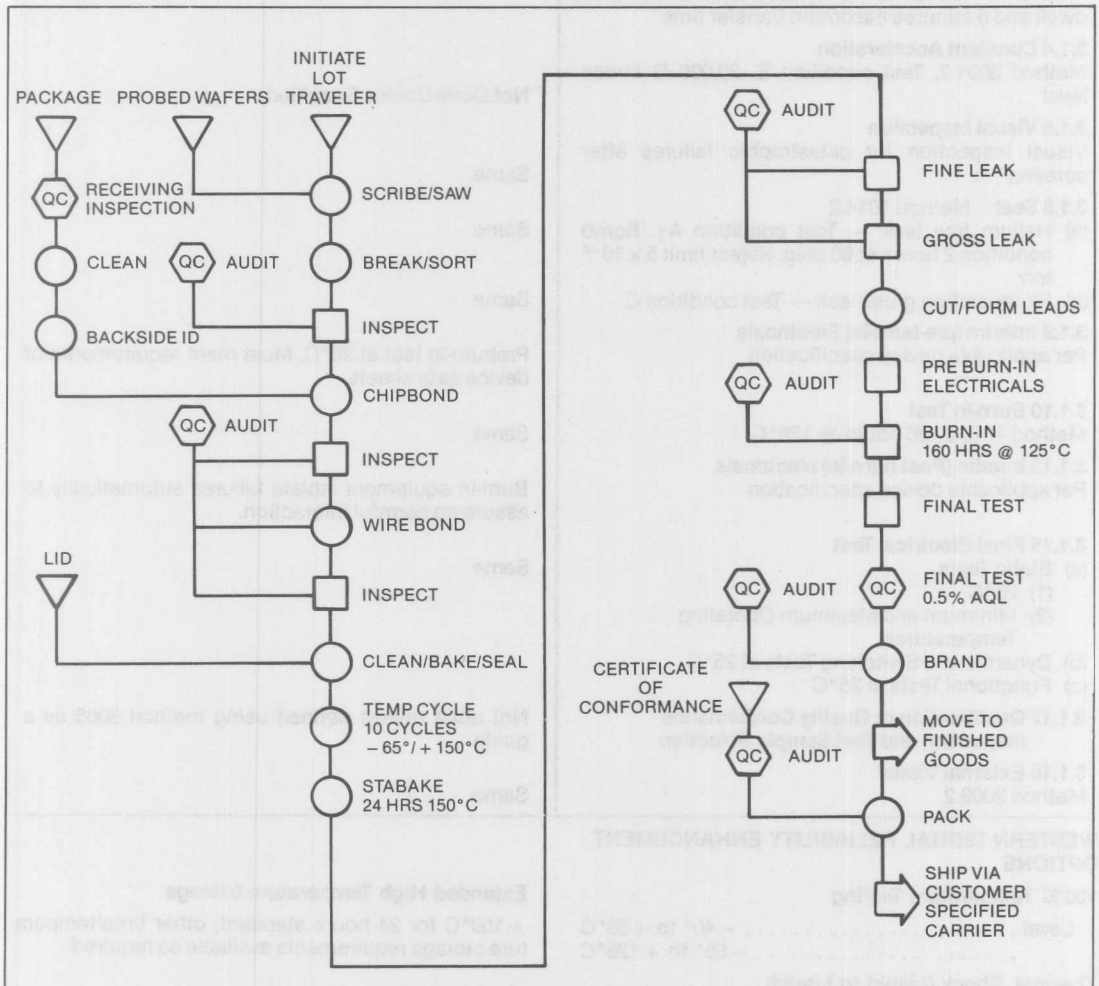
FEATURES

GENERAL CONFORMANCE TO MIL-STD-883B, METHOD 5004.4, CLASS B (SEE COMPARISON ON FOLLOWING PAGES)

- INCLUDES:
  - PRECAP VISUALS
  - SEAL INTEGRITY
  - POWER CONDITIONING
  - ENHANCEMENT OPTIONS

GENERAL DESCRIPTION

Western Digital's Hi-Rel "K" program is designed to provide high reliability devices for extended temperature environments. Individual enhancements may be specified to meet a customer's requirements.



HI-REL "K" PROGRAM FLOW DIAGRAM

COMPARISON OF MIL-STD-883 AND HI-REL "K" TEST PROGRAM

MIL-STD-883B, METHOD 5004.4, CLASS B	HI-REL "K" TEST
3.1.1 Internal Visual Method 2010.3 Test condition B	All Hi-Rel "K" devices receive 100% inspections prior to lid seal. These inspections together comprise criteria comparable to Mil-Std-883, method 2010.3, test condition B.
3.1.2 Stabilization Bake Method 1008.1 Test condition C 24 hours at 150°C	Same
3.1.3 Temperature Cycling Method 1010.2, Test condition C −65°C to 150°C for 10 cycles, with 10 minutes dwell and 5 minutes maximum transfer time	Same
3.1.4 Constant Acceleration Method 2001.2, Test condition E. 30,000 G stress level	Not Done Unless Specified
3.1.5 Visual Inspection Visual inspection for catastrophic failures after screens	Same
3.1.6 Seal Method 1014.2 (a) Helium fine leak — Test condition A_1. Bomb condition 2 hours at 60 psig. Reject limit 5×10^{-8} torr	Same
(b) Flourocarbon gross leak — Test condition C	Same
3.1.9 Interim (pre-burn-in) Electricals Per applicable device specification	Preburn-in test at 25°C. Must meet requirements of device data sheets.
3.1.10 Burn-in Test Method 1015.2 160 hours @ 125°C	Same
3.1.13 Interim (Post burn-in) electricals Per applicable device specification	Burn-in equipment isolate failures automatically to assure no harmful interaction.
3.1.15 Final Electrical Test (a) Static Tests (1) 25°C (2) Minimum and Maximum Operating Temperatures (b) Dynamic and Switching Tests at 25°C (c) Functional Tests at 25°C	Same
3.1.17 Qualification or Quality Conformance Inspection and Test Sample Selection	Not done unless defined using method 5005 as a guide.
3.1.18 External Visual Method 2009.2	Same

WESTERN DIGITAL RELIABILITY ENHANCEMENT OPTIONS

100% Temperature Testing

Level . . . . . −40° to +85°C
. . . . . −55° to +125°C

Thermal, Shock (Liquid to Liquid)

Level. . . . . 0° to +100°C, 15 cycles
. . . . . −55° to +125°C
. . . . . −65° to +150°C

Extended High Temperature Storage

+150°C for 24 hours standard, other time/temperature storage requirements available as required.

Dynamic Burn-In

Per note previously supplied.

Printed in U.S.A.

WD8275 Programmable CRT Controller

FEATURES

- PROGRAMMABLE SCREEN AND CHARACTER FORMAT
- 6 INDEPENDENT VISUAL FIELD ATTRIBUTES
- 11 VISUAL CHARACTER ATTRIBUTES (GRAPHIC CAPABILITY)
- CURSOR CONTROL (4 TYPES)
- LIGHT PEN DETECTION AND REGISTERS
- DUAL ROW BUFFERS
- PROGRAMMABLE DMA BURST MODE
- SINGLE +5V SUPPLY
- 40-PIN PACKAGE

GENERAL DESCRIPTION

The WD8275 Programmable CRT Controller is a single chip device to Interface CRT raster scan displays with microcomputer systems. Its primary function is to refresh the display by buffering the information from main memory and keeping track of the display position of the screen. The flexibility designed into the WD8275 will allow simple interface to almost any raster scan CRT display with a minimum of external hardware and software overhead.

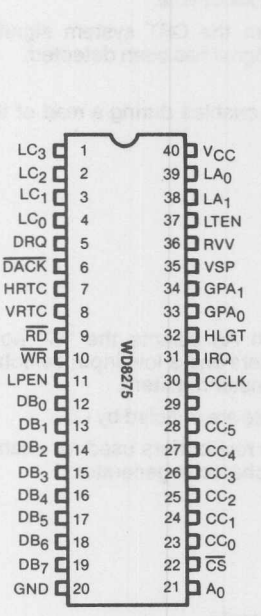


Figure 1. PIN CONFIGURATION

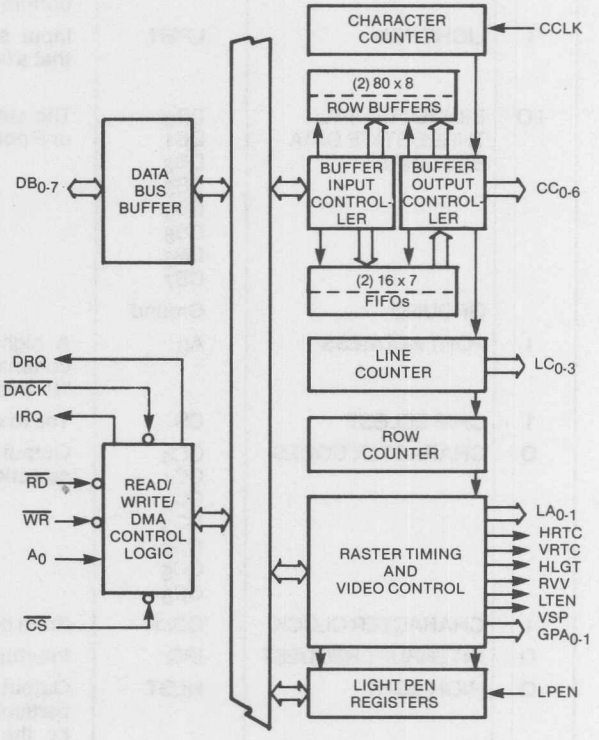


Figure 2. BLOCK DIAGRAM

TABLE 1. PIN DESCRIPTIONS

PIN NO.	TYPE	PIN NAME	SYMBOL	FUNCTION
1 2 3 4	O	LINE COUNT	LC_3 LC_2 LC_1 LC_0	Output from the line counter which is used to address the character generator for the line positions on the screen.
5	O	DMA REQUEST	DRQ	Output signal to the DMA controller requesting a DMA cycle.
6	I	DMA ACKNOWLEDGE	$\overline{DACK}$	Input signal from the DMA controller acknowledging that the requested DMA cycle has been granted.
7	O	HORIZONTAL RETRACE	HRTC	Output signal which is active during the programmed horizontal retrace interval. During this period the VSP output is high and the LTEN output is low.
8	O	VERTICAL RETRACE	VRTC	Output signal which is active during the programmed vertical retrace interval. During this period the VSP output is high and the LTEN output is low.
9	I	READ INPUT	$\overline{RD}$	A control signal to read registers.
10	I	WRITE INPUT	$\overline{WR}$	A control signal to write commands into the control registers or write data into the row buffers during a DMA cycle.
11	I	LIGHT PEN	LPEN	Input signal from the CRT system signifying that a light pen signal has been detected.
12 13 14 15 16 17 18 19	I/O	BIDIRECTIONAL THREE-STATE DATA BUS LINES	DB_0 DB_1 DB_2 DB_3 DB_4 DB_5 DB_6 DB_7	The outputs are enabled during a read of the C or P ports.
20		GROUND	Ground	
21	I	PORT ADDRESS	A_0	A high input on A_0 selects the "C" port or command registers and a low input selects the "P" port or parameter registers.
22	I	CHIP SELECT	CS	The read and write are enabled by CS.
23 24 25 26 27 28 29	O	CHARACTER CODES	CC_0 CC_1 CC_2 CC_3 CC_4 CC_5 CC_6	Output from the row buffers used for character selection in the character generator.
30	I	CHARACTER CLOCK	CCLK	From dot/timing logic.
31	O	INTERRUPT REQUEST	IRQ	Interrupt request.
32	O	HIGHLIGHT	HLGT	Output signal used to intensify the display at particular positions on the screen as specified by the character attribute codes or field attribute codes.

TABLE 1. PIN DESCRIPTIONS (Continued)

PIN NO.	TYPE	PIN NAME	SYMBOL	FUNCTION
33 34	O	GENERAL PURPOSE ATTRIBUTE CODES	GPA_1 GPA_0	Outputs which are enabled by the general purpose field attribute codes.
35	O	VIDEO SUPPRESSION	VSP	Output signal used to blank the video signal to the CRT. This output is active: —during the horizontal and vertical retrace intervals. —at the top and bottom lines of rows if underline is programmed to be number 8 or greater. —when an end of row or end of screen code is detected. —when a DMA underrun occurs. —at regular intervals (1/16 frame frequency for cursor, 1/32 frame frequency for character and field attributes) — to create blinking displays as specified by cursor, character attribute, or field attribute programming.
36	O	REVERSE VIDEO	RVV	Output signal used to indicate the CRT circuitry to reverse the video signal. This output is active at the cursor position if a reverse video block cursor is programmed or at the positions specified by the field attribute codes.
37	O	LIGHT ENABLE	LTEN	Output signal used to enable the video signal to the CRT. This output is active at the programmed underline cursor position, and at positions specified by attribute codes.
38 39	O	LINE ATTRIBUTE CODES	LA_0 LA_1	These attribute codes have to be decoded externally by the dot/timing logic to generate the horizontal and vertical line combinations for the graphic displays specified by the character attribute codes.
40		+5V POWER SUPPLY	V_{CC}	+5V power supply.

FUNCTIONAL DESCRIPTION

Data Bus Buffer

This 3-state, bidirectional, 8-bit buffer is used to interface the WD8275 to the system Data Bus.

This functional block accepts inputs from the System Control Bus and generates control signals for overall device operation. It contains the Command, Parameter, and Status Registers that store the various control formats for the device functional definition.

A_0	OPERATION	REGISTER
0	Read	PREG
0	Write	PREG
1	Read	SREG
1	Write	CREG

$\overline{RD}$ (READ)

A "low" on this input informs the WD8275 that the CPU is reading data or status information from the WD8275.

$\overline{WR}$ (WRITE)

A "low" on this input informs the WD8275 that the CPU is writing data or control words to the WD8275.

$\overline{CS}$ (CHIP SELECT)

A "low" on this input selects the WD8275. No reading or writing will occur unless the device is selected. When CS is high, the Data Bus in the float state and RD and WR will have no effect on the chip.

$\overline{DRQ}$ (DMA REQUEST)

A "high" on this output informs the DMA Controller that the WD8275 desires a DMA transfer.

$\overline{DACK}$ (DMA ACKNOWLEDGE)

A "low" on this input informs the WD8275 that a DMA cycle is in progress.

IRQ (INTERRUPT REQUEST)

A "high" on this output informs the CPU that the WD8275 desires interrupt service.

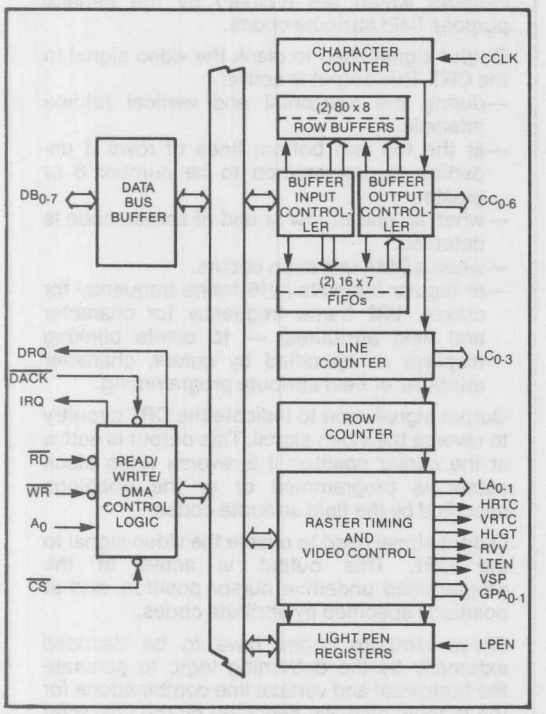


Figure 3.
WD8275 BLOCK DIAGRAM SHOWING DATA BUS BUFFER AND READ/WRITE FUNCTIONS

A_0	$\overline{RD}$	$\overline{WR}$	$\overline{CS}$	
0	0	1	0	Write WD8275 Parameter
0	1	0	0	Read WD8275 Parameter
1	0	1	0	Write WD8275 Command
1	1	0	0	Read WD8275 Status
X	1	1	0	Three-State
X	X	X	1	Three-State

Character Counter

The Character Counter is a programmable counter that is used to determine the number of characters to be displayed per row and the length of the horizontal retrace interval. It is driven by the CCLK (Character Clock) input, which should be a derivative of the external dot clock.

Line Counter

The Line Counter is a programmable counter that is used to determine the number of horizontal lines (Sweeps) per character row. Its outputs are used to address the external character generator ROM.

Row Counter

The Row Counter is a programmable counter that is used to determine the number of character rows to be displayed per frame and length of the vertical retrace interval.

Light Pen Registers

The Light Pen Registers are two registers that store the contents of the character counter and the row counter whenever there is a rising edge on the LPEN (Light Pen) input.

NOTE:
Software correction is required.

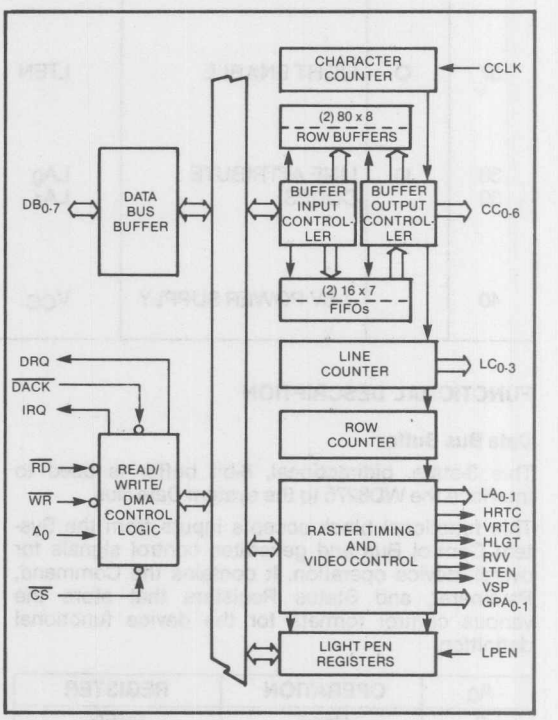


Figure 4.
WD8275 BLOCK DIAGRAM SHOWING COUNTER AND REGISTER FUNCTIONS

Raster Timing and Video Controls

The Raster Timing circuitry controls the timing of the HRTC (Horizontal Retrace) and VRTC (Vertical Retrace) outputs. The Video Control circuitry controls the generation of LA_{0-1} (Line Attribute), HGLT (Highlight), RVV (Reverse Video), LTEN (Light Enable), VSP (Video Suppress), and GPA_{0-1} (General Purpose Attribute) outputs.

Row Buffers

The Row Buffers are two 80-character buffers. They are filled from the microcomputer system memory with the character codes to be displayed. While one row buffer is displaying a row of characters, the other is being filled with the next row of characters.

FIFOs

There are two 16 character FIFOs in the WD8275. They are used to provide extra row buffer length in the Transparent Attribute Mode (see Detailed Operation section).

Buffer Input/Output Controllers

The Buffer Input/output Controllers decode the characters being placed in the row buffers. If the character is a character attribute, field attribute or special code, these controllers control the appropriate action. (Examples: An "End of Screen-Stop DMA" special code will cause the Buffer Input Controller to stop further DMA requests. A "Highlight" field attribute will cause the Buffer Output Controller to activate the HGLT output.)

SYSTEM OPERATION

The WD8275 is programmable to a large number of different display formats. It provides raster timing, display row buffering, visual attribute decoding, cursor timing, and light pen detection.

It is designed to interface with a DMA Controller and standard character generator ROMs for dot matrix decoding. Dot level timing must be provided by external circuitry.

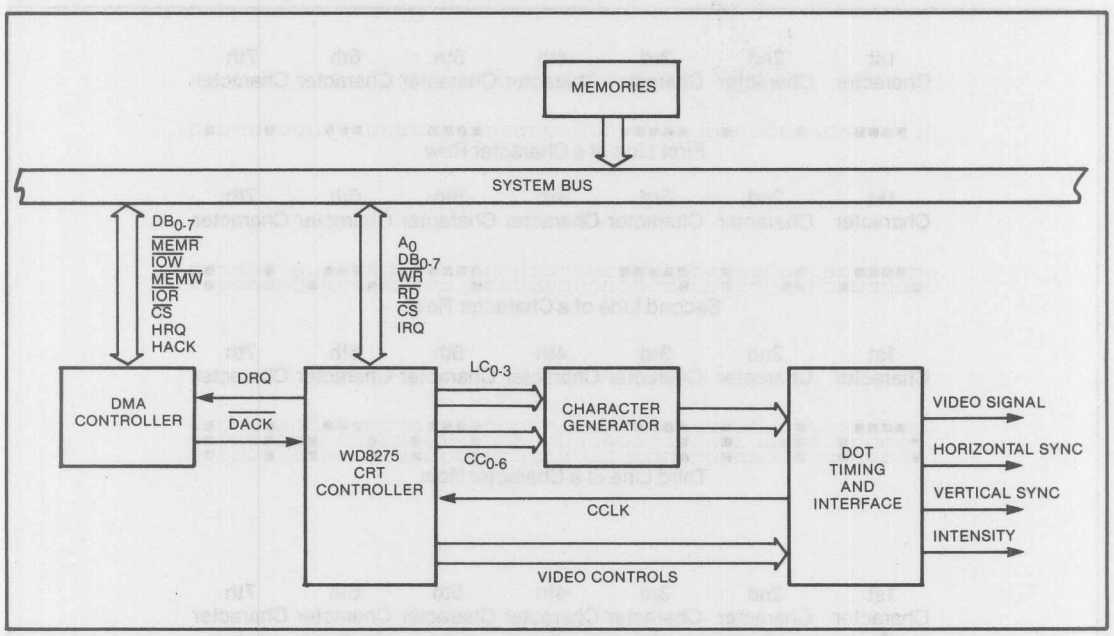


Figure 5. WD8275 SYSTEMS BLOCK DIAGRAM SHOWING SYSTEMS OPERATION

GENERAL SYSTEMS OPERATIONAL DESCRIPTION

The WD8275 provides a "window" into the microcomputer system memory.

Display characters are retrieved from memory and displayed on a row-by-row basis. The WD8275 has two row buffers. While one row buffer is being used for display, the other is being filled with the next row of characters to be displayed. The number of display characters per row and the number of character rows per frame are software programmable, providing easy interface to most CRT displays. (See Programming Section.)

The WD8275 requests DMA to fill the row buffer that is not being used for display. DMA burst length and spacing is programmable. (See Programming Section.)

The WD8275 displays character rows one line at a time.

The number of lines per character row, the underline position, and blanking of top and bottom lines are programmable. (See Programming Section.)

The WD8275 provides special Control Codes which can be used to minimize DMA or software overhead. It also provides Visual Attribute Codes to cause special action or symbols on the screen without the use of the character generator (see Visual Attributes Section).

The WD8275 also controls raster timing. This is done by generating Horizontal Retrace (HRTC) and Vertical Retrace (VRTC) signals. The timing of these signals is programmable.

The WD8275 can generate a cursor. Cursor location and format are programmable. (See Programming Section.)

The WD8275 has a light pen input and registers. The light pen input is used to load the registers. Light pen registers can be read on command. (See Programming Section.)

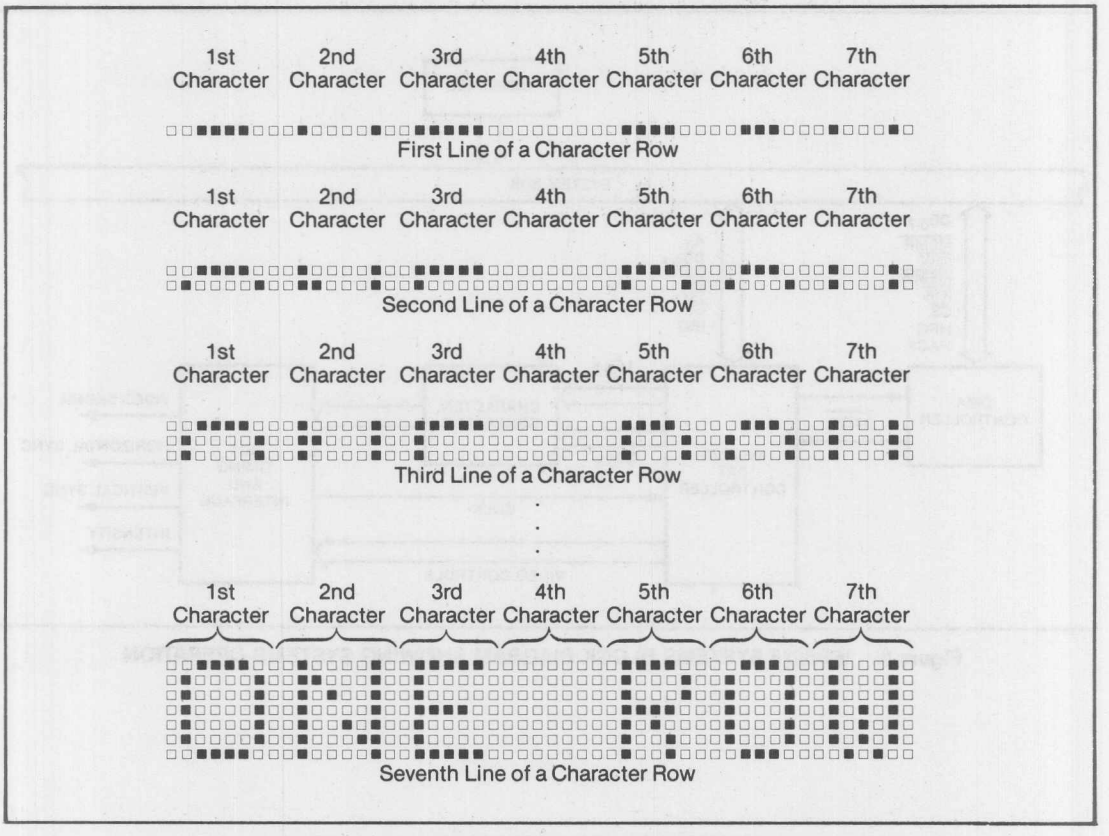


Figure 6. DISPLAY OF A CHARACTER ROW

DISPLAY ROW BUFFERING

Before the start of a frame, the WD8275 requests DMA and one row buffer is filled with characters.

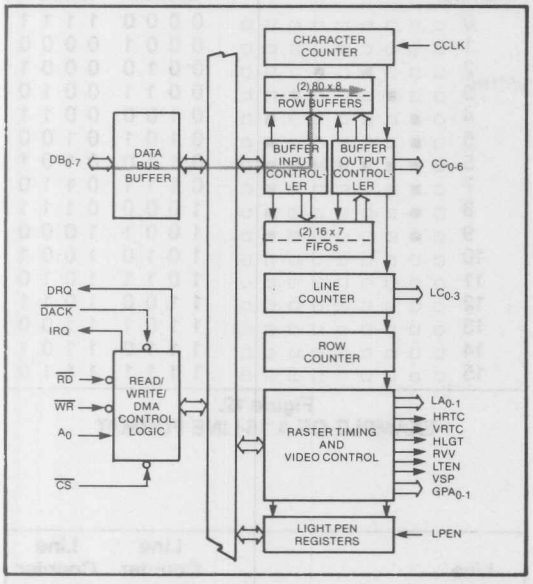


Figure 7.
FIRST ROW BUFFER FILLED

When the first horizontal sweep is started, character codes are output to the character generator from the row buffer just filled. Simultaneously, DMA begins filling the other row buffer with the next row of characters.

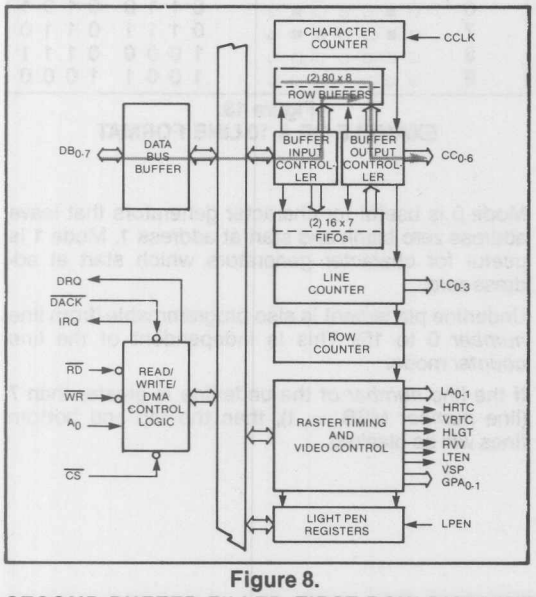


Figure 8.
SECOND BUFFER FILLED, FIRST ROW DISPLAYED

After all the lines of the character row are scanned, the roles of the two row buffers are reversed and the same procedure is followed for the next row.

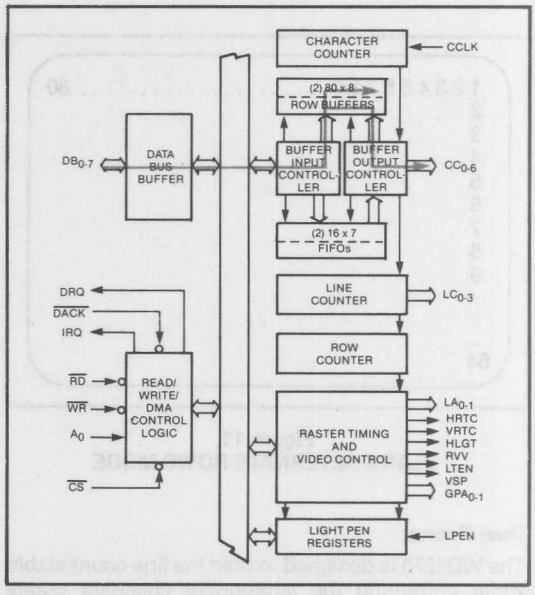


Figure 9.
FIRST BUFFER FILLED WITH THIRD ROW, SECOND ROW DISPLAYED

This is repeated until all of the character rows are displayed.

DISPLAY FORMAT

Screen Format

The WD8275 can be programmed to generate from 1 to 80 characters per row, and from 1 to 64 rows per frame.

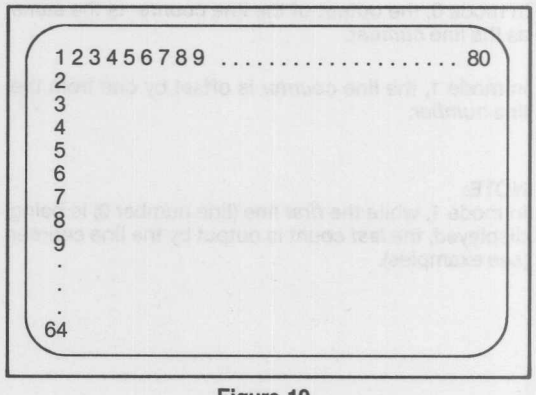


Figure 10.
SCREEN FORMAT

The WD8275 can also be programmed to blank alternate rows. In this mode, the first row is displayed, the second blanked, the third displayed, etc. DMA is not requested for the blanked rows.

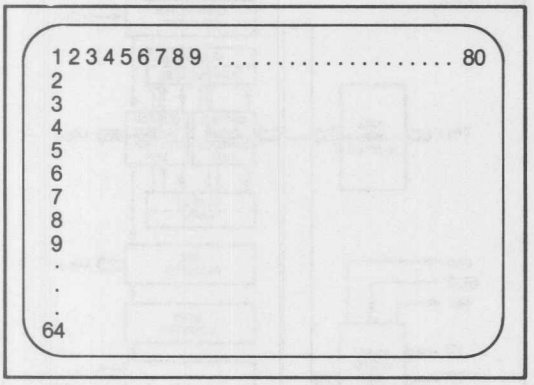


Figure 11.
BLANK ALTERNATE ROWS MODE

Row Format

The WD8275 is designed to hold the line count stable while outputting the appropriate character codes during each horizontal sweep. The line count is incremented during horizontal retrace and the whole row of character codes are output again during the next sweep. This is continued until the entire character row is displayed.

The number of lines (horizontal sweeps) per character row is programmable from 1 to 16.

The output of the line counter can be programmed to be in one of two modes.

In mode 0, the output of the line *counter* is the same as the line *number*.

In mode 1, the line *counter* is offset by one from the line *number*.

NOTE:
In mode 1, while the *first* line (line number 0) is being displayed, the *last* count is output by the line counter (see examples).

Line Number		Line Counter Mode 0	Line Counter Mode 1
0	□ □ □ □ □ □ □ □ □	0 0 0 0	1 1 1 1
1	□ □ □ □ ■ □ □ □ □	0 0 0 1	0 0 0 0
2	□ □ □ ■ □ ■ □ □ □	0 0 1 0	0 0 0 1
3	□ □ ■ □ □ □ ■ □ □	0 0 1 1	0 0 1 0
4	□ ■ □ □ □ □ □ ■ □	0 1 0 0	0 0 1 1
5	□ ■ □ □ □ □ □ ■ □	0 1 0 1	0 1 0 0
6	□ ■ ■ ■ ■ ■ ■ ■ □	0 1 1 0	0 1 0 1
7	□ ■ □ □ □ □ □ ■ □	0 1 1 1	0 1 1 0
8	□ ■ □ □ □ □ □ ■ □	1 0 0 0	0 1 1 1
9	□ ■ □ □ □ □ □ ■ □	1 0 0 1	1 0 0 0
10	□ □ □ □ □ □ □ □ □	1 0 1 0	1 0 0 1
11	□ □ □ □ □ □ □ □ □	1 0 1 1	1 0 1 0
12	□ □ □ □ □ □ □ □ □	1 1 0 0	1 0 1 1
13	□ □ □ □ □ □ □ □ □	1 1 0 1	1 1 0 0
14	□ □ □ □ □ □ □ □ □	1 1 1 0	1 1 0 1
15	□ □ □ □ □ □ □ □ □	1 1 1 1	1 1 1 0

Figure 12.
EXAMPLE OF A 16-LINE FORMAT

Line Number		Line Counter Mode 0	Line Counter Mode 1
0	□ □ □ □ □ □ □	0 0 0 0	1 0 0 1
1	□ □ □ ■ □ □ □	0 0 0 1	0 0 0 0
2	□ □ ■ □ ■ □ □	0 0 1 0	0 0 0 1
3	□ ■ □ □ □ ■ □	0 0 1 1	0 0 1 0
4	□ ■ □ □ □ ■ □	0 1 0 0	0 0 1 1
5	□ ■ ■ ■ ■ ■ □	0 1 0 1	0 1 0 0
6	□ ■ □ □ □ ■ □	0 1 1 0	0 1 0 1
7	□ ■ □ □ □ ■ □	0 1 1 1	0 1 1 0
8	□ □ □ □ □ □ □	1 0 0 0	0 1 1 1
9	□ □ □ □ □ □ □	1 0 0 1	1 0 0 0

Figure 13.
EXAMPLE OF A 10-LINE FORMAT

Mode 0 is useful for character generators that leave address zero blank and start at address 1. Mode 1 is useful for character generators which start at address zero.

Underline placement is also programmable (from line *number* 0 to 15). This is independent of the line *counter* mode.

If the line *number* of the underline is greater than 7 (line *number* MSB = 1), then the top and bottom lines will be blanked.

Line Number	Line Counter Mode 0	Line Counter Mode 1
0	0 0 0 0	1 0 1 1
1	0 0 0 1	0 0 0 0
2	0 0 1 0	0 0 0 1
3	0 0 1 1	0 0 1 0
4	0 1 0 0	0 0 1 1
5	0 1 0 1	0 1 0 0
6	0 1 1 0	0 1 0 1
7	0 1 1 1	0 1 1 0
8	1 0 0 0	0 1 1 1
9	1 0 0 1	1 0 0 0
10	1 0 1 0	1 0 0 1
11	1 0 1 1	1 0 1 0

Top and Bottom Lines are Blanked

Figure 14.
UNDERLINE IN LINE NUMBER 10

If the line *number* of the underline is less than or equal to 7 (line *number* MSB = 0), then the top and bottom lines will *not* be blanked.

Line Number	Line Counter Mode 0	Line Counter Mode 1
0	0 0 0 0	0 1 1 1
1	0 0 0 1	0 0 0 0
2	0 0 1 0	0 0 0 1
3	0 0 1 1	0 0 1 0
4	0 1 0 0	0 0 1 1
5	0 1 0 1	0 1 0 0
6	0 1 1 0	0 1 0 1
7	0 1 1 1	0 1 1 0

Top and Bottom Lines are not Blanked

Figure 15.
UNDERLINE IN LINE NUMBER 7

If the line *number* of the underline is greater than the maximum number of lines, the underline will not appear.

Blanking is accomplished by the VSP (Video Suppression) signal. Underline is accomplished by the LTEN (Light Enable) signal.

Dot Format

Dot width and character width are dependent upon the external timing and control circuitry.

Dot level timing circuitry should be designed to accept the parallel output of the character generator and shift it out serially at the rate required by the CRT display.

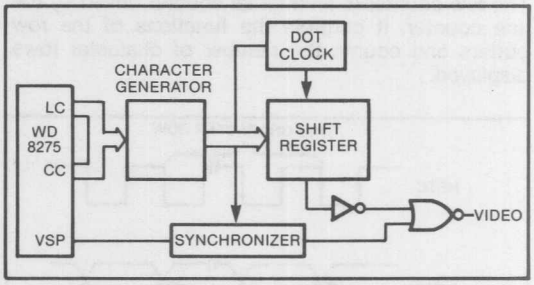


Figure 16.
TYPICAL DOT LEVEL BLOCK DIAGRAM

Dot width is a function of dot clock frequency.

Character width is a function of the character generator width.

Horizontal character spacing is a function of the shift register length.

NOTE:
Video control and timing signals must be synchronized with the video signal due to the character generator access delay.

RASTER TIMING

The character counter is driven by the character clock input (CCLK). It counts out the characters being displayed (programmable from 1 to 80). It then causes the line counter to increment, and it starts counting out the horizontal retrace interval (programmable from 2 to 32). This is constantly repeated.

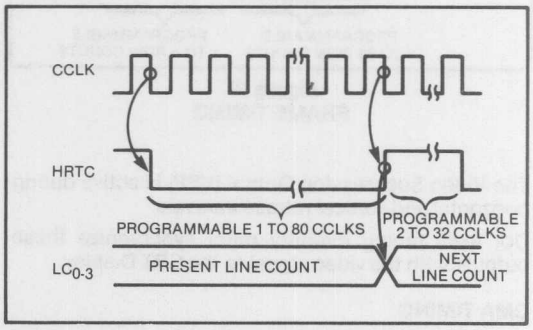


Figure 17.
LINE TIMING

The line counter is driven by the character counter. It is used to generate the line address outputs (LC_{0-3}) for the character generator. After it counts all of the lines in a character row (programmable from 1 to 16), it increments the row counter, and starts over again. (See Character Format Section for detailed description of Line Counter functions.)

The row counter is an internal counter driven by the line counter. It controls the functions of the row buffers and counts the number of character rows displayed.

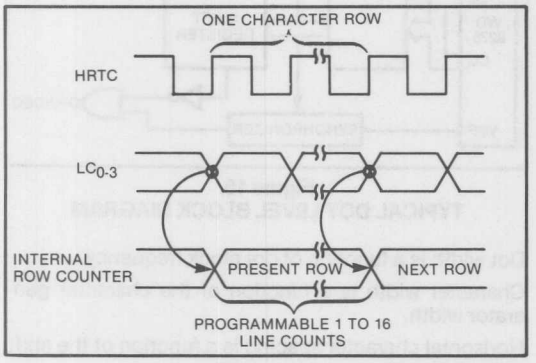


Figure 18. ROW TIMING

After the row counter counts all of the rows in a frame (programmable from 1 to 64), it starts counting out the vertical retrace interval (programmable from 1 to 4).

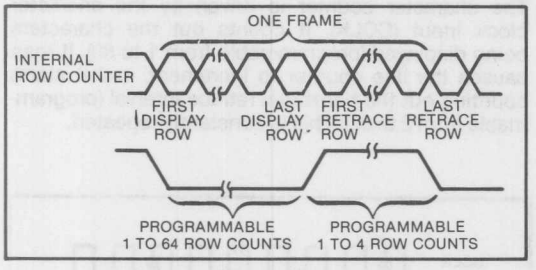


Figure 19. FRAME TIMING

The Video Suppression Output (VSP) is active during horizontal and vertical retrace intervals.

Dot level timing circuitry must synchronize these outputs with the video signal to the CRT Display.

DMA TIMING

The WD8275 can be programmed to request burst DMA transfers of 1 to 8 characters. The interval between bursts is also programmable (from 0 to 55 character clock periods ± 1). This allows the user to tailor his DMA overhead to fit his system needs.

The first DMA request of the frame occurs one *row time* before the end of vertical retrace. DMA requests continue as programmed, until the row buffer is filled. If the row buffer is filled in the middle of a burst, the WD8275 terminates the burst and resets the burst counter. No more DMA requests will occur until the *beginning* of the *next* row. At that time, DMA requests are activated as programmed until the other buffer is filled.

The first DMA request for a row will start at the first character clock of the preceding row. If the burst mode is used, the first DMA request may occur a number of character clocks later. This number is equal to the programmed burst space.

If, for any reason, there is a DMA underrun, a flag in the status word will be set.

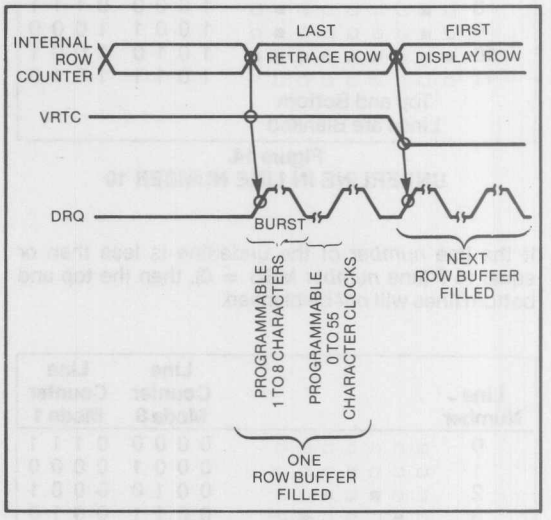


Figure 20. DMA TIMING

The DMA controller is typically initialized for the next frame at the end of the current frame.

INTERRUPT TIMING

The WD8275 can be programmed to generate an interrupt request at the end of each frame. This can be used to reinitialize the DMA controller. If the WD8275 interrupt enable flag is set, an interrupt request will occur at the *beginning* of the *last display row*.

IRQ will go inactive after the status register is read.

A reset command will also cause IRQ to go inactive, but this is not recommended during normal service.

Another method of reinitializing the DMA controller is to have the DMA controller itself interrupt on terminal count. With this method, the WD8275 interrupt enable flag should not be set.

NOTE:
Upon power-up, the WD8275 Interrupt Enable Flag may be set. As a result, the user's cold start routine should write a reset command to the WD8275 before system interrupts are enabled.

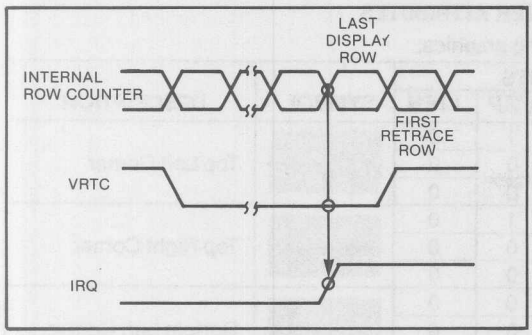


Figure 21.
BEGINNING OF INTERRUPT REQUEST

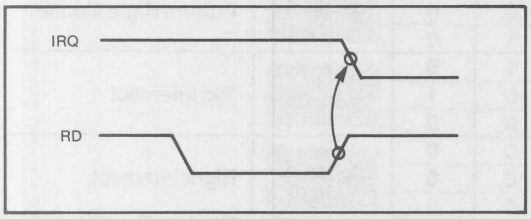


Figure 22.
END OF INTERRUPT REQUEST

VISUAL ATTRIBUTES AND SPECIAL CODES

The characters processed by the WD8275 are 8-bit quantities. The character code outputs provide the character generator with 7 bits of address. The Most Significant Bit is the extra bit and it is used to determine if it is a normal display character (MSB = 0), or if it is a Visual Attribute or Special Code (MSB = 1).

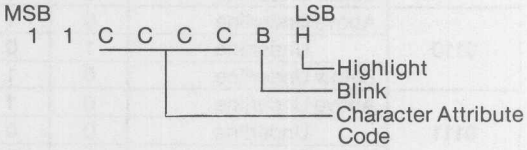
There are two types of Visual Attribute Codes. They are Character Attributes and Field Attributes.

Character Attribute Codes

Character attribute codes are codes that can be used to generate graphics symbols without the use of a character generator. This is accomplished by selectively activating the Line Attribute outputs (LA_{0-1}), the Video Suppression output (VSP), and the Light Enable output. The dot level timing circuitry can use these signals to generate the proper symbols.

Character attributes can be programmed to blink or be highlighted individually. Blinking is accomplished with the Video Suppression output (VSP). Blink frequency is equal to the screen refresh frequency divided by 32. Highlighting is accomplished by activating the Highlight output (HGLT).

Character Attributes



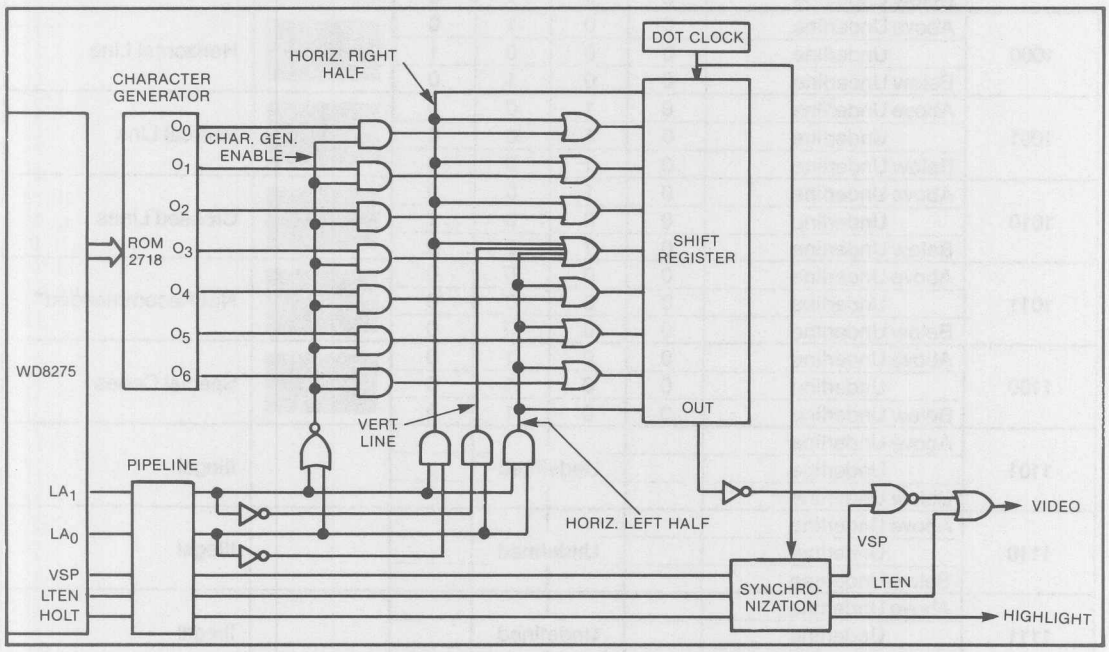
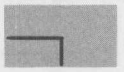
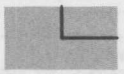
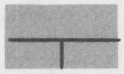
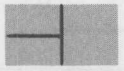
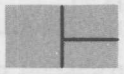
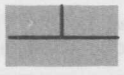
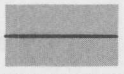
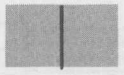
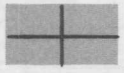
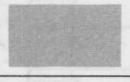
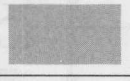


Figure 23. TYPICAL CHARACTER ATTRIBUTE LOGIC

TABLE 2. CHARACTER ATTRIBUTES

Character attributes were designed to produce the following graphics:

CHARACTER ATTRIBUTE CODE "CCCC"		OUTPUTS LA_1	LA_0	VSP	LTEN	SYMBOL	DESCRIPTION
0000	Above Underline	0	0	1	0		Top Left Corner
	Underline	1	0	0	0		
	Below Underline	0	1	0	0		
0001	Above Underline	0	0	1	0		Top Right Corner
	Underline	1	1	0	0		
	Below Underline	0	1	0	0		
0010	Above Underline	0	1	0	0		Bottom Left Corner
	Underline	1	0	0	0		
	Below Underline	0	0	1	0		
0011	Above Underline	0	1	0	0		Bottom Right Corner
	Underline	1	1	0	0		
	Below Underline	0	0	1	0		
0100	Above Underline	0	0	1	0		Top Intersect
	Underline	0	0	0	1		
	Below Underline	0	1	0	0		
0101	Above Underline	0	1	0	0		Right Intersect
	Underline	1	1	0	0		
	Below Underline	0	1	0	0		
0110	Above Underline	0	1	0	0		Left Intersect
	Underline	1	0	0	0		
	Below Underline	0	1	0	0		
0111	Above Underline	0	1	0	0		Bottom Intersect
	Underline	0	0	0	1		
	Below Underline	0	0	1	0		
1000	Above Underline	0	0	1	0		Horizontal Line
	Underline	0	0	0	1		
	Below Underline	0	0	1	0		
1001	Above Underline	0	1	0	0		Vertical Line
	Underline	0	1	0	0		
	Below Underline	0	1	0	0		
1010	Above Underline	0	1	0	0		Crossed Lines
	Underline	0	0	0	1		
	Below Underline	0	1	0	0		
1011	Above Underline	0	0	0	0		Not Recommended*
	Underline	0	0	0	0		
	Below Underline	0	0	0	0		
1100	Above Underline	0	0	1	0		Special Codes
	Underline	0	0	1	0		
	Below Underline	0	0	1	0		
1101	Above Underline		Undefined				Illegal
	Underline						
	Below Underline						
1110	Above Underline		Undefined				Illegal
	Underline						
	Below Underline						
1111	Above Underline		Undefined				Illegal
	Underline						
	Below Underline						

*Character Attribute Code 1011 is not recommended for normal operation. Since none of the attribute outputs are active, the character Generator will not be disabled, and an indeterminate character will be generated.

Character Attribute Codes 1101, 1110, and 1111 are illegal.

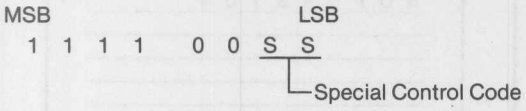
Blinking is active when B = 1.

Highlight is active when H = 1.

Special Codes

Four special codes are available to help reduce memory, software, or DMA overhead.

SPECIAL CONTROL CHARACTER



S	S	FUNCTION
0	0	End of Row
0	1	End of Row-Stop DMA
1	0	End of Screen
1	1	End of Screen-Stop DMA

The End of Row Code (00) activates VSP and holds it to the end of the line.

The End of Row-Stop DMA Code (01) causes the DMA Control Logic to stop DMA for the rest of the row when it is written into the Row Buffer. It affects the display in the same way as the End of Row Code (00).

The End of Screen Code (10) activates VSP and holds it to the end of the frame.

The End of Screen-Stop DMA Code (11) causes the DMA Control Logic to stop DMA for the rest of the frame when it is written into the Row Buffer. It affects the display in the same way as the End of Screen Code (10).

If the Stop DMA feature is not used, all characters after an End of Row character are ignored, except for the End of Screen character, which operates normally. All characters after an End of Screen character are ignored.

NOTE:
If a Stop DMA character is not the last character in a burst or row, DMA is not stopped until after the next character is read. In this situation, a dummy character must be placed in memory after the Stop DMA character.

Field Attributes

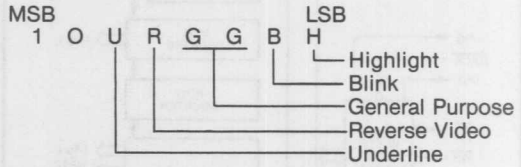
The field attributes are control codes which affect the visual characteristics for a field of characters, starting at the character following the code up to, and including, the character which precedes the *next* field attribute code, or up to the end of the frame. The field attributes are reset during the vertical retrace interval.

There are six field attributes:

1. *Blink* — Characters following the code are caused to blink by activating the Video Suppression output (VSP). The blink frequency is equal to the screen refresh frequency divided by 32.
2. *Highlight* — Characters following the code are caused to be highlighted by activating the Highlight output (HGLT).
3. *Reverse Video* — Characters following the code are caused to appear with reverse video by activating the Reverse Video output (RVV).
4. *Underline* — Characters following the code are caused to be underlined by activating the Light Enable output (LTEN).

5,6. *General Purpose* — There are two additional WD8275 outputs which act as general purpose, independently programmable field attributes. $GPA_{0\text{-}1}$ are active high outputs.

FIELD ATTRIBUTE CODE



H = 1 for highlighting
B = 1 for blinking
R = 1 for reverse video
U = 1 for underline
GG = GPA_1, GPA_0

NOTE:
More than one attribute can be enabled at the same time. If the blinking and reverse video attributes are enabled simultaneously, only the reversed characters will blink.

The WD8275 can be programmed to provide visible or invisible field attribute characters.

If the WD8275 is programmed in the visible field attribute mode, all field attributes will occupy a position on the screen. They will appear as blanks caused by activation of the Video Suppression output (VSP). The chosen visual attributes are activated after this blanked character.

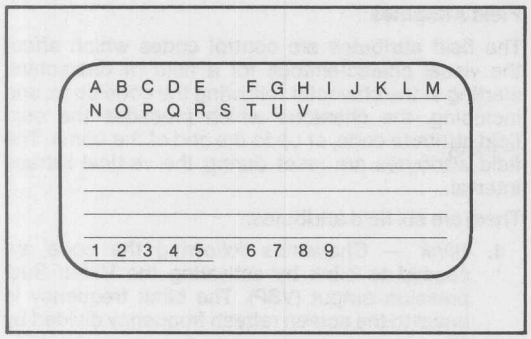


Figure 24.
EXAMPLE OF A VISIBLE FIELD ATTRIBUTE MODE (UNDERLINE ATTRIBUTE)

If the WD8275 is programmed in the invisible field attribute mode, the WD8275 FIFO is activated.

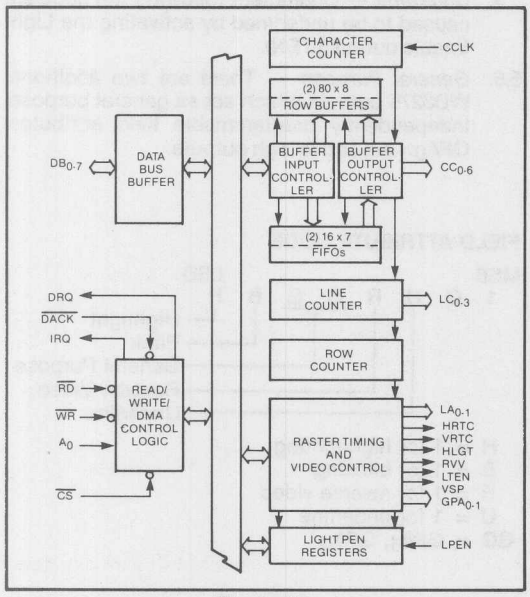


Figure 25.
BLOCK DIAGRAM SHOWING FIFO ACTIVATION

Each row buffer has a corresponding FIFO. These FIFOs are 16 characters by 7 bits in size.

When a field attribute is placed in the row buffer during DMA, the buffer input controller recognizes it and places the *next* character in the proper FIFO.

When a field attribute is placed in the Buffer Output Controller during display, it causes the controller to immediately put a character from the FIFO on the Character Code outputs (CC_{0-6}). The chosen Visual Attributes are also activated.

Since the FIFO is 16 characters long, no more than 16 field attribute characters may be used per line in this mode. If more are used, a bit in the status word is set and the first characters in the FIFO are written over and lost.

NOTE:
Since the FIFO is 7 bits wide, the MSB of any characters put in it are stripped off. Therefore, a Visual Attribute or Special Code must *not* immediately follow a field attribute code. If this situation does occur, the Visual Attribute or Special Code will be treated as a normal display character.

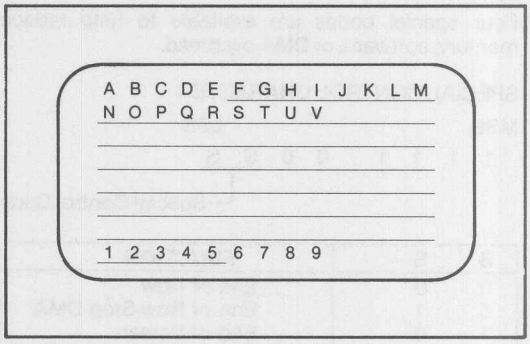


Figure 26.
EXAMPLE OF THE INVISIBLE FIELD ATTRIBUTE MODE (UNDERLINE ATTRIBUTE)

Field and Character Attribute Interaction

Character Attribute Symbols are affected by the Reverse Video (RVV) and General Purpose (GPA_{0-1}) field attributes. They are not affected by Underline, Blink or Highlight field attributes; however, these characteristics can be programmed *individually* for Character Attribute Symbols.

Cursor Timing

The cursor location is determined by a cursor row register and a character position register which are loaded by command to the controller. The cursor can be programmed to appear on the display as:

1. a blinking underline
2. a blinking reverse video block
3. a non-blinking underline
4. a non-blinking reverse video block

The cursor blinking frequency is equal to the screen refresh frequency divided by 16.

If a non-blinking reverse video *cursor* appears in a non-blinking reverse video *field*, the cursor will appear as a normal video block.

If a non-blinking underline *cursor* appears in a non-blinking underline *field*, the cursor will not be visible.

Light Pen Detection

A light pen consists of a micro switch and a tiny light sensor. When the light pen is pressed against the CRT screen, the micro switch enables the light sensor. When the raster sweep reaches the light sensor, it triggers the light pen output.

If the output of the light pen is presented to the WD8275 LPEN input, the row and character position coordinates are stored in a pair of registers. These registers can be read on command. A bit in the status word is set, indicating that the light pen signal was detected. The LPEN input must be a 0 to 1 transition for proper operation.

NOTE:
Due to internal and external delays, the character position coordinate will be off by at least three character positions. This has to be corrected in software.

Device Programming

The WD8275 has two programming registers, the Command Register (CREG) and the Parameter Register (PREG). It also has a Status Register (SREG). The Command Register can only be written into and the Status Registers can only be read from. They are addressed as follows:

A_0	OPERATION	REGISTER
0	Read	PREG
0	Write	PREG
1	Read	SREG
1	Write	CREG

The WD8275 expects to receive a command and a sequence of 0 to 4 parameters, depending on the command. If the proper number of parameter bytes are not received before another command is given, a status flag is set, indicating an improper command.

INSTRUCTION SET

The WD8275 instruction set consists of 8 commands.

COMMAND	NO. OF PARAMETER BYTES
Reset	4
Start Display	0
Stop Display	0
Read Light Pen	2
Load Cursor	2
Enable Interrupt	0
Disable Interrupt	0
Preset Counters	0

In addition, the status of the WD8275 (SREG) can be read by the CPU at any time.

1. Reset Command

	OPERATION	C/P	DESCRIPTION	DATA BUS MSB LSB
Command	Write	1	Reset Command	0 0 0 0 0 0 0 0
Parameters	Write	0	Screen Comp Byte 1	S H H H H H H H
	Write	0	Screen Comp Byte 2	V V R R R R R R
	Write	0	Screen Comp Byte 3	U U U U L L L L
	Write	0	Screen Comp Byte 4	M F C C Z Z Z Z

Action

After the reset command is written, DMA requests stop, WD8275 interrupts are disabled, and the VSP output is used to blank the screen. HRTC and VRTC continue to run. HRTC and VRTC timing are random on power-up.

As parameters are written, the screen composition is defined.

Parameter—S Spaced Rows

S	FUNCTIONS
0	Normal Rows
1	Spaced Rows

Parameter—HHHHHHH Horizontal Characters/Row

H H H H H H H H	NO. OF CHARACTERS PER ROW
0 0 0 0 0 0 0 0	1
0 0 0 0 0 0 0 1	2
0 0 0 0 0 0 1 0	3
.	.
.	.
.	.
1 0 0 1 1 1 1 1	80
1 0 1 0 0 0 0 0	Undefined
.	.
.	.
.	.
1 1 1 1 1 1 1 1	Undefined

Parameter—VV Vertical Retrace Row Count

V	V	NO. OF ROW COUNTS PER VRTC
0	0	1
0	1	2
1	0	3
1	1	4

Parameter—RRRRRR Vertical Rows/Frame

R	R	R	R	R	R	NO. OF ROWS/FRAME
0	0	0	0	0	0	1
0	0	0	0	0	1	2
0	0	0	0	1	0	3
			.			.
			.			.
			.			.
1	1	1	1	1	1	64

Parameter—UUUU Underline Placement

U	U	U	U	LINE NO. OF UNDERLINE
0	0	0	0	1
0	0	0	1	2
0	0	1	0	3
		.		.
		.		.
		.		.
1	1	1	1	16

Parameter—LLLL
Number of Lines per Character Row

L	L	L	L	NO. OF LINES/ROW
0	0	0	0	1
0	0	0	1	2
0	0	1	0	3
		.		.
		.		.
		.		.
1	1	1	1	16

Parameter—M Line Counter Mode

M	LINE COUNTER MODE
0	Mode 0 (Non-Offset)
1	Mode 1 (Offset by 1 Count)

Parameter—F Field Attribute Mode

F	FIELD ATTRIBUTE MODE
0	Transparent
1	Non-Transparent

Parameter—CC Cursor Format

C	C	CURSOR FORMAT
0	0	Blinking reverse video block
0	1	Blinking underline
1	0	Non-blinking reverse video block
1	1	Non-blinking underline

Parameter—ZZZZ Horizontal Retrace Count

Z	Z	Z	Z	NO. OF CHARACTER COUNTS PER HRTC
0	0	0	0	2
0	0	0	1	4
0	0	1	0	6
		.		.
		.		.
		.		.
1	1	1	1	32

NOTE:
uuuu MSB determines blanking of top and bottom lines (1 = blanked, 0 = not blanked).

2. Start Display Command

	OPERATION	A_0	DESCRIPTION	DATA BUS MSB LSB
Command	Write	1	Start Display	0 0 1 S S S B B
No parameters				

SSS Burst Space Code

S	S	S	NO. OF CHARACTER CLOCKS BETWEEN DMA REQUESTS
0	0	0	0
0	0	1	7
0	1	0	15
0	1	1	23
1	0	0	31
1	0	1	39
1	1	0	47
1	1	1	55

BB Burst Count Code

B	B	NO. OF DMA CYCLES PER BURST
0	0	1
0	1	2
1	0	4
1	1	8

Action
WD8275 interrupts are enabled, DMA requests begin, video is enabled, Interrupt Enable and Video Enable Status flags are set.

3. Stop Display Command

	OPERATION	A_0	DESCRIPTION	DATA BUS MSB LSB
Command	Write	1	Start Display	0 1 0 0 0 0 0 0
No parameters				

Action

Disables video, interrupts remain enabled, HRTC and VRTC continue to run, Video Enable status flag is reset, and the "Start Display" command must be given to re-enable the display.

4. Read Light Pen Command

	OPERATION	A_0	DESCRIPTION	DATA BUS MSB LSB
Command	Write	1	Read Light Pen	0 1 1 0 0 0 0 0
Parameters	Read	0	Char. Number	(Char. Position in Row)
	Read	0	Row Number	(Row Number)

Action

The WD8275 is conditioned to supply the contents of the light pen position registers in the next two read cycles of the parameter register. Status flags are not affected.

NOTE:
Software correction of light pen position is required.

5. Load Cursor Position

	OPERATION	A_0	DESCRIPTION	DATA BUS MSB LSB
Command	Write	1	Load Cursor	1 0 0 0 0 0 0 0
Parameters	Write	0	Char. Number	(Char. Position in Row)
	Write	0	Row Number	(Row Number)

Action

The WD8275 is conditioned to place the next two parameter bytes into the cursor position registers. Status flags not affected.

6. Enable Interrupt Command

	OPERATION	A_0	DESCRIPTION	DATA BUS MSB LSB
Command	Write	1	Enable Interrupt	1 0 1 0 0 0 0 0
No parameters				

Action

The interrupt enable flag is set and interrupts are enabled.

7. Disable Interrupt Command

	OPERATION	A_0	DESCRIPTION	DATA BUS MSB LSB
Command	Write	1	Disable Interrupt	1 1 0 0 0 0 0 0
No parameters				

Action

Interrupts are disabled and the interrupt enable status flag is reset.

8. Preset Counters Command

	OPERATION	A_0	DESCRIPTION	DATA BUS MSB LSB
Command	Write	1	Preset Counters	1 1 1 0 0 0 0 0
No parameters				

Action

The internal timing counters are preset, corresponding to a screen display position at the top left corner. Two character clocks are required for this operation. The counters will remain in this state until any other command is given.

This command is useful for system debug and synchronization of clustered CRT displays on a single CPU.

STATUS FLAGS

	OPERATION	A_0	DESCRIPTION	DATA BUS MSB LSB
Command	Read	1	Status Word	0 IE IR LP IC VE OU FO

IE —(Interrupt Enable) Set or reset by command. It enables vertical retrace interrupt. It is automatically set by a "Start Display" command and reset with the "Reset" command.

IR —(Interrupt Request) This flag is set at the beginning of display of the last row of the frame if the interrupt enable flag is set. It is reset after a status read operation.

LP —This flag is set when the light pen input (LPEN) is activated and the light pen registers have been loaded. This flag is automatically reset after a status read.

IC —(Improper Command) This flag is set when a command parameter string is too long or too short. The flag is automatically reset after a status read.

VE —(Video Enable) This flag indicates that video operation of the CRT is enabled. This flag is set on a "Start Display" command, and reset on a "Stop Display" or "Reset" command.

DU —(DMA underrun) This flag is set whenever a data underrun occurs during DMA transfers. Upon detection of DU, the DMA operation is stopped and the screen is blanked until after the vertical retrace interval. This flag is reset after a status read.

FO —(FIFO Overrun) This flag is set whenever the FIFO is overrun. It is reset on a status read.

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature Under Bias ..... 0°C to 70°C
Storage Temperature ..... −65°C to +150°C
Voltage On Any Pin
With Respect to Ground ..... −0.5V to +7V
Power Dissipation ..... 1 Watt

*NOTICE:
Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

DC Characteristics (T_A = 0°C to 70°C; V_{CC} = 5V ±5%)

SYMBOL	PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
V_{IL}	Input Low Voltage	−0.5	0.8	V	
V_{IH}	Input High Voltage	2.0	V_{CC} +0.5V	V	
V_{OL}	Output Low Voltage		0.45	V	I_{OL} = 2.2 mA
V_{OH}	Output High Voltage	2.4		V	I_{OH} = −400 μA
I_{IL}	Input Load Current		±10	μA	V_{IN} = V_{CC} to 0V
I_{OFL}	Output Float Leakage		±10	μA	V_{OUT} = V_{CC} to 0V
I_{CC}	V_{CC} Supply Current		160	mA	

Capacitance (T_A = 25°C; V_{CC} = GND = 0V)

SYMBOL	PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
C_{IN}	Input Capacitance		10	pF	f_C = 1 MHz
$C_{I/O}$	I/O Capacitance		20	pF	Unmeasured pins returned to V_{SS}.

AC Characteristics (T_A = 0°C to 70°C; V_{CC} = 5.0V ±5%; GND = 0V)

BUS PARAMETERS

Read Cycle

SYMBOL	PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
t_{AR}	Address Stable Before READ	0		ns	
t_{RA}	Address Hold Time for READ	0		ns	
t_{RR}	READ Pulse Width	250		ns	
t_{RD}	Data Delay from READ		200	ns	C_L = 150pF
t_{DF}	READ to Data Floating	20	100	ns	C_L min. = 20 pF; C_L max. = 150 pF

Write Cycle

SYMBOL	PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
t_{AW}	Address Stable Before WRITE	0		ns	
t_{WA}	Address Hold Time for WRITE	0		ns	
t_{WW}	WRITE Pulse Width	250		ns	
t_{DW}	Data Setup Time for WRITE	150		ns	
t_{WD}	Data Hold Time for WRITE	0		ns	

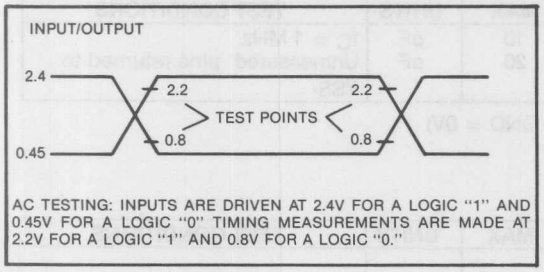
Clock Timing

SYMBOL	PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
t_{CLK}	Clock Period	480		ns	
t_{KH}	Clock High	240		ns	
t_{KL}	Clock Low	160		ns	
t_{KR}	Clock Rise	5	30	ns	
t_{KF}	Clock Fall	5	30	ns	

Other Timing

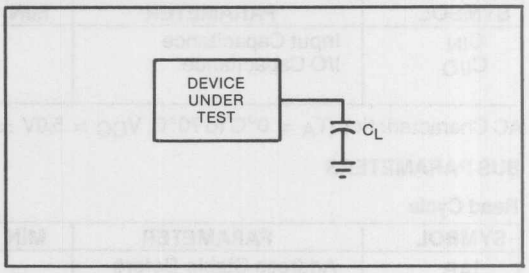
SYMBOL	PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
t_{CC}	Character Code Output Delay		150	ns	C_L = 50 pF
t_{HR}	Horizontal Retrace Output Delay		200	ns	C_L = 50 pF
t_{LC}	Line Count Output Delay		400	ns	C_L = 50 pF
t_{AT}	Control/Attribute Output Delay		275	ns	C_L = 50 pF
t_{VR}	Vertical Retrace Output Delay		275	ns	C_L = 50 pF
t_{RI}	INT↓ from RD↑		250	ns	C_L = 50 pF
t_{WQ}	DRQ↑ from WR↑		250	ns	C_L = 50 pF
t_{RQ}	DRQ↓ from WR↓		200	ns	C_L = 50 pF
t_{LR}	DACK↓ to WR↓	0		ns	
t_{RL}	WR↑ to DACK↑	0		ns	
t_{PR}	LPEN Rise		50	ns	
t_{PH}	LPEN Hold	100		ns	

AC Testing Input, Output Wave Form



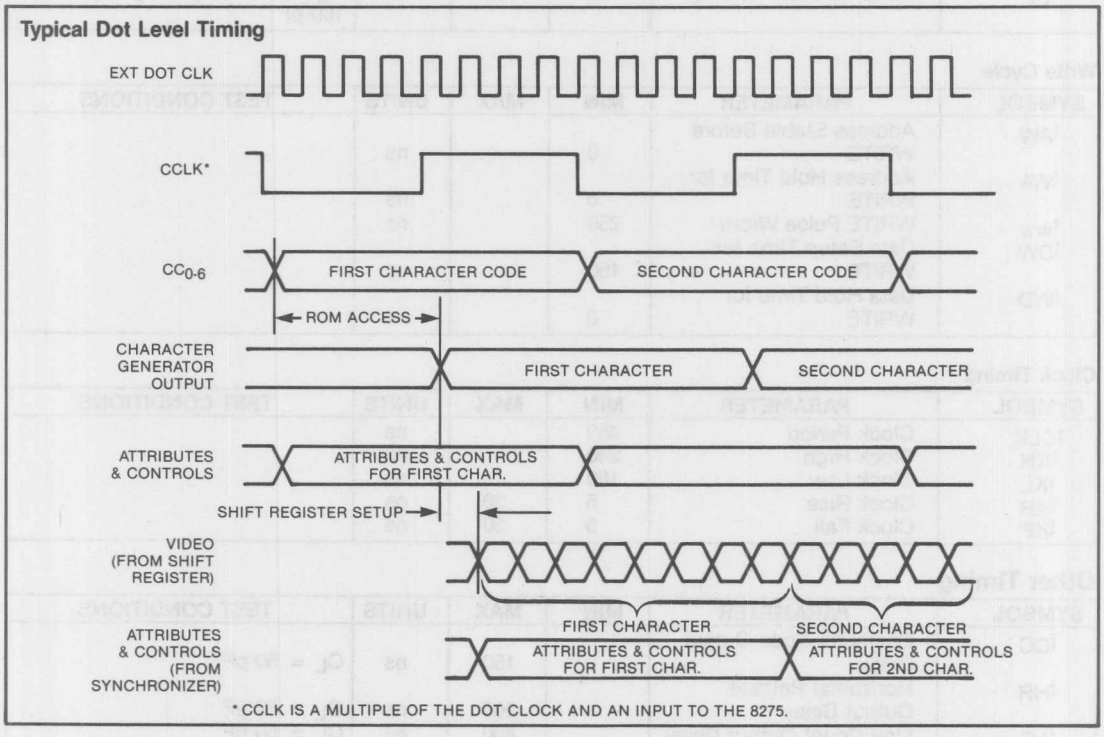
AC TESTING: INPUTS ARE DRIVEN AT 2.4V FOR A LOGIC "1" AND 0.45V FOR A LOGIC "0" TIMING MEASUREMENTS ARE MADE AT 2.2V FOR A LOGIC "1" AND 0.8V FOR A LOGIC "0."

AC Testing Load Circuit



WAVEFORMS

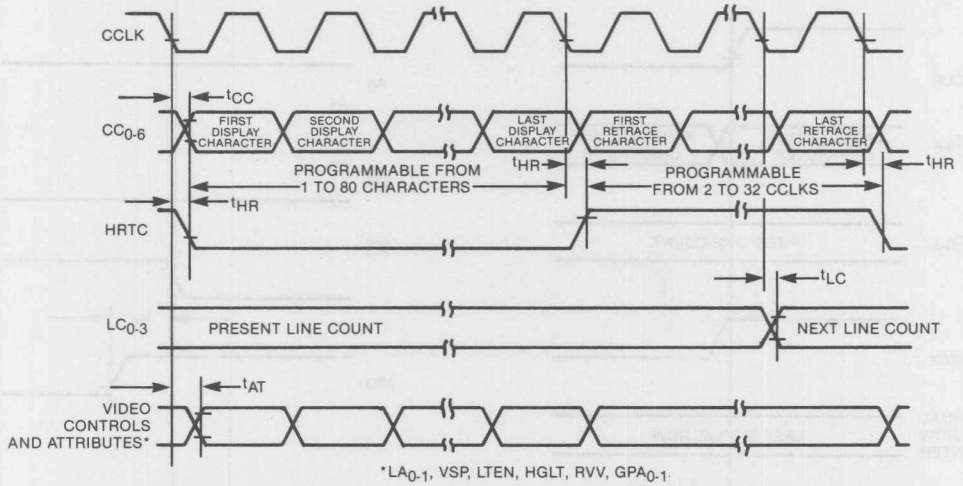
Typical Dot Level Timing



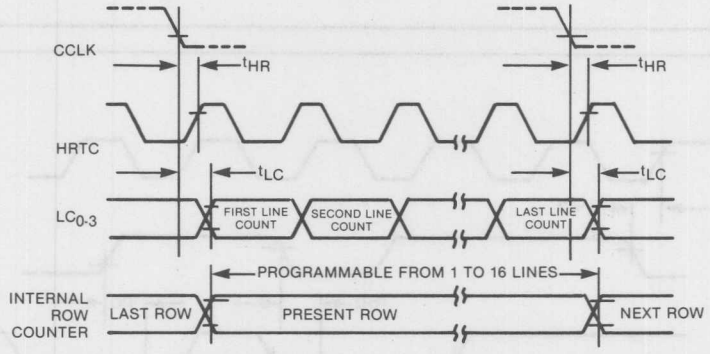
*CCLK IS A MULTIPLE OF THE DOT CLOCK AND AN INPUT TO THE 8275.

WAVEFORMS (Continued)

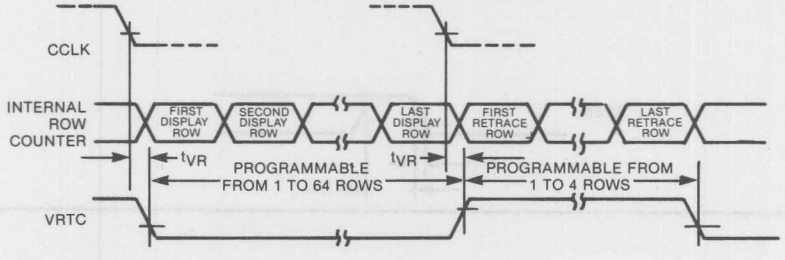
Line Timing



Row Timing

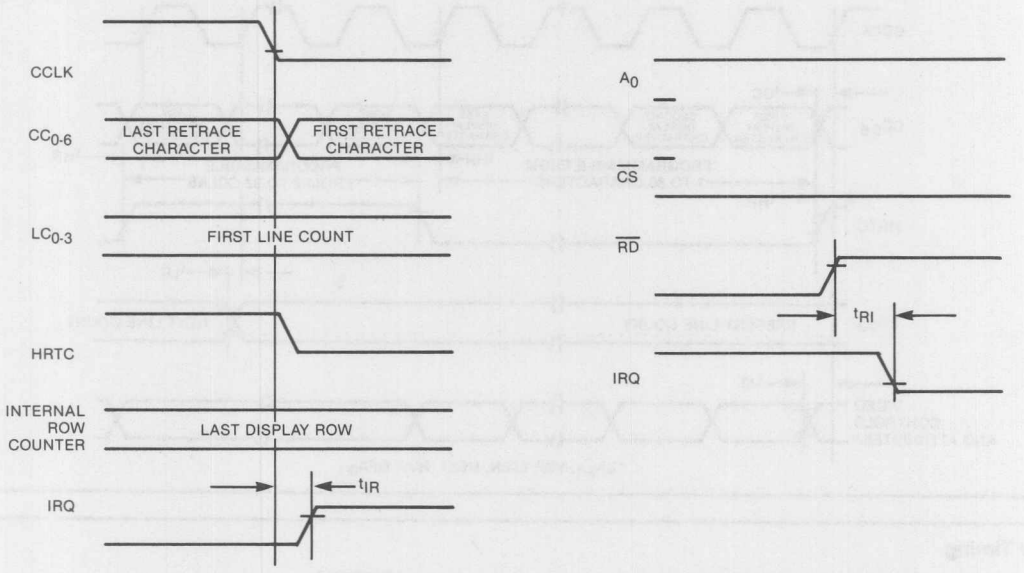


Frame Timing

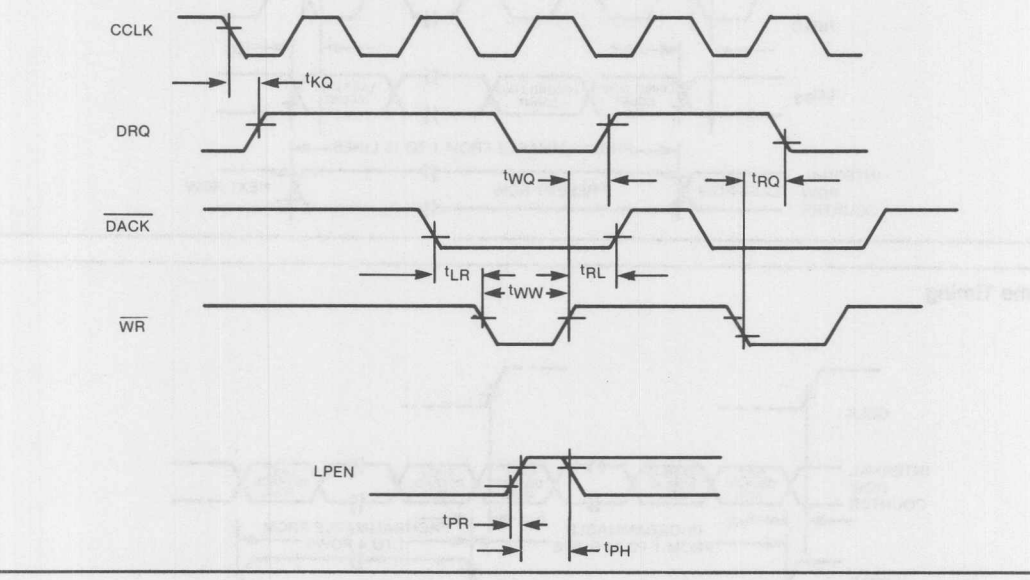


WAVEFORMS (Continued)

Interrupt Timing

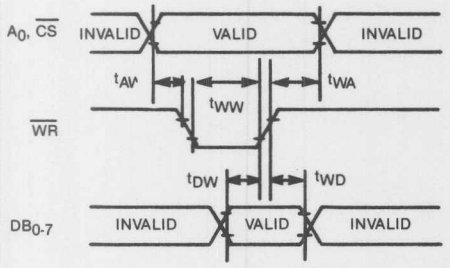


DMA Timing

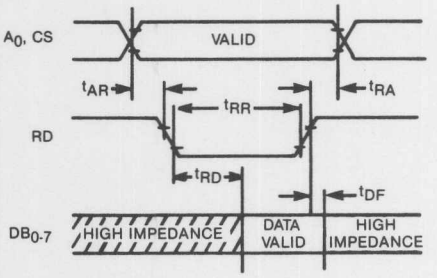


WAVEFORMS (Continued)

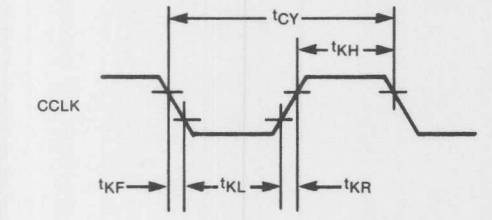
Write Timing



Read Timing



Clock Timing



See page 429 for ordering information.

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WD8276 Small System CRT Controller

FEATURES

- PROGRAMMABLE SCREEN AND CHARACTER FORMAT
- 6 INDEPENDENT VISUAL FIELD ATTRIBUTES
- CURSOR CONTROL (4 TYPES)
- DUAL ROW BUFFERS
- SINGLE +5V SUPPLY
- 40-PIN PACKAGE

GENERAL DESCRIPTION

The WD8276 Small System CRT Controller is a single chip device intended to interface CRT raster scan displays with Intel microcomputers in minimum device-count systems. Its primary function is to refresh the display by buffering character information from main memory and keeping track of the display position of the screen. The flexibility designed into the WD8276 will allow simple interface to almost any raster scan CRT display with a minimum system IC count.

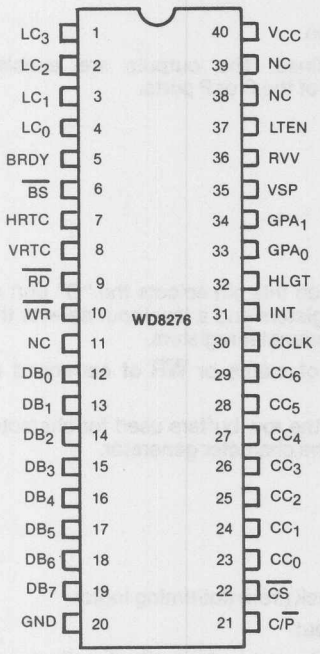


Figure 1. PIN CONFIGURATION

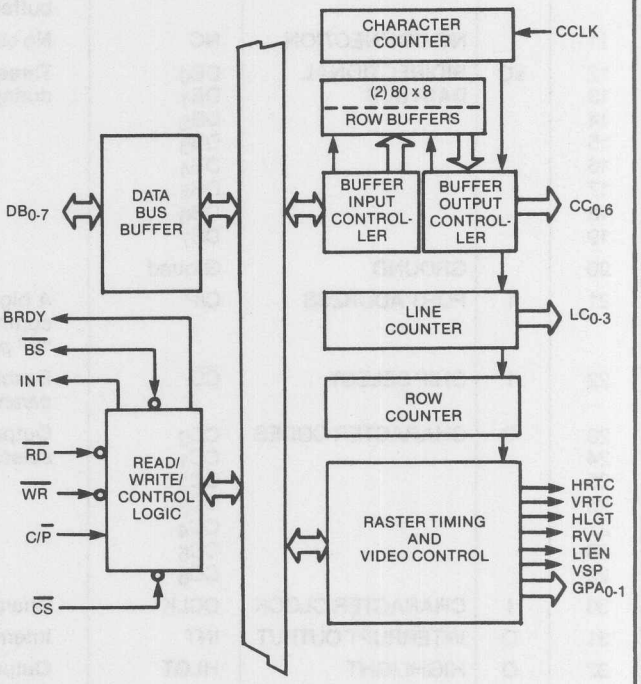


Figure 2. BLOCK DIAGRAM

TABLE 1. PIN DESCRIPTIONS

PIN NO.	TYPE	PIN NAME	SYMBOL	FUNCTION
1 2 3 4	O	LINE COUNT	LC_3 LC_2 LC_1 LC_0	Output from the line counter which is used to address the character generator for the line positions on the screen.
5	O	BUFFER READY	BRDY	Output signal indicating that a Row Buffer is ready for loading of character data.
6	I	BUFFER SELECT	$\overline{BS}$	Input signal enabling $\overline{WR}$ for character data into the Row Buffers.
7	O	HORIZONTAL RETRACE	HRTC	Output signal which is active during the programmed horizontal retrace interval. During this period the VSP output is high and the LTEN output is low.
8	O	VERTICAL RETRACE	VRTC	Output signal which is active during the programmed vertical retrace interval. During this period the VSP output is high and the LTEN output is low.
9	I	READ INPUT	$\overline{RD}$	A control signal to read registers.
10	I	WRITE INPUT	$\overline{WR}$	A control signal to write commands into the control registers or write data into the row buffers.
11		NO CONNECTION	NC	No connection
12 13 14 15 16 17 18 19	I/O	BIDIRECTIONAL DATA BUS	DB_0 DB_1 DB_2 DB_3 DB_4 DB_5 DB_6 DB_7	Three-state lines. The outputs are enabled during a read of the C or P ports.
20		GROUND	Ground	
21	I	PORT ADDRESS	$C/\overline{P}$	A high input on this pin selects the "C" port or command registers and a low input selects the "P" port or parameter registers.
22	I	CHIP SELECT	$\overline{CS}$	Enables $\overline{RD}$ of status or $\overline{WR}$ of command or parameters.
23 24 25 26 27 28 29	O	CHARACTER CODES	CC_0 CC_1 CC_2 CC_3 CC_4 CC_5 CC_6	Output from the row buffers used for character selection in the character generator.
30	I	CHARACTER CLOCK	CCLK	Character clock (from dot/timing logic).
31	O	INTERRUPT OUTPUT	INT	Interrupt output.
32	O	HIGHLIGHT	HLGT	Output signal used to intensify the display at particular positions on the screen as specified by the field attribute codes.
33 34	O	GENERAL PURPOSE ATTRIBUTE CODES	GPA_1 GPA_0	Outputs which are enabled by the general purpose field attribute codes.

TABLE 1. PIN DESCRIPTIONS

PIN NO.	TYPE	PIN NAME	SYMBOL	FUNCTION
35	O	VIDEO SUPPRESSION	VSP	Output signal used to blank the video signal to the CRT. This output is active: —during the horizontal and vertical retrace intervals. —at the top and bottom lines of rows if underline is programmed to be number 8 or greater. —when an end of row or end of screen code is detected. —when a Row Buffer underrun occurs. —at regular intervals (1/16 frame frequency for cursor, 1/32 frame frequency for attributes) — to create blinking displays as specified by cursor or field attribute programming.
36	O	REVERSE VIDEO	RVV	Output signal used to activate the CRT circuitry to reverse the video signal. This output is active at the cursor position if a reverse video block cursor is programmed or at the positions specified by the field attribute codes.
37	O	LIGHT ENABLE	LTEN	Output signal used to enable the video signal to the CRT. This output is active at the programmed underline cursor position, and at positions specified by attribute codes.
38		NO CONNECTION	NC	No connection.
39		NO CONNECTION	NC	No connection.
40		+5V POWER SUPPLY	V_{CC}	+5V power supply.

FUNCTIONAL DESCRIPTION

Data Bus Buffer

This 3-state, bidirectional, 8-bit buffer is used to interface the WD8276 to the system Data Bus.

This functional block accepts inputs from the System Control Bus and generates control signals for overall device operation. It contains the Command, Parameter, and Status Registers that store the various control formats for the device functional definition.

C/P	OPERATION	REGISTER
0	Read	RESERVED
0	Write	PARAMETER
1	Read	STATUS
1	Write	COMMAND

$\overline{RD}$ (READ)

A "low" on this input informs the WD8276 that the CPU is reading status information from the WD8276.

$\overline{WR}$ (WRITE)

A "low" on this input informs the WD8276 that the CPU is writing data or control words to the WD8276.

$\overline{CS}$ (CHIP SELECT)

A "low" on this input selects the WD8276 for $\overline{RD}$ or $\overline{WR}$ of Commands, Status, and Parameters.

BRDY (BUFFER READY)

A "high" on this output indicates that the WD8276 is ready to receive character data.

BS (BUFFER SELECT)

A "low" on this input enables $\overline{WR}$ of character data to the WD8276 row buffers.

INT (INTERRUPT)

A "high" on this output informs the CPU that the WD8276 needs interrupt service.

C/P	RD	WR	CS	BS	
0	0	1	0	1	Reserved
0	1	0	0	1	Write WD8276 Parameter
1	0	1	0	1	Read WD8276 Status
1	1	0	0	1	Write WD8276 Command
X	1	0	1	0	Write WD8276 Row Buffer
X	1	1	X	X	High Impedance
X	X	X	1	1	High Impedance

Character Counter

The Character Counter is a programmable counter that is used to determine the number of characters to be displayed per row and the length of the horizontal retrace interval. It is driven by the CCLK (Character Clock) input, which should be derived from the external dot clock.

Line Counter

The Line Counter is a programmable counter that is used to determine the number of horizontal lines (Raster Scans) per character row. Its outputs are used to address the external character generator.

Row Counter

The Row Counter is a programmable counter that is used to determine the number of character rows to be displayed per frame and length of the vertical retrace interval.

Raster Timing and Video Controls

The Raster Timing circuitry controls the timing of the HRTC (Horizontal Retrace) and VRTC (Vertical Retrace) outputs. The Video Control circuitry controls the generation of HGLT (Highlight), RVV (Reverse Video), LTEN (Light Enable), VSP (Video Suppress), and GPA_{0-1} (General Purpose Attribute) outputs.

Row Buffers

The Row Buffers are two 80-character buffers. They are filled from the microcomputer system memory with the character codes to be displayed. While one row buffer is displaying a row of characters,

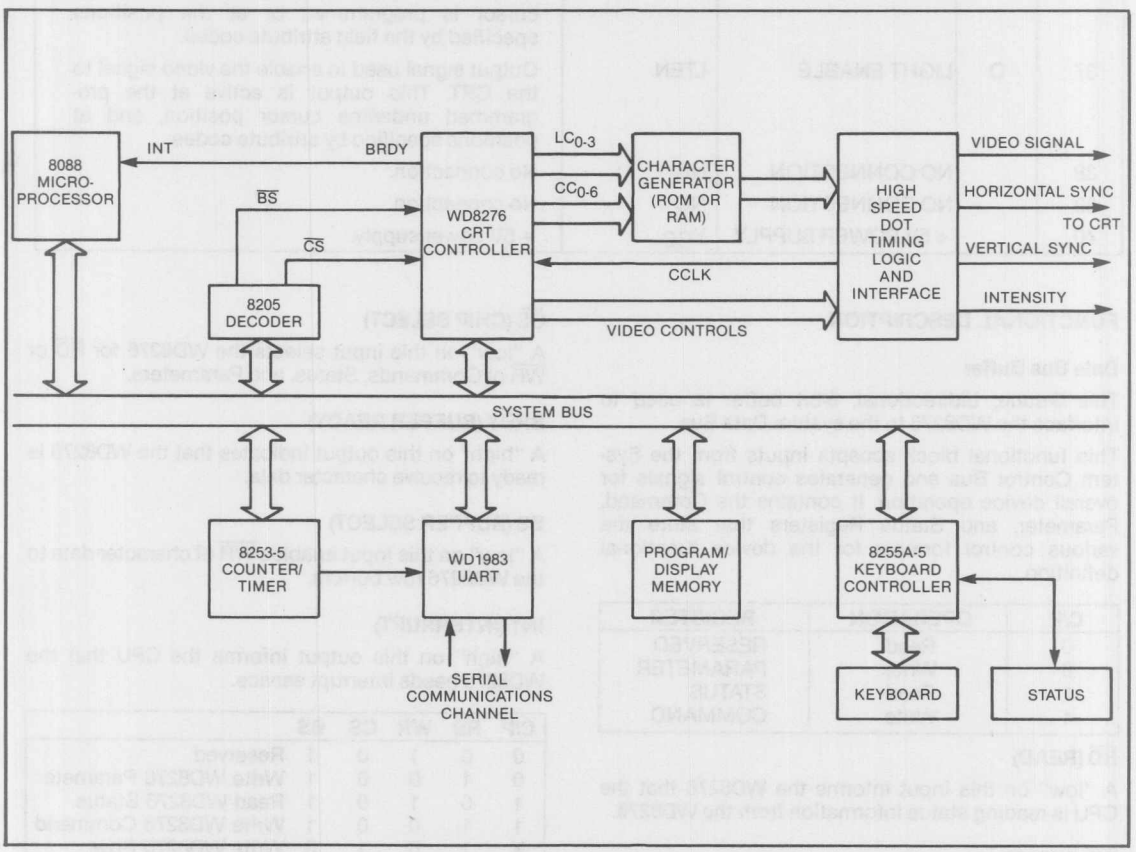


Figure 3. CRT SYSTEM BLOCK DIAGRAM

the other is being filled with the next row of characters.

Buffer Input/Output Controllers

The Buffer Input/Output Controllers decode the characters being placed in the row buffers. If the character is a field attribute or special code, they control the appropriate action. (Example: A "Highlight" field attribute will cause the Buffer Output Controller to activate the HGLT output.)

SYSTEM OPERATION

The WD8276 is programmable to a large number of different display formats. It provides raster timing, display row buffering, visual attribute decoding and cursor timing.

It is designed to interface with standard character generators for dot matrix decoding. Dot level timing must be provided by external circuitry.

GENERAL SYSTEMS OPERATIONAL DESCRIPTION

Display characters are retrieved from memory and displayed on a row-by-row basis. The WD8276 has two row buffers. While one row buffer is being used for display, the other is being filled with the next row of characters to be displayed. The number of display characters per row and the number of character rows per frame are software programmable, providing easy interface to most CRT displays. (See Programming Section.)

The WD8276 uses BRDY to request character data to fill the row buffer that is not being used for display.

The WD8276 displays character rows one scan line at a time. The number of scan lines per character row, the underline position, and blanking of top and bottom lines are programmable. (See Programming Section.)

The WD8276 provides special Control Codes which can be used to minimize overhead. It also provides Visual Attribute Codes to cause special action on the screen without the use of the character generator. (See Visual Attributes Section.)

The WD8276 also controls raster timing. This is done by generating Horizontal Retrace (HRTC) and Vertical Retrace (VRTC) signals. The timing of these signals is also programmable.

The WD8276 can generate a cursor. Cursor location and format are programmable. (See Programming Section.)

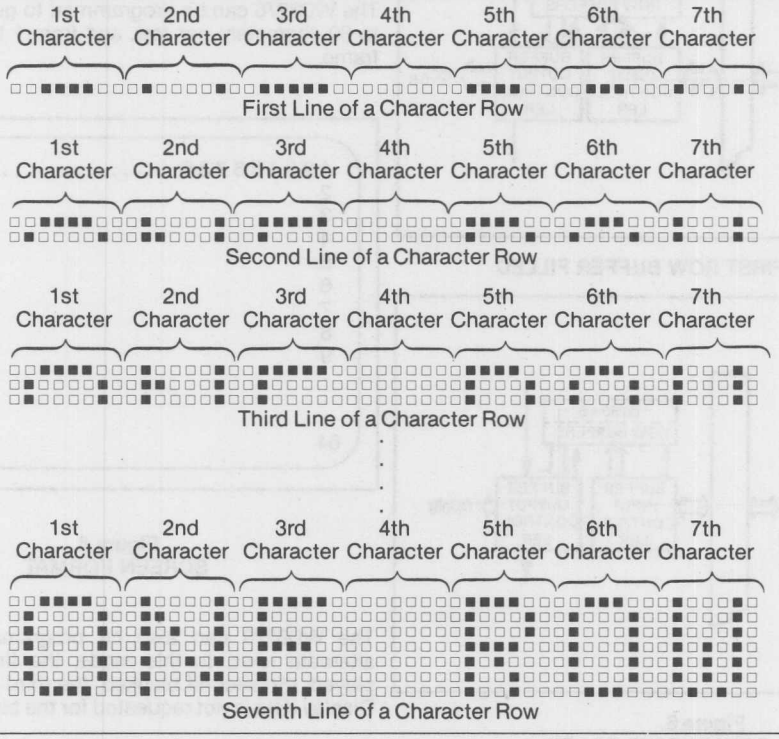


Figure 4. DISPLAY OF A CHARACTER ROW

DISPLAY ROW BUFFERING

Before the start of a frame, the WD8276 uses BRDY and $\overline{BS}$ to fill one row buffer with characters.

When the first horizontal sweep is started, character codes are output to the character generator from the row buffer just filled. Simultaneously, the other row buffer is filled with the next row of characters.

After all the lines of the character row are scanned, the buffers are swapped and the same procedure is followed for the next row.

This process is repeated until all of the character rows are displayed.

Row Buffering allows the CPU access to the display memory at all times except during Buffer Loading (about 25%). This compares favorably to alternative approaches which restrict CPU access to the display memory to occur only during horizontal and vertical retrace intervals (80% of the bus time is used to refresh the display.)

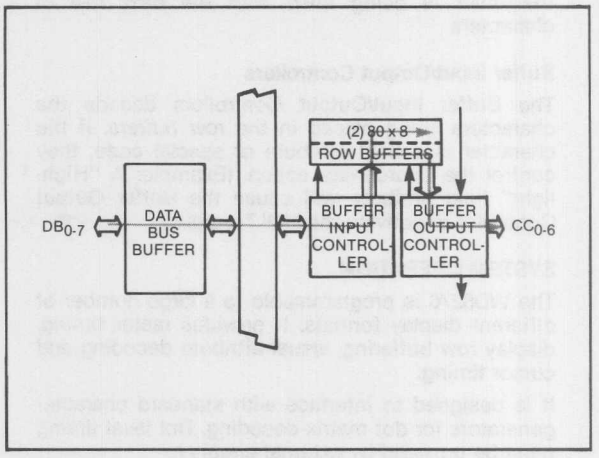


Figure 7.
FIRST ROW BUFFER FILLED WITH THIRD ROW, SECOND ROW DISPLAYED

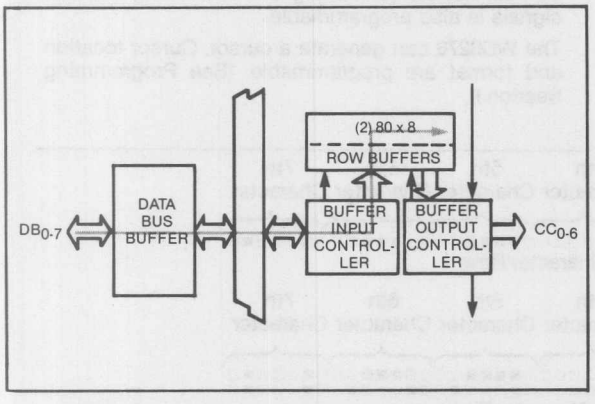


Figure 5. FIRST ROW BUFFER FILLED

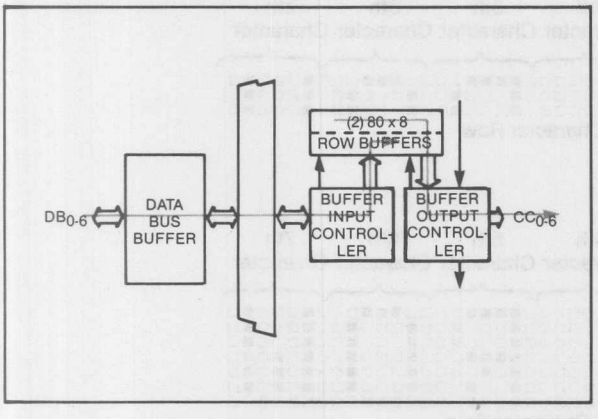


Figure 6.
SECOND ROW BUFFER FILLED, FIRST ROW DISPLAYED

DISPLAY FORMAT

Screen Format

The WD8276 can be programmed to generate from 1 to 80 characters per row, and from 1 to 64 rows per frame.

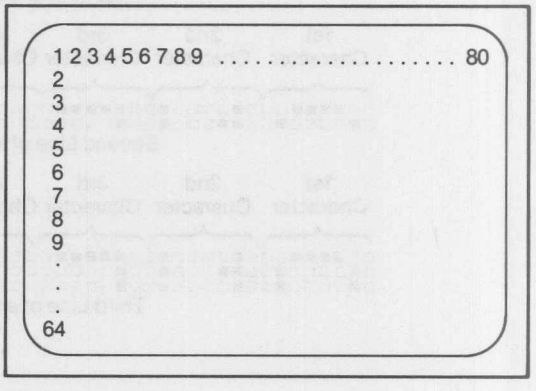


Figure 8.
SCREEN FORMAT

The WD8276 can also be programmed to blank alternate rows. In this mode, the first row is displayed, the second blanked, the third displayed, etc. Display data is not requested for the blanked rows.

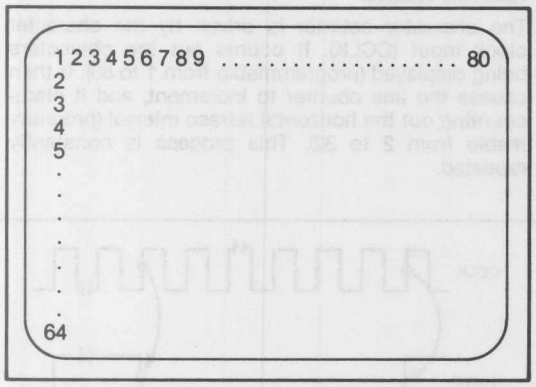


Figure 9.
BLANK ALTERNATE ROWS MODE

Row Format

The WD8276 is designed to hold the line count stable while outputting the appropriate character codes during each horizontal sweep. The line count is incremented during horizontal retrace and the whole row of character codes are output again during the next sweep. This is continued until the entire character row is displayed.

The number of lines (horizontal sweeps) per character row is programmable from 1 to 16.

The output of the line counter can be programmed to be in one of two modes.

In mode 0, the output of the line *counter* is the same as the line *number*.

Line Number	Line Counter Mode 0	Line Counter Mode 1
0	0 0 0 0	1 1 1 1
1	0 0 0 1	0 0 0 0
2	0 0 1 0	0 0 0 1
3	0 0 1 1	0 0 1 0
4	0 1 0 0	0 0 1 1
5	0 1 0 1	0 1 0 0
6	0 1 1 0	0 1 0 1
7	0 1 1 1	0 1 1 0
8	1 0 0 0	0 1 1 1
9	1 0 0 1	1 0 0 0
10	1 0 1 0	1 0 0 1
11	1 0 1 1	1 0 1 0
12	1 1 0 0	1 0 1 1
13	1 1 0 1	1 1 0 0
14	1 1 1 0	1 1 0 1
15	1 1 1 1	1 1 1 0

Figure 10.
EXAMPLE OF A 16-LINE FORMAT

In mode 1, the line *counter* is offset by one from the line *number*.

NOTE:
In mode 1, while the *first* line (line number 0) is being displayed, the *last* count is output by the line counter (see examples).

Line Number	Line Counter Mode 0	Line Counter Mode 1
0	0 0 0 0	1 0 0 1
1	0 0 0 1	0 0 0 0
2	0 0 1 0	0 0 0 1
3	0 0 1 1	0 0 1 0
4	0 1 0 0	0 0 1 1
5	0 1 0 1	0 1 0 0
6	0 1 1 0	0 1 0 1
7	0 1 1 1	0 1 1 0
8	1 0 0 0	0 1 1 1
9	1 0 0 1	1 0 0 0

Figure 11.
EXAMPLE OF A 10-LINE FORMAT

Mode 0 is useful for character generators that leave address zero blank and start at address 1. Mode 1 is useful for character generators which start at address zero.

Underline placement is also programmable (from line *number* 0 to 15). This is independent of the line *counter* mode.

If the line *number* of the underline is greater than 7 (line *number* MSB = 1), then the top and bottom lines will be blanked.

Line Number	Line Counter Mode 0	Line Counter Mode 1
0	0 0 0 0	1 0 1 1
1	0 0 0 1	0 0 0 0
2	0 0 1 0	0 0 0 1
3	0 0 1 1	0 0 1 0
4	0 1 0 0	0 0 1 1
5	0 1 0 1	0 1 0 0
6	0 1 1 0	0 1 0 1
7	0 1 1 1	0 1 1 0
8	1 0 0 0	0 1 1 1
9	1 0 0 1	1 0 0 0
10	1 0 1 0	1 0 0 1
11	1 0 1 1	1 0 1 0

Top and Bottom Lines are Blanked

Figure 12.
UNDERLINE IN LINE NUMBER 10

If the line *number* of the underline is less than or equal to 7 (line *number* MSB = 0), then the top and bottom lines will *not* be blanked.

Line Number		Line Counter Mode 0	Line Counter Mode 1
0	□ □ □ □ □ □ □ □	0 0 0 0	0 1 1 1
1	□ □ □ ■ □ □ □	0 0 0 1	0 0 0 0
2	□ □ ■ □ ■ □ □	0 0 1 0	0 0 0 1
3	□ ■ □ □ □ ■ □	0 0 1 1	0 0 1 0
4	□ ■ □ □ □ ■ □	0 1 0 0	0 0 1 1
5	□ ■ ■ ■ ■ ■ □	0 1 0 1	0 1 0 0
6	□ ■ □ □ □ ■ □	0 1 1 0	0 1 0 1
7	■ ■ ■ ■ ■ ■ ■	0 1 1 1	0 1 1 0

Top and Bottom Lines are not Blanked

Figure 13.
UNDERLINE IN LINE NUMBER 7

If the line *number* of the underline is greater than the maximum number of lines, the underline will not appear.

Blanking is accomplished by the VSP (Video Suppression) signal. Underline is accomplished by the LTEN (Light Enable) signal.

Dot Format

Dot width and character width are dependent upon the external timing and control circuitry.

Dot level timing circuitry should be designed to accept the parallel output of the character generator and shift it out serially at the rate required by the CRT display.

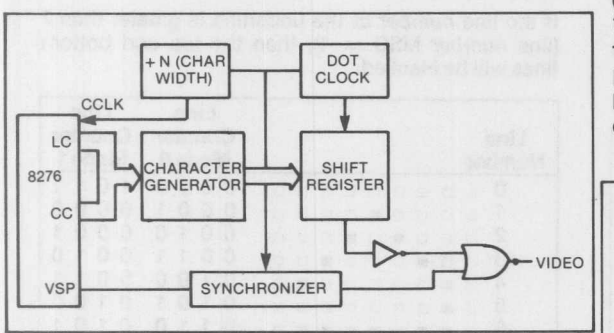


Figure 14.
TYPICAL DOT LEVEL BLOCK DIAGRAM

Dot width is a function of dot clock frequency.

Character width is a function of the character generator width.

Horizontal character spacing is a function of the shift register length.

NOTE:
Video control and timing signals must be synchronized with the video signal due to the character generator access delay.

RASTER TIMING

The character counter is driven by the character clock input (CCLK). It counts out the characters being displayed (programmable from 1 to 80). It then causes the line counter to increment, and it starts counting out the horizontal retrace interval (programmable from 2 to 32). This process is constantly repeated.

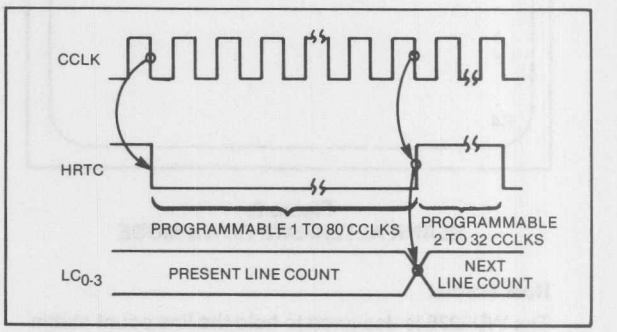


Figure 15.
LINE TIMING

The line counter is driven by the character counter. It is used to generate the line address outputs (LC_{0-3}) for the character generator. After it counts all of the lines in a character row (programmable from 1 to 16), it increments the row counter, and starts over again. (See Character Format Section for detailed description of Line Counter functions.)

The row counter is an internal counter driven by the line counter. It controls the functions of the row buffers and counts the number of character rows displayed.

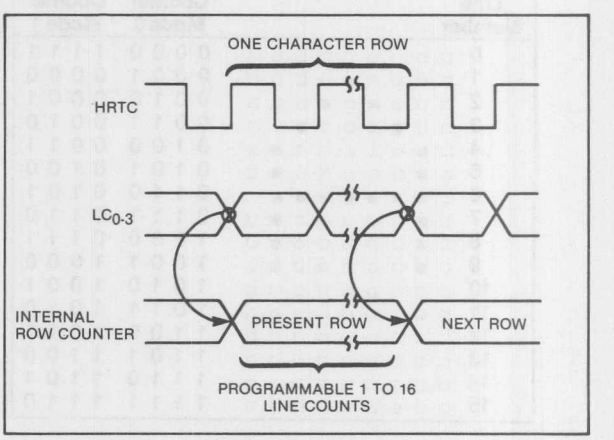


Figure 16.
ROW TIMING

After the row counter counts all of the rows in a frame (programmable from 1 to 64), it starts counting out the vertical retrace interval (programmable from 1 to 4).

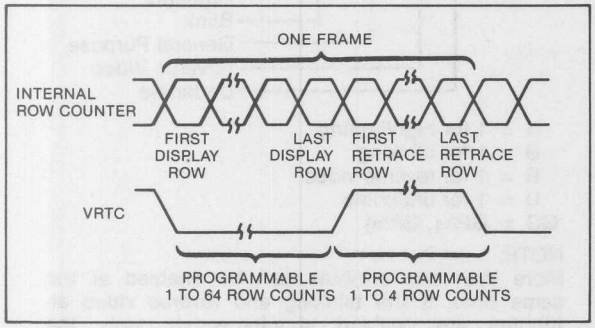


Figure 17.
FRAME TIMING

The Video Suppression Output (VSP) is active during horizontal and vertical retrace intervals.

Dot level timing circuitry must synchronize these outputs with the video signal to the CRT Display.

INTERRUPT TIMING

The WD8276 can be programmed to generate an interrupt request at the end of each frame. If the WD8276 interrupt enable flag is set, an interrupt request will occur at the *beginning* of the *last display row.*

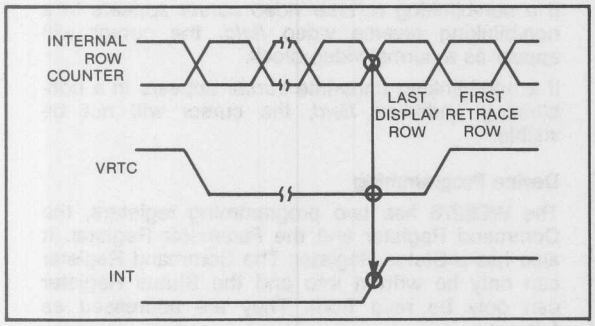


Figure 18.
BEGINNING OF INTERRUPT

INT will go inactive after the status register is read.

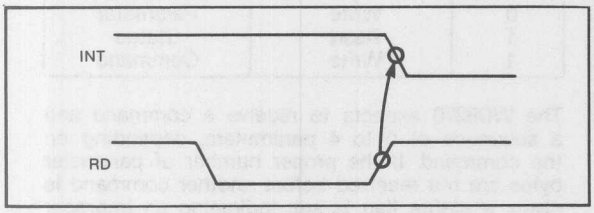


Figure 19.
END OF INTERRUPT

A reset command will also cause INT to go inactive, but this is not recommended during normal service.

NOTE:
Upon power-up, the WD8276 Interrupt Enable Flag may be set. As a result, the user's cold start routine should write a reset command to the WD8276 before system interrupts are enabled.

VISUAL ATTRIBUTES AND SPECIAL CODES

The characters processed by the WD8276 are 8-bit quantities. The character code outputs provide the character generator with 7 bits of address. The Most Significant Bit is the extra bit and it is used to determine if it is a normal display character (MSB = 0), or if it is a Field Attribute or Special Code (MSB = 1).

Special Codes

Four special codes are available to help reduce bus usage.

SPECIAL CONTROL CHARACTER

MSB LSB

1 1 1 1 0 0 S S

Special Control Code

S	S	FUNCTION
0	0	End of Row
0	1	End of Row-Stop Buffer Loading
1	0	End of Screen
1	1	End of Screen-Stop Buffer Loading

The End of Row Code (00) activates VSP and holds it to the end of the line.

The End of Row-Stop Buffer Loading (BRDY) Code (01) causes the Buffer Loading Control Logic to stop buffer loading for the rest of the row upon being written into the Row Buffer. It affects the display in the same way as the End of Row Code (00).

The End of Screen Code (10) activates VSP and holds it to the end of the frame.

The End of Screen-Stop Buffer Loading (BRDY) Code (11) causes the Row Buffer Control Logic to stop buffer loading for the rest of the frame upon being written. It affects the display in the same way as the End of Screen Code (10).

If the Stop Buffer Loading feature is not used, all characters after an End of Row character are ignored, except for the End of Screen character, which operates normally. All characters after an End of Screen character are ignored.

NOTE:
If a Stop Buffer Loading is not the last character in a row, Buffer Loading is not stopped until after the next character is read. In this situation, a dummy character must be placed in memory after the Stop Buffer Loading character.

Field Attributes

The field attributes are control codes which affect the visual characteristics for a field of characters, starting at the character following the code up to, and including, the character which precedes the *next* field attribute code, or up to the end of the frame. The field attributes are reset during the vertical retrace interval.

The WD8276 can be programmed to provide visible field attribute characters; all field attribute codes will occupy a position on the screen. These codes will appear as blanks caused by activation of the Video Suppression output (VSP). The chosen visual attributes are activated after this blanked character.

There are six field attributes:

1. *Blink* — Characters following the code are caused to blink by activating the Video Suppression output (VSP). The blink frequency is equal to the screen refresh frequency divided by 32.
2. *Highlight* — Characters following the code are caused to be highlighted by activating the Highlight output (HGLT).
3. *Reverse Video* — Characters following the code are caused to appear with reverse video by activating the Reverse Video output (RVV).
4. *Underline* — Characters following the code are caused to be underlined by activating the Light Enable output (LTEN).

5,6. *General Purpose* — There are two additional WD8276 outputs which act as general purpose, independently programmable field attributes. GPA_{0-1} are active high outputs.

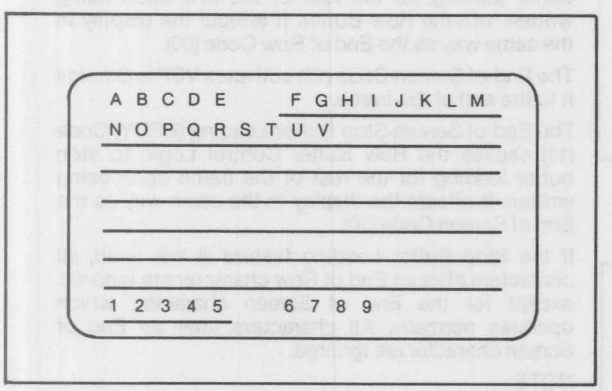
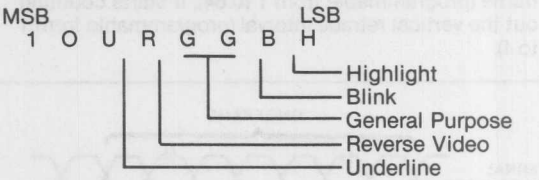


Figure 20.
EXAMPLE OF A VISIBLE FIELD ATTRIBUTE (UNDERLINE ATTRIBUTE)

FIELD ATTRIBUTE CODE



H = 1 for highlighting
B = 1 for blinking
R = 1 for reverse video
U = 1 for underline
GG = GPA_1, GPA_0

NOTE:
More than one attribute can be enabled at the same time. If the blinking and reverse video attributes are enabled simultaneously, only the reversed characters will blink.

Cursor Timing

The cursor location is determined by a cursor row register and a character position register which are loaded by command to the controller. The cursor can be programmed to appear on the display as:

1. a blinking underline
2. a blinking reverse video block
3. a non-blinking underline
4. a non-blinking reverse video block

The cursor blinking frequency is equal to the screen refresh frequency divided by 16.

If a non-blinking reverse video *cursor* appears in a non-blinking reverse video *field*, the cursor will appear as a normal video block.

If a non-blinking underline *cursor* appears in a non-blinking underline *field*, the cursor will not be visible.

Device Programming

The WD8276 has two programming registers, the Command Register and the Parameter Register. It also has a Status Register. The Command Register can only be written into and the Status Register can only be read from. They are addressed as follows:

C/$\overline{P}$	OPERATION	REGISTER
0	Read	Reserved
0	Write	Parameter
1	Read	Status
1	Write	Command

The WD8276 expects to receive a command and a sequence of 0 to 4 parameters, depending on the command. If the proper number of parameter bytes are not received before another command is given, a status flag is set, indicating an improper command.

INSTRUCTION SET

The WD8276 instruction set consists of 7 commands.

In addition, the status of the WD8276 can be read by the CPU at any time.

COMMAND	NO. OF PARAMETER BYTES
Reset	4
Start Display	0
Stop Display	0
Load Cursor	2
Enable Interrupt	0
Disable Interrupt	0
Preset Counters	0

1. Reset Command

	OPERATION	C/P	DESCRIPTION	DATA BUS MSB LSB
Command	Write	1	Reset Command	0 0 0 0 0 0 0 0
Parameters	Write	0	Screen Comp Byte 1	S H H H H H H H
	Write	0	Screen Comp Byte 2	V V R R R R R R
	Write	0	Screen Comp Byte 3	U U U U L L L L
	Write	0	Screen Comp Byte 4	M 1 C C Z Z Z Z

Action

After the reset command is written, BRDY goes inactive, WD8276 interrupts are disabled, and the VSP output is used to blank the screen. HRTC and VRTC continue to run. HRTC and VRTC timing are random on power-up.

As parameters are written, the screen composition is defined.

Parameter—S Spaced Rows

S	FUNCTIONS
0	Normal Rows
1	Spaced Rows

Parameter—HHHHHHH Horizontal Characters/Row

H H H H H H H H	NO. OF CHARACTERS PER ROW
0 0 0 0 0 0 0 0	1
0 0 0 0 0 0 0 1	2
0 0 0 0 0 0 1 0	3
.	.
.	.
.	.
1 0 0 1 1 1 1 1	80
1 0 1 0 0 0 0 0	Undefined
.	.
.	.
.	.
1 1 1 1 1 1 1 1	Undefined

Parameter—VV Vertical Retrace Row Count

V V	NO. OF ROW COUNTS PER VRTC
0 0	1
0 1	2
1 0	3
1 1	4

Parameter—RRRRRR Vertical Rows/Frame

R R R R R R	NO. OF ROWS/FRAME
0 0 0 0 0 0	1
0 0 0 0 0 1	2
0 0 0 0 1 0	3
.	.
.	.
.	.
1 1 1 1 1 1	64

Parameter—UUUU Underline Placement

U U U U	LINE NO. OF UNDERLINE
0 0 0 0	1
0 0 0 1	2
0 0 1 0	3
.	.
.	.
.	.
1 1 1 1	16

Parameter—LLLL Number of Lines per Character Row

L L L L	NO. OF LINES/ROW
0 0 0 0	1
0 0 0 1	2
0 0 1 0	3
.	.
.	.
.	.
1 1 1 1	16

Parameter—M Line Counter Mode

M	LINE COUNTER MODE
0	Mode 0 (Non-Offset)
1	Mode 1 (Offset by 1 Count)

Parameter—CC Cursor Format

C	C	CURSOR FORMAT
0	0	Blinking reverse video block
0	1	Blinking underline
1	0	Non-blinking reverse video block
1	1	Non-blinking underline

NOTE:
uuuu MSB determines blanking of top and bottom lines (1 = blanked, 0 = not blanked).

Parameter—ZZZZ Horizontal Retrace Count

Z	Z	Z	Z	NO. OF CHARACTER COUNTS PER HRTC
0	0	0	0	2
0	0	0	1	4
0	0	1	0	6
		.		.
		.		.
		.		.
1	1	1	1	32

2. Start Display Command

	OPERATION	C/$\overline{P}$	DESCRIPTION	DATA BUS MSB LSB
Command	Write	1	Start Display	0 0 1 0 0 0 0 0
No parameters				

Action

WD8276 interrupts are enabled, BRDY goes active, video is enabled, Interrupt Enable and Video Enable status flags are set.

3. Stop Display Command

	OPERATION	C/$\overline{P}$	DESCRIPTION	DATA BUS MSB LSB
Command	Write	1	Start Display	0 1 0 0 0 0 0 0
No parameters				

Action

Disables video, interrupts remain enabled, HRTC and VRTC continue to run, Video Enable status flag is reset, and the "Start Display" command must be given to reenable the display.

4. Load Cursor Position

	OPERATION	C/$\overline{P}$	DESCRIPTION	DATA BUS MSB LSB
Command	Write	1	Load Cursor	1 0 0 0 0 0 0 0
Parameters	Write Write	0 0	Char. Number Row Number	(Char. Position in Row) (Row Number)

Action

The WD8276 is conditioned to place the next two parameter bytes into the cursor position registers. Status flag not affected.

5. Enable Interrupt Command

	OPERATION	C/$\overline{P}$	DESCRIPTION	DATA BUS MSB LSB
Command	Write	1	Enable Interrupt	1 0 1 0 0 0 0 0
No parameters				

Action

The interrupt enable flag is set and interrupts are enabled.

6. Disable Interrupt Command

	OPERATION	C/$\overline{P}$	DESCRIPTION	DATA BUS MSB LSB
Command	Write	1	Disable Interrupt	1 1 0 0 0 0 0 0
No parameters				

Action

Interrupts are disabled and the interrupt enable status flag is reset.

7. Preset Counters Command

	OPERATION	C/$\overline{P}$	DESCRIPTION	DATA BUS MSB LSB
Command	Write	1	Preset Counters	1 1 1 0 0 0 0 0
No parameters				

Action

The internal timing counters are preset, corresponding to a screen display position at the top left corner. Two character clocks are required for this operation. The counters will remain in this state until any other command is given.

This command is useful for system debug and synchronization of clustered CRT displays on a single CPU.

STATUS FLAGS

	OPERATION	C/$\overline{P}$	DESCRIPTION	DATA BUS MSB LSB
Command	Read	1	Status Word	0 IE IR X IC VE BU X

IE —(Interrupt Enable) Set or reset by command. It enables vertical retrace interrupt. It is automatically set by a "Start Display" command and reset with the "Reset" command.

IR —(Interrupt Request) This flag is set at the beginning of display of the last row of the frame if the interrupt enable flag is set. It is reset after a status read operation.

IC —(Improper Command) This flag is set when a command parameter string is too long or too short. The flag is automatically reset after a status read.

VE —(Video Enable) This flag indicates that video operation of the CRT is enabled. This flag is set on a "Start Display" command, and reset on a "Stop Display" or "Reset" command.

BU —(Buffer Underrun) This flag is set whenever a Row Buffer is not filled with character data in time for a buffer swap required by the display. Upon activation of this bit, buffer loading ceases, and the screen is blanked until after the vertical retrace interval.

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature Under Bias ..... 0°C to 70°C
Storage Temperature ..... −65°C to +150°C
Voltage On Any Pin
With Respect to Ground ..... −0.5V to +7V
Power Dissipation ..... 1 Watt

*NOTICE:
Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

DC Characteristics (T_A = 0°C to 70°C; V_{CC} = 5V ±5%)

SYMBOL	PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
V_{IL}	Input Low Voltage	−0.5	0.8	V	
V_{IH}	Input High Voltage	2.0	V_{CC} +0.5V	V	
V_{OL}	Output Low Voltage		0.45	V	I_{OL} = 2.2 mA
V_{OH}	Output High Voltage	2.4		V	I_{OH} = −400 μA
I_{IL}	Input Load Current		±10	μA	V_{IN} = V_{CC} to 0V
I_{OFL}	Output Float Leakage		±10	μA	V_{OUT} = V_{CC} to 0.45V
I_{CC}	V_{CC} Supply Current		160	mA	

Capacitance (T_A = 25°C; V_{CC} = GND = 0V)

SYMBOL	PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
C_{IN}	Input Capacitance		10	pF	f_C = 1 MHz
$C_{I/O}$	I/O Capacitance		20	pF	Unmeasured pins returned to V_{SS}.

AC Characteristics (T_A = 0°C to 70°C; V_{CC} = 5.0V ±5%; GND = 0V)

BUS PARAMETERS (Note 1)

Read Cycle

SYMBOL	PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
t_{AR}	Address Stable Before READ	0		ns	
t_{RA}	Address Hold Time for READ	0		ns	
t_{RR}	READ Pulse Width	250		ns	
t_{RD}	Data Delay from READ		200	ns	C_L = 150pF
t_{DF}	READ to Data Floating	20	100	ns	

Write Cycle

SYMBOL	PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
t_{AW}	Address Stable Before WRITE	0		ns	
t_{WA}	Address Hold Time for WRITE	0		ns	
t_{WW}	WRITE Pulse Width	250		ns	
t_{DW}	Data Setup Time for WRITE	150		ns	
t_{WD}	Data Hold Time for WRITE	0		ns	

Clock Timing

SYMBOL	PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
t_{CLK}	Clock Period	480		ns	
t_{KH}	Clock High	240		ns	
t_{KL}	Clock Low	160		ns	
t_{KR}	Clock Rise	5	30	ns	
t_{KF}	Clock Fall	5	30	ns	

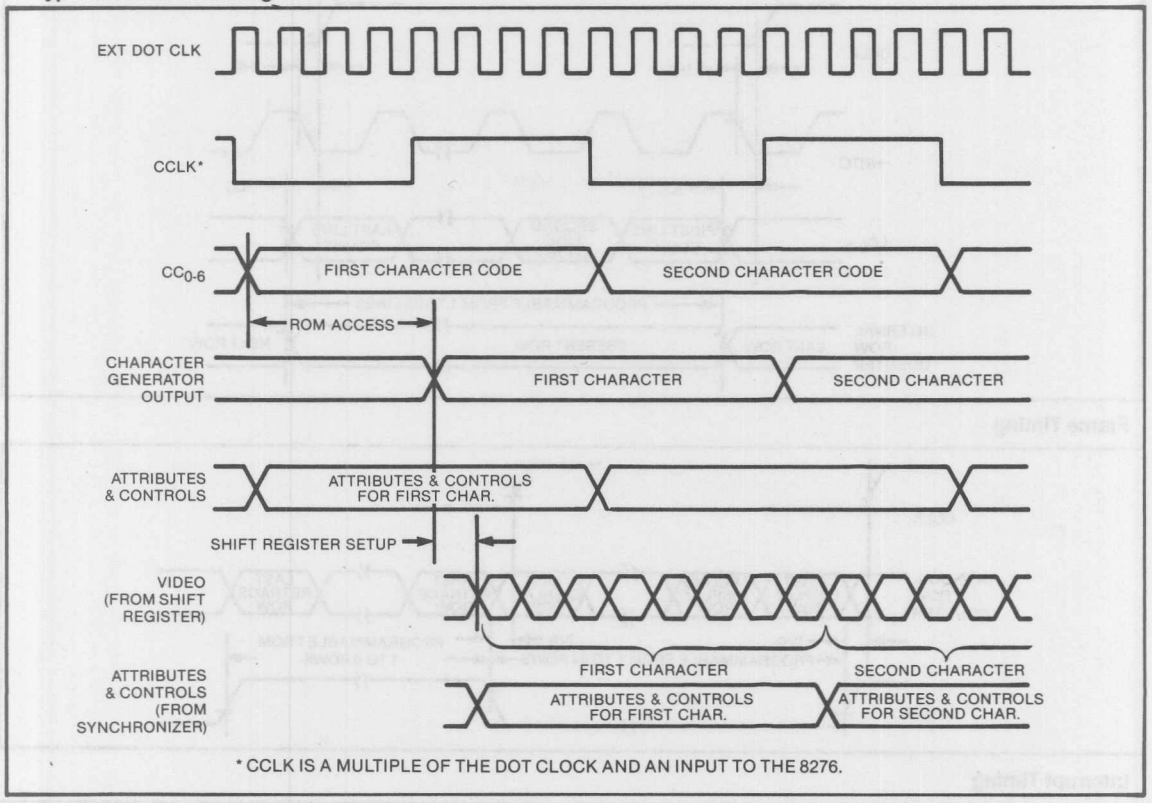
NOTE 1: AC timings measured at V_{OH} = 2.0, V_{OL} = 0.8, V_{IH} = 2.4 V_{IL} = 0.45.

Other Timing

SYMBOL	PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
t_{CC}	Character Code Output Delay		150	ns	C_L = 50 pF
t_{HR}	Horizontal Retrace Output Delay		200	ns	C_L = 50 pF
t_{LC}	Line Count Output Delay		400	ns	C_L = 50 pF
t_{AT}	Control/Attribute Output Delay		275	ns	C_L = 50 pF
t_{VR}	Vertical Retrace Output Delay		275	ns	C_L = 50 pF
t_{RI}	INT↓ from $\overline{RD}$↑		250	ns	C_L = 50 pF
t_{WQ}	BRDY↑ from $\overline{WR}$↑		250	ns	C_L = 50 pF
t_{RQ}	BRDY↓ from $\overline{WR}$↓		200	ns	C_L = 50 pF
t_{LR}	$\overline{BS}$↓ to $\overline{WR}$↓	0		ns	
t_{RL}	$\overline{WR}$↑ to $\overline{BS}$↑	0		ns	

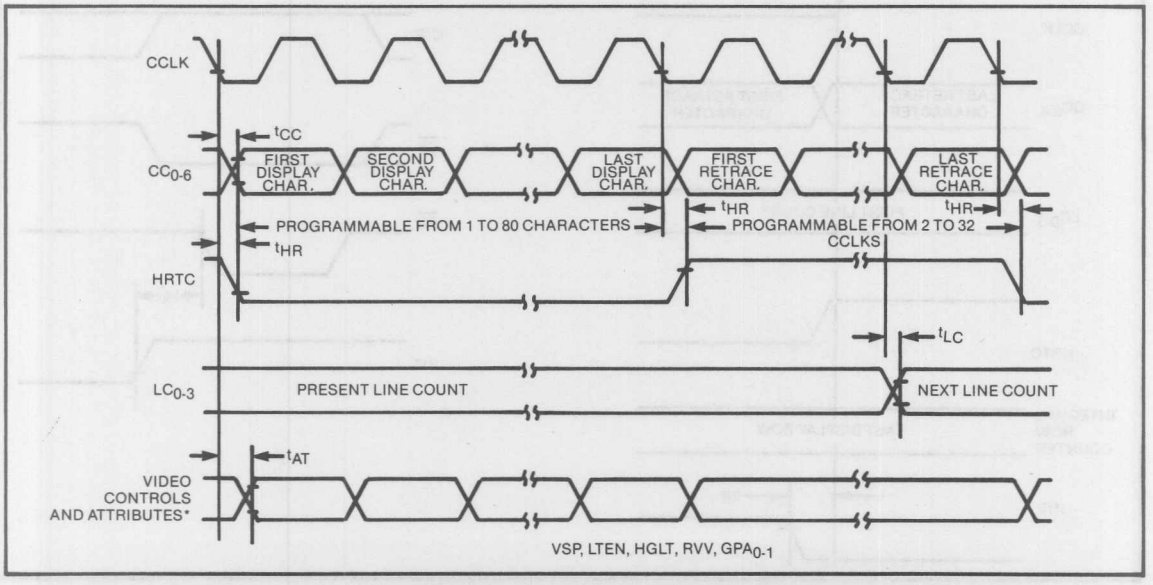
WAVEFORMS

Typical Dot Level Timing

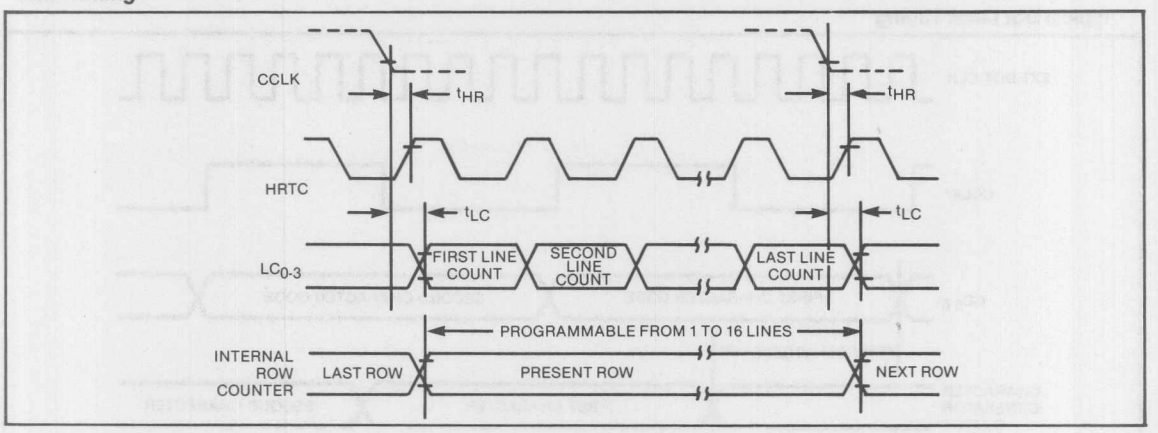


* CCLK IS A MULTIPLE OF THE DOT CLOCK AND AN INPUT TO THE 8276.

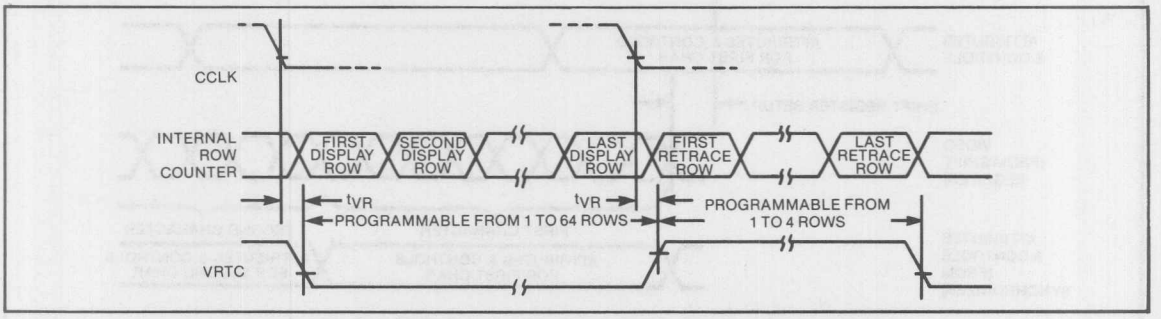
Line Timing



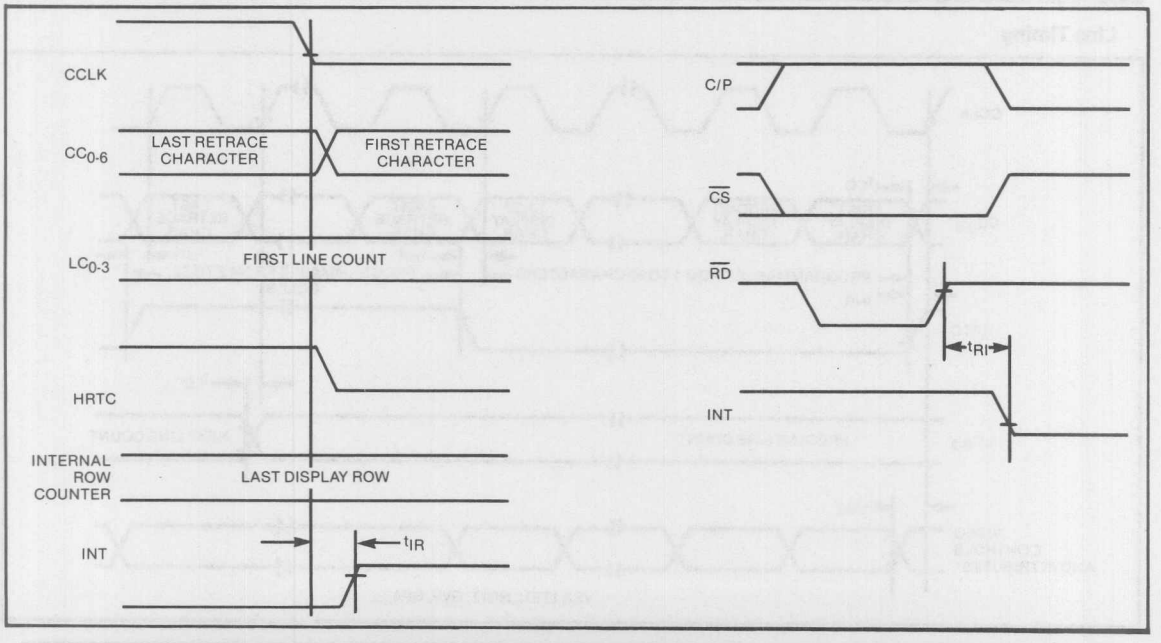
Row Timing



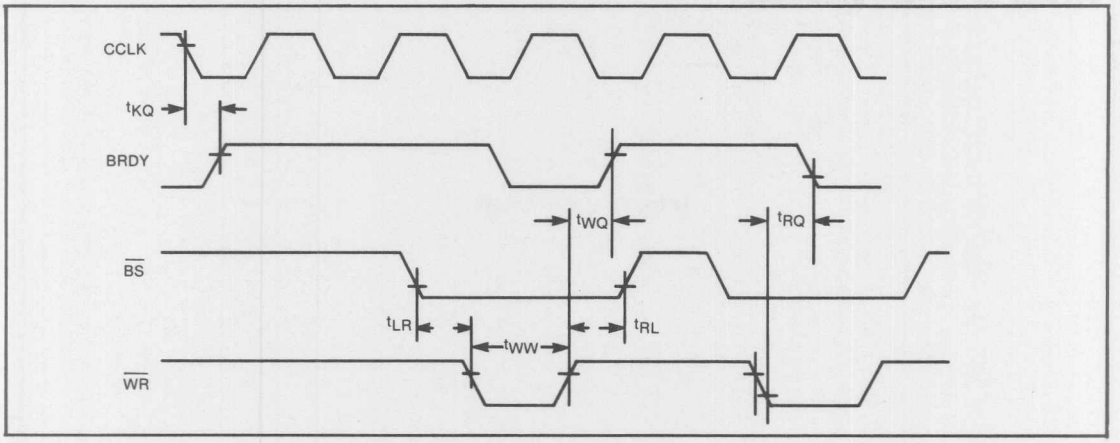
Frame Timing



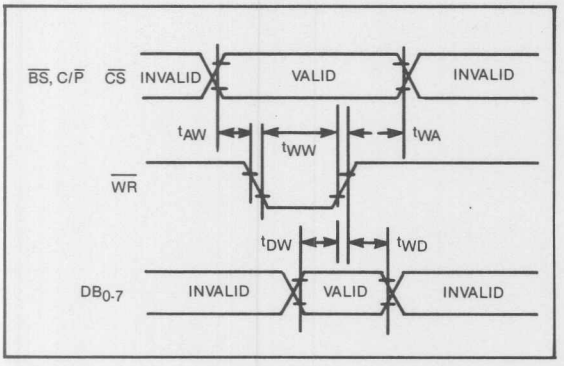
Interrupt Timing



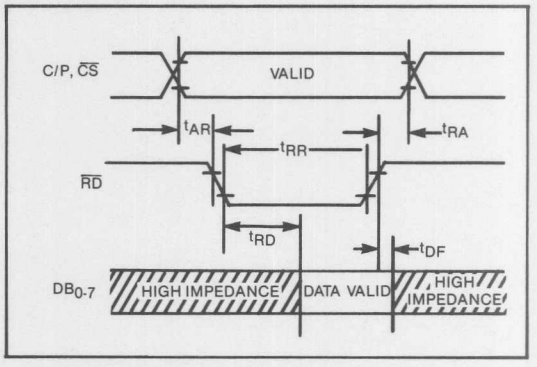
Timing for Buffer Loading



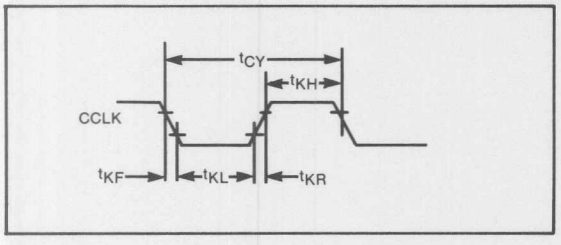
Write Timing



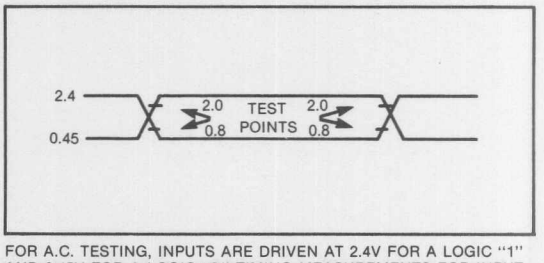
Read Timing



Clock Timing

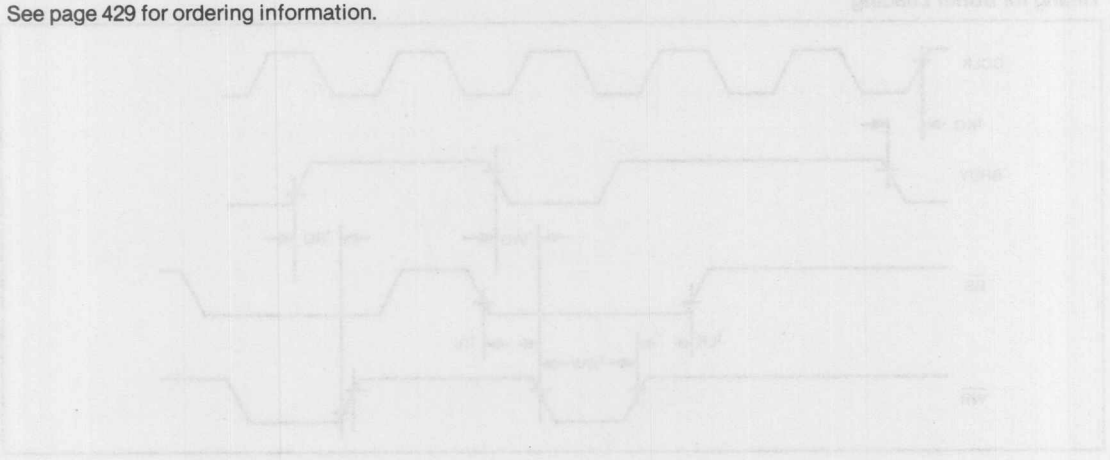


Input and Output Waveforms for A.C. Tests



FOR A.C. TESTING, INPUTS ARE DRIVEN AT 2.4V FOR A LOGIC "1" AND 0.45V FOR A LOGIC "0." TIMING MEASUREMENTS FOR INPUT AND OUTPUT SIGNALS ARE MADE AT 2.0V FOR A LOGIC "1" AND 0.8V FOR A LOGIC "0."

See page 429 for ordering information.



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WD9918/WD9928/WD9929 Video Display Processors

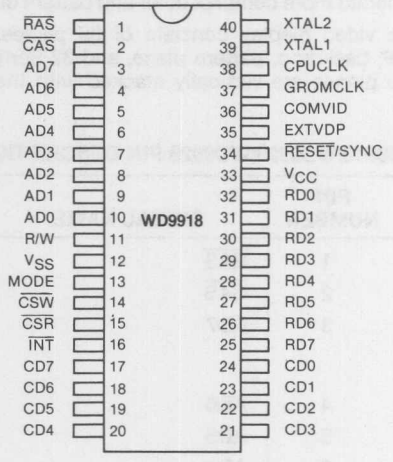
FEATURES

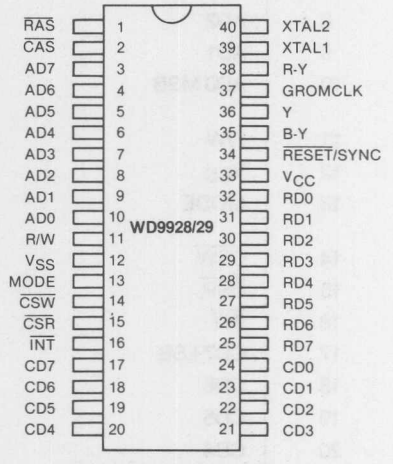
- SINGLE-CHIP SOLUTION FOR INTERFACING COLOR TVS [EXCLUDING RANDOM-ACCESS MEMORY (RAM) AND RADIO FREQUENCY (RF) MODULATOR (WD9918 ONLY)]
- 256 X 192 RESOLUTION ON TV SCREEN
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- AUTOMATIC AND TRANSPARENT REFRESH OF DYNAMIC RAMS
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- STANDARD 40-PIN PACKAGE
- COLOR DIFFERENCE OUTPUTS ALLOW RGB DRIVE — WD9928/WD9929
- SINGLE +5 VDC POWER SUPPLY

DESCRIPTION

The WD9918/9928/9929 video display processors (VDP) are N-channel MOS LSI devices used in video systems where data display on a raster-scanned home color television set or color monitor is desired. These devices generate all necessary video, control, and synchronization signals and also control the storage, retrieval, and refresh of display data in the dynamic screen refresh memory. The interfaces to the microprocessor, refresh memory, and the TV require a minimum of additional electronics for the WD9918.

The WD9928/9929 VDPs are functionally identical to the WD9918 except that the NTSC color encoding circuitry has been removed and replaced with luminance and color difference signals. The WD9918 is pin-for-pin compatible with the WD9928/9929, except for three pins, the composite video output, the external video input and the CPU clock output. These pins are replaced with the Black/White luminance and composite sync (Y) output and two color difference pins, Blue (B-Y) and Red (R-T) outputs, respectively. The color difference outputs allow the user to generate Red-Green-Blue (R-G-B) drive for direct color gun control, or composite video for use





PIN DESIGNATIONS

with NTSC or PAL video color monitor. However, to connect these three outputs to a R-G-B or monitor requires additional R-G-B or encoder circuitry.

The WD9918/9928 have a 525-line format for U.S. televisions while the WD9929 has a 625-line format for use with the European PAL system.

The VDP has four video display modes: Graphics I, Graphics II, Multicolor and Text mode. The Text mode provides twenty-four 40-character rows in two colors

and is intended to maximize the capacity of the TV screen to display alphanumeric character. The Multicolor mode provides an unrestricted 64 x 48 color-dot display employing 15 colors plus transparent. The Graphics I mode provides a 256 x 192 pixel display for generating pattern graphics in 15 colors plus transparent. The Graphics II mode is an enhancement of Graphics I mode, allowing it to generate more complex color and pattern displays.

The video display consists of 35 planes: external VDP, backdrop, pattern plane, and 32 Sprite Planes. The planes are vertically stacked with the external VDP being the bottom or innermost plane. The backdrop plane is the next plane followed by the pattern plane that contains Graphics I and Graphics II patterns with the 32 Sprite Planes as the top planes.

The WD9918/9928/9929 VDPs use either a 4K, 8K, or 16K-type low-cost dynamic memory for storage of the display parameters.

The WD9918, WD9928, and WD9929 interface identically to the host microprocessor making them software compatible. Thus, all references to VDP in this document apply to all three devices, except where noted.

WD9918/WD9928/WD9929 PIN DESCRIPTIONS

PIN NUMBER	SIGNAL NAME	I/O	DESCRIPTION
1	$\overline{RAS}$	O	VRAM row address strobe.
2	$\overline{CAS}$	O	VRAM column address strobe.
3	AD7	O	VRAM address/data bus (multiplexed high and low order VRAM address and output data bytes).†**
4	AD6	O	
5	AD5	O	
6	AD4	O	
7	AD3	O	
8	AD2	O	
9	AD1	O	
10	AD0 MSB	O	AD0 is the most significant bit and is used only for data and not for addressing.**
11	R/W	O	VRAM write strobe.
12	V_{SS}	I	Ground References.
13	MODE	I	CPU interface mode select; usually a processor address line.
14	$\overline{CSW}$	I	CPU-VDP write strobe
15	$\overline{CSR}$	I	CPU-VDP read strobe
16	$\overline{INT}$	O	CPU interrupt output.
17	CD7 LSB	I/O	
18	CD6	I/O	
19	CD5	I/O	
20	CD4	I/O	
21	CD3	I/O	
22	CD2	I/O	
23	CD1	I/O	
24	CD0 MSB	I/O	CPU data bus; (CD0) is the most significant bit.
25	RD7	I	
26	RD6	I	
27	RD5	I	
28	RD4	I	

WD9918/WD9928/WD9929 PIN DESCRIPTIONS (Continued)

PIN NUMBER	SIGNAL NAME	I/O	DESCRIPTION
29	RD3	I	
30	RD2	I	
31	RD1	I	
32	RD0 MSB	I	VRAM read data bus.
33	V_{CC}	I	+5 volt supply.
34	$\overline{\text{RESET}}$/SYNC	I	The $\overline{\text{RESET}}$ pin is a trilevel input pin. When it is below 0.8 volts, RESET initializes the VDP. When it is above 9 volts, RESET is the synchronizing input for external video.
35	B-Y (WD9928/9929)	I/O	On the WD9928/9929, this is the B-Y color difference output.
35	EXTVDP (WD9918)	I/O	On the WD9918, this is the external VDP input.
36	Y (WD9928/9929)	O	On the WD9928/9929, this is the Y (black/white luminance and composite sync) output.
36	COMVID (WD9918)	O	Composite video output for the WD9918.
37	GROMCLK	O	VDP output clock = XTAL/24 (usage is optional).
38	R-Y (WD9928/9929)	O	On the WD9928/9929, this is the R-Y color difference output.
38	CPUCLK (WD9918)	O	VDP color burst frequency clock (usage is optional).
40, 39	XTAL1, XTAL2	I	10.7 + MHz crystal inputs.*

* When driven externally, both inputs must be driven.

** The least significant address bit (AD7) is wired to A0 of the dynamic RAMs. Likewise, AD6 is wired to A1 of the RAMs.

† Care must be exercised in assuring proper orientation of the WD9918 address outputs to the dynamic RAM address inputs.

TYPICAL APPLICATIONS

- Color computer terminals
- Home computers
- Drafting/design aids
- Teaching aids
- Industrial process monitoring
- Home educational systems
- Animation aids
- European 625-line TV (WD9929 only)

The following example of a typical application may help introduce the user to the WD9918 VDP. Figure 1-1 is a block diagram of a typical application. Each of the concepts presented in the example is described more fully later in this data sheet.

The VDP basically has three interfaces: CPU, color monitor, and dynamic refresh RAM (VRAM), the contents of which define the TV image. The WD9918 also has eight write-only registers and a read-only status register.

The VDP communicates with the CPU via an 8-bit bidirectional data bus. Three control lines, decoded from the CPU address and enable lines, determine interpretation of the bus. Through the bus, the CPU can write to VRAM, read from VRAM, write to VDP registers, and read the VDP status. The VDP also generates an interrupt signal after every refresh of the TV display.

The dynamic RAM interface consists of direct wiring of eight 4K x 1, 8K x 1, or 16K x 1 dynamic RAS/CAS-type RAMs to the VDP. The amount of RAM required is dependent upon the features selected for use in the application.

The interface to the monitor can consist of either wiring the WD9918 composite video output pin (suitably buffered) to the input of a color or black-and-white monitor, or using an appropriate RF modulator to feed the signal into a TV antenna terminal. The WD9928/9929 require additional encoder circuitry to interface to a RGB or to a composite video monitor.

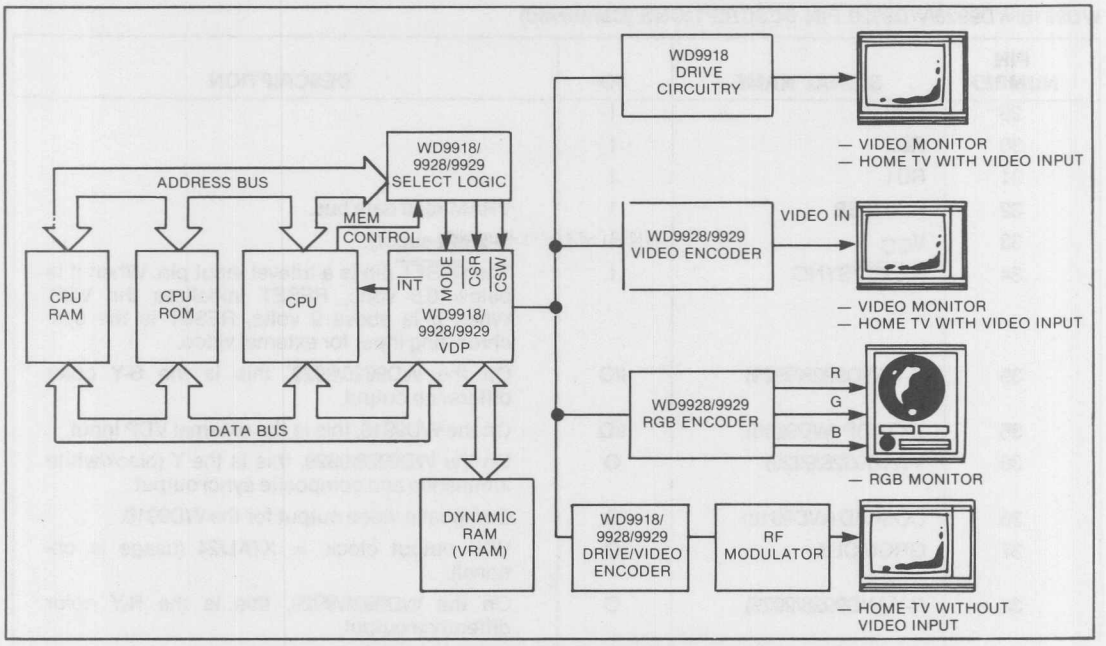


Figure 1. WD9918/28/29 SYSTEM BLOCK DIAGRAM

The VDP operates in four modes, and each one can affect the way the VRAM is mapped onto the television screen. In Graphics I and II modes, characters are mapped onto the screen in 8 x 8 pixel blocks, yielding 24 lines of 32 blocks (pattern positions) each. In Text mode, there are 24 lines of 40 blocks, each of which is 6 x 8 pixels. In Multicolor mode, there are 48 lines of 64 blocks, each of which is composed of 4 x 4 picture elements (pixels), all of one solid color. In addition to these, sprites can be superimposed onto the television image in Graphics I, II, and Multicolor mode. Furthermore, signals entering the WD9918 through the external VDP input can be used as a background to the WD9918.

ACRONYMS AND GLOSSARY

B-Y	Blue color difference output
COMVID (Composite Video)	Contains luminance, chrominance and all sync pulse necessary for horizontal and vertical timing
CAS	Column Address Strobe
CPU	Central Processor Unit
CSR	CPU from VDP read select
CSW	CPU to VDP write select
CPUCLK	XTAL — 3
GROMCLK	XTAL — 24
LSB	Least Significant Bit
LSI	Large Scale Integration
MOS	Metal Oxide Semiconductor
MHz	Megahertz
MSB	Most Significant Bit
NTSC	National Television Standards Committee which specifies television signal standards for the USA
PAL	Phase Alternating Line

Pixel	Picture Element — the smallest point on the TV screen that can be independently controlled
RAM	Random-Access Memory
RAS	Row-Address Strobe
RASTER	The area in which an image is reproduced
RF	Radio Frequency
R-G-B	Red-Green-Blue
ROM	Read-Only Memory
R/W	Read/Write
R-Y	Red color difference output
Sprite	An object whose pattern is relative to a specified X, Y coordinate and whose position can therefore be controlled by that coordinate with a positional resolution of one pixel
VDP	Video Display Processor
VRAM	Video RAM; refers to the dynamic RAMs that connect to the VDP and whose contents define the TV image
Y	Black/white luminance and composite sync

ARCHITECTURE

The WD9918 video display processor (VDP) is designed to provide a simple interface between a microprocessor and a raster-scanned color television. The WD9928/9929 VDPs are designed as a simple interface between a microprocessor, and R-G-B monitor or video encoder which produces the video for a video monitor. Figure 2 is a block diagram of the major portions of the VDP architecture interfaces to the VDP, CPU, VRAM, and color television.

CPU INTERFACE

The VDP interface to the CPU using an 8-bit bidirectional data bus, three control lines, and an interrupt is shown in Figure 3. Through this interface the CPU can conduct four operations:

1. Write data bytes to VRAM
2. Read data bytes from VRAM
3. Write to one of the eight VDP write-only registers
4. Read the VDP Status Register.

Each of these operations requires one or more data transfers to take place over the CPU/VDP data bus interface. The interpretation of the data transfer is determined by the three control lines of the VDP.

NOTE:
The CPU can communicate with the VDP simultaneously and asynchronously with the VDP's TV screen refresh operations. The VDP performs memory management and allows periodic intervals of CPU access to VRAM even in the middle of a raster scan.

CPU INTERFACE CONTROL SIGNALS

The type and direction of data transfers are controlled by the CSW, CSR, and MODE inputs. CSW is the CPU to VDP write select. When it is active (low), the eight bits on CD0-CD7 are strobed into the VDP. CSR is the CPU from VDP read select. When it is active (low), the VDP outputs eight bits on CD0-CD7 to the CPU. CSW and CSR should never be simultaneously low at the same time. If both are low, the VDP outputs data on CD0-CD7 and latches in invalid data.

MODE determines the source or destination of a read or write data transfer. MODE is normally tied to a CPU low order address line.

CPU WRITE TO VDP REGISTER

The VDP has eight write-only registers and one read-only status register. The write-only registers control the VDP operation and determine the way in which VRAM is allocated. The status register contains interrupt, sprite coincidence and fifth sprite status flags.

Each of the eight VDP write-only registers can be loaded using two 8-bit data transfers from the CPU. Table 1 describes the required format for the two bytes. The first byte transferred is the data byte, and the second byte transferred controls the destination. The MSB of the second byte must be a 1. The next four bits are 0s, and the lowest three bits make up the destination register number. The MODE input is high for both byte transfers.

To rewrite the data in an internal register after a byte of data has already been loaded, the status register must be read so that internal CPU interface logic is reinitialized and will accept the next byte as data and not as a register destination. This situation may be encountered in interrupt-driven program environments. Whenever the status of VDP write parameters is in question, this procedure should be used.

NOTE:
The CPU address is destroyed by writing to the VDP register.

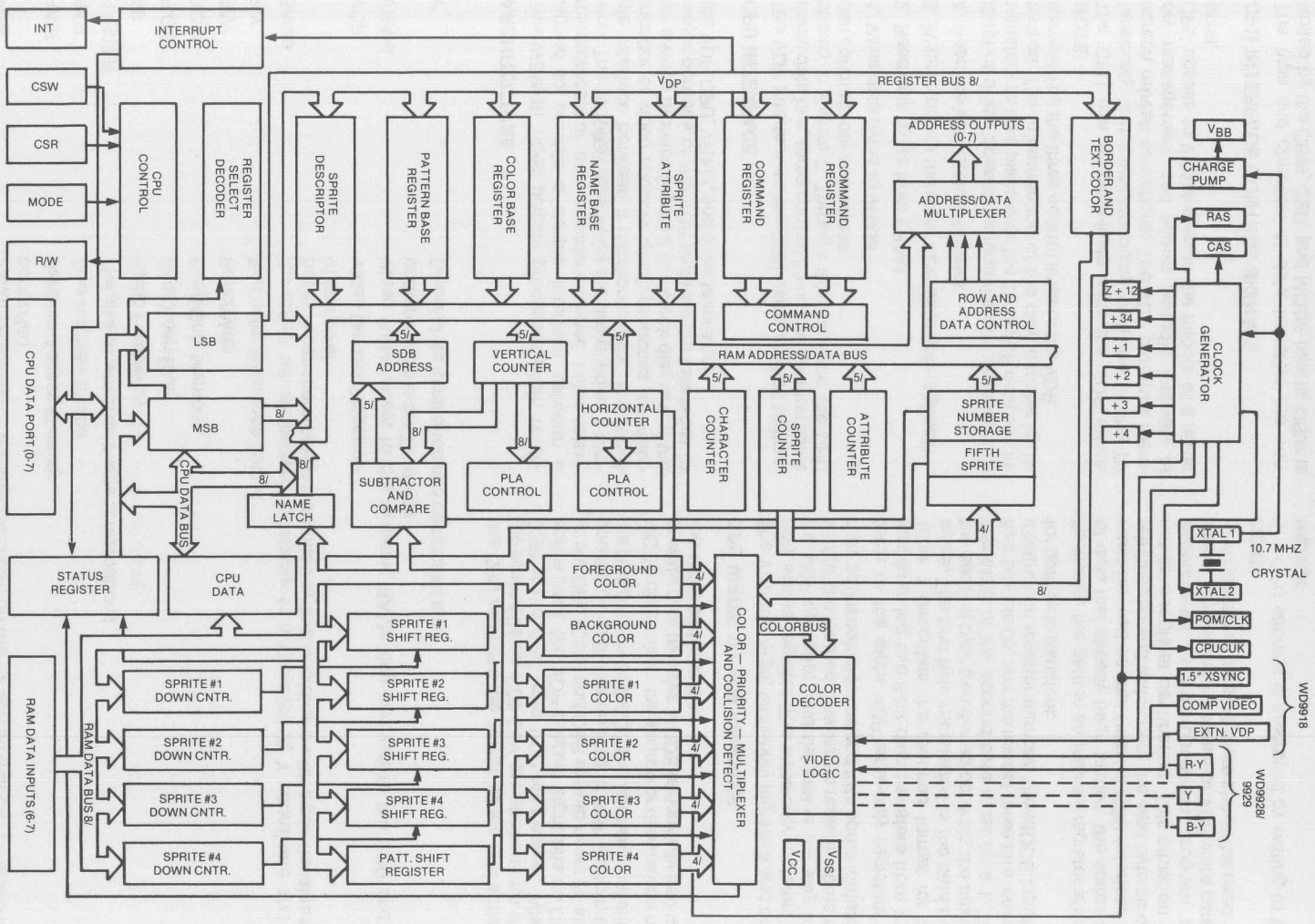


Figure 2. VDP BLOCK DIAGRAM

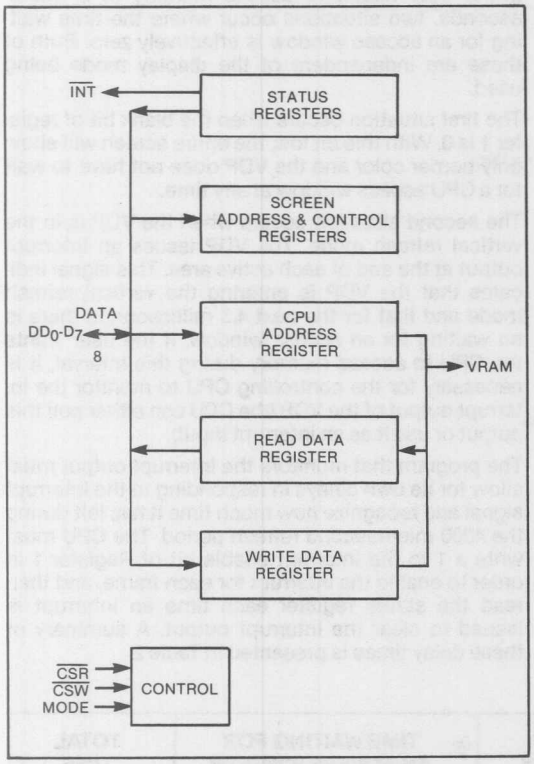


Figure 3. VDP TO CPU INTERFACE

CPU WRITE TO VRAM

The CPU transfers data to the VRAM through the VDP using a 14-bit autoincrementing address register. The address register setup requires 2-byte transfers. A 1-byte transfer is then required to write the data to the addressed VRAM byte. The address register is then autoincremented. Sequential VRAM writes require only 1-byte transfers since the address register is already set up. During setup of the address register, the two MSBs of the second address byte must be 0 and 1 respectively. MODE is high for both address transfers and low for the data transfer. CSW is used in all transfers to strobe the 8 bits into the VDP. See Table 1.

CPU READ FROM VDP STATUS REGISTER

The CPU can read the contents of the status register with a single-byte transfer. MODE is high for the transfer. CSR is used to signal the VDP that a read operation is required.

CPU READ FROM VRAM

The CPU reads from the VRAM through the VDP using the autoincrementing address register. A 1-byte transfer is then required to read the data from the addressed VRAM byte. The address register is then autoincremented. Sequential VRAM data reads require only a 1-byte transfer since the address register is already set up. During setup of the address register, the two MSBs of the second address byte must be 0. By setting up the address this way, a read cycle to VRAM is initiated and read data will be available for the first data transfer to the CPU. (See Table

Table 1. CPU/VDP DATA TRANSFERS

OPERATION	BIT 0	1	2	3	4	5	6	7	$\overline{CSW}$	$\overline{CSR}$	MODE
Write to VDP Register											
Byte 1 Data Write	D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7	0	1	1
Byte 2 Register Select	1	0	0	0	0	RS_0	RS_1	RS_2	0	1	1
Write to VRAM											
Byte 1 Address Setup	A_6	A_7	A_8	A_9	A_{10}	A_{11}	A_{12}	A_{13}	0	1	1
Byte 2 Address Setup	0	1	A_0	A_1	A_2	A_3	A_4	A_5	0	1	1
Byte 3 Data Write	D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7	0	1	0
Read from VDP Register											
Byte 1 Data Read	D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7	1	0	1
Read from VRAM											
Byte 1 Address Setup	A_6	A_7	A_8	A_9	A_{10}	A_{11}	A_{12}	A_{13}	0	1	1
Byte 2 Address Setup	0	0	A_0	A_1	A_2	A_3	A_4	A_5	0	1	1
Byte 3 Data Read	D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7	1	0	0

1). MODE is high for the address byte transfers and low for the data transfers. The VDP requires approximately 8 microseconds to fetch the VRAM byte following the last data transfer and 2 microseconds following address setup.

The CPU interacts with VRAM memory through the VDP. The amount of time necessary for the CPU to transfer a byte of data to or from VRAM memory can vary from 2 to 8 microseconds. Once the VDP has been told to read or write a byte of data to or from VRAM it takes approximately 2 microseconds until the VDP is ready to make the data transfer. In addition to this 2 microsecond delay, the VDP must wait for a CPU access window; i.e., the period of time when the VDP is not occupied with memory refresh or screen display and is available to read or write data.

The worst case time between windows occurs during the Graphics I or Graphics II mode when sprites are being used. During the active display, CPU windows occur once every 16 memory cycles giving a maximum delay of 6 microseconds (a memory cycle takes about 372 nanoseconds). In the Text mode the CPU windows occur at least once out of every three memory cycles or a worst case delay of about 1.1 microseconds. Finally, in the Multicolor mode, CPU windows occur at least once out of every four memory cycles.

If the user needs to access memory in 2 microseconds, two situations occur where the time waiting for an access window is effectively zero. Both of these are independent of the display mode being used.

The first situation occurs when the blank bit of register 1 is 0. With this bit low, the entire screen will show only border color and the VDP does not have to wait for a CPU access window at any time.

The second situation occurs when the VDP is in the vertical refresh mode. The VDP issues an interrupt output at the end of each active area. This signal indicates that the VDP is entering the vertical refresh mode and that for the next 4.3 milliseconds there is no waiting for an access window. If the user wants the CPU to access memory during this interval, it is necessary for the controlling CPU to monitor the interrupt output of the VDP (the CPU can either poll this output or use it as an interrupt input).

The program that monitors the interrupt output must allow for its own delays in responding to the interrupt signal and recognize how much time it has left during the 4300 microsecond refresh period. The CPU must write a 1 to the interrupt enable bit of Register 1 in order to enable the interrupt for each frame, and then read the status register each time an interrupt is issued to clear the interrupt output. A summary of these delay times is presented in Table 2.

Table 2. MEMORY ACCESS DELAY TIMES

CONDITION	MODE	VDP DELAY	TIME WAITING FOR AN ACCESS WINDOW	TOTAL TIME
Active Display Area	Text	2 μs	0 - 1.1 μs	2 - 3.1 μs
Active Display Area	Graphics I, II	2 μs	0 - 5.95 μs	2 - 8 μs
4300 μs after Vertical Interrupt Signal	All	2 μs	0 μs	2 μs
Register I Blank Bit 0	All	2 μs	0 μs	2 μs
Active Display Area	Multicolor	2 μs	0 - 1.5 μs	2 - 3.5 μs

VDP INTERRUPT

The VDP INT output pin is used to generate an interrupt at the end of each active-display scan, which is about every 1/60 second for the WD9918/9928 and 1/50 second for the WD9929. The INT output is active when the Interrupt Enable bit (IE) in VDP Register 1 is a 1 and the F bit of the status register is a 1. Interrupts are cleared when the status register is read.

VDP INITIALIZATION

The VDP is externally initialized whenever the RESET input is active (low) and must be held low for a minimum of 3 microseconds. The external reset synchronizes all clocks with its falling edge, sets the horizontal and vertical counters to known states, and clears VDP registers 0 and 1. The video display is automatically blanked since the BLANK bit in VDP register 1 becomes a 0. The VDP, however, continues to refresh the VRAM even though the display is blanked. While the RESET line is active, the VDP does not refresh the VRAM.

VIDEO DISPLAY MODES

The VDP displays an image on the screen that can best be envisioned as a set of display planes sandwiched together. Figure 4 shows the definition of each of the planes. Objects on planes closest to the viewer have higher priority. In cases where two entities on two different planes are occupying the same spot on the screen, the entity on the higher priority plane will show at that point. For an entity on a specific plane to show through, all planes in front of that plane must be transparent at that point. The first 32 planes (Figure 5) each may contain a single sprite.

The areas of the Sprite Planes, outside of the sprite itself, are transparent. Since the coordinates of the sprite are in terms of pixels, the sprite can be positioned and moved about very accurately. Sprites are available in three sizes: 8 x 8 pixels, 16 x 16 pixels, and 32 x 32 pixels.

Behind the Sprite Planes is the Pattern Plane. The Pattern Plane is used for textual and graphics images generated by the Text, Graphics I, Graphics II, or Multicolor modes. Behind the Pattern Plane is the backdrop, which is larger in area than the other planes so that it forms a border around the other planes. The last and lowest priority plane is the External VDP Plane. Its image is defined by the external VDP input pin which allows the WD9918 to mix the external video signal internal to the chip.

This mixing must occur outside of the chip for the WD9928 and WD9929. This is achieved through the color difference outputs swinging to a special level (sync level is shown in Figure 6) not used by the color difference signals in normal operation. This occurs when bit 7 of Register 0 is set high. External mixing circuitry is required to detect this change in the level of the color difference signals and then switch from the VDP signals to an external source's signals (see Figures 7 and 8).

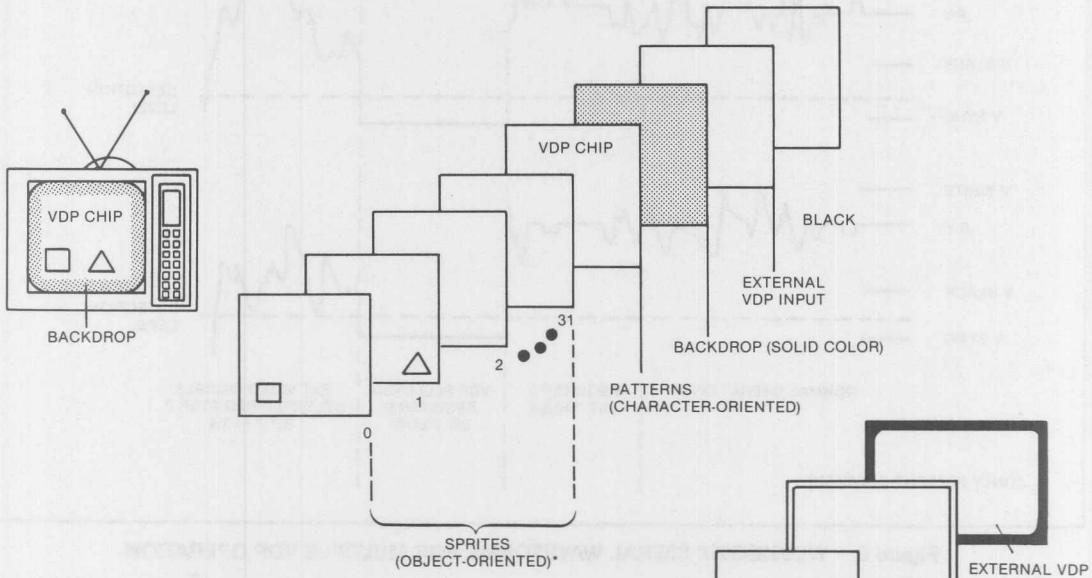


Figure 4. VDP DISPLAY PLANES (DEFINITION)

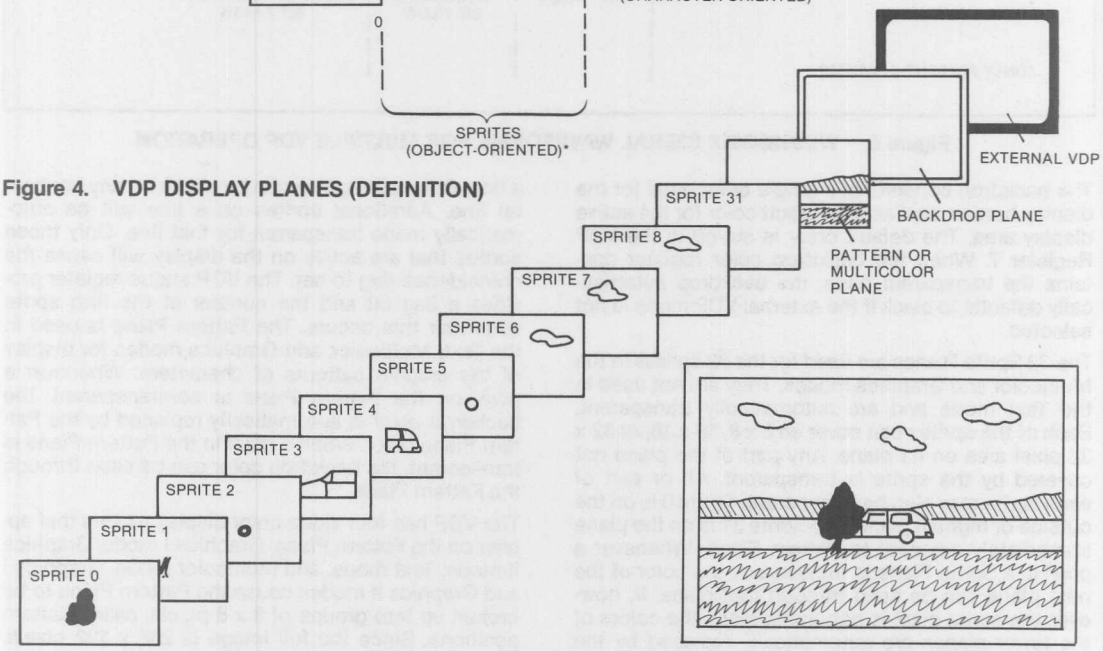


Figure 5. VDP DISPLAY PLANES (FIRST 32 PLANES)

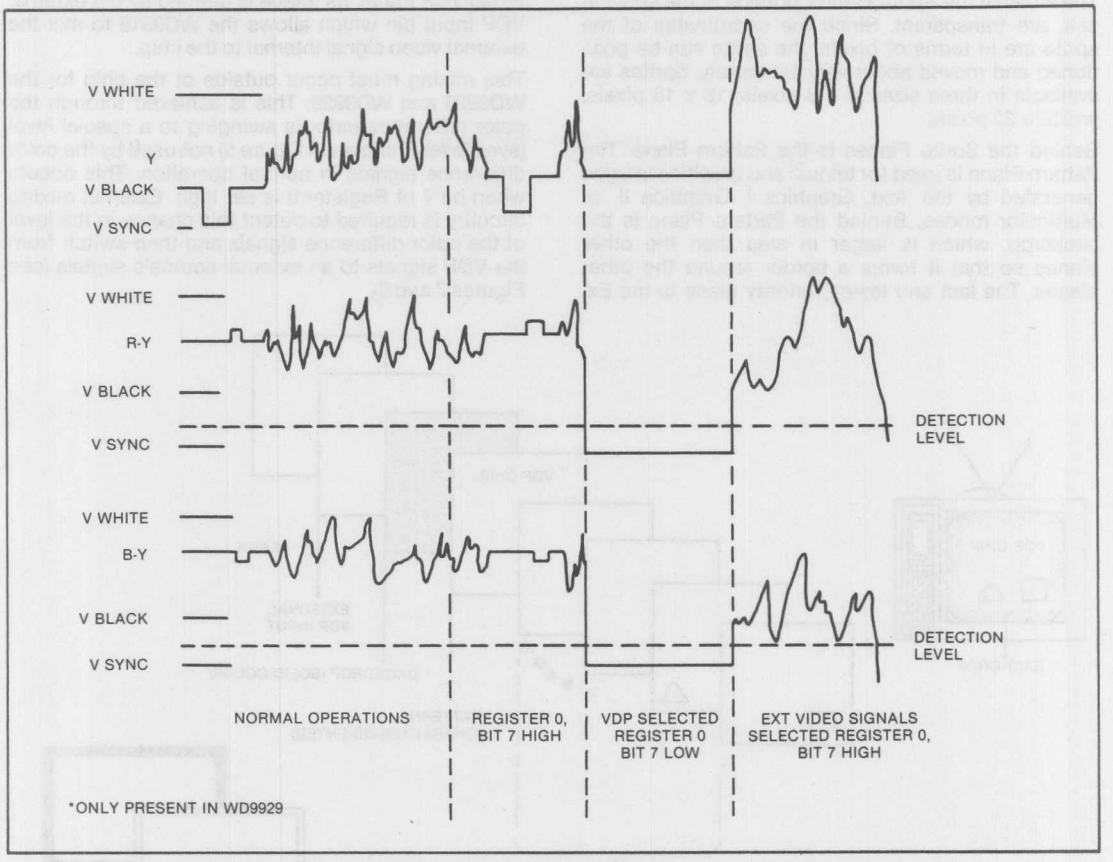


Figure 6. WD9928/9929 SIGNAL WAVEFORMS FOR MULTIPLE VDP OPERATION

The backdrop consists of a single color used for the display borders and as the default color for the active display area. The default color is stored in the VDP Register 7. When the backdrop color register contains the transparent code, the backdrop automatically defaults to black if the external VDP mode is not selected.

The 32 Sprite Planes are used for the 32 sprites in the Multicolor and Graphics modes. They are not used in the Text mode and are automatically transparent. Each of the sprites can cover an 8 x 8, 16 x 16, or 32 x 32 pixel area on its plane. Any part of the plane not covered by the sprite is transparent. All or part of each sprite may also be transparent. Sprite 0 is on the outside or highest plane, and sprite 31 is on the plane immediately adjacent to Pattern Plane. Whenever a pixel in a Sprite Plane is transparent, the color of the next plane can be seen through that plane. If, however, the sprite pixel is non-transparent, the colors of the lower planes are automatically replaced by the sprite color.

There is also a restriction on the number of sprites on a line. Only four sprites can be active on any horizontal line. Additional sprites on a line will be automatically made transparent for that line. Only those sprites that are active on the display will cause the coincidence flag to set. The VDP status register provides a flag bit and the number of the fifth sprite whenever this occurs. The Pattern Plane is used in the Text, Multicolor, and Graphics modes for display of the graphic patterns of characters. Whenever a pixel on the Pattern Plane is nontransparent, the backdrop color is automatically replaced by the Pattern Plane color. When a pixel in the Pattern Plane is transparent, the backdrop color can be seen through the Pattern Plane.

The VDP has four video color display modes that appear on the Pattern Plane: Graphics I mode, Graphics II mode, Text mode, and Multicolor mode. Graphics I and Graphics II modes cause the Pattern Plane to be broken up into groups of 8 x 8 pixels, called pattern positions. Since the full image is 256 x 192 pixels, there are 32 x 24 pattern positions on the screen in the Graphics modes.

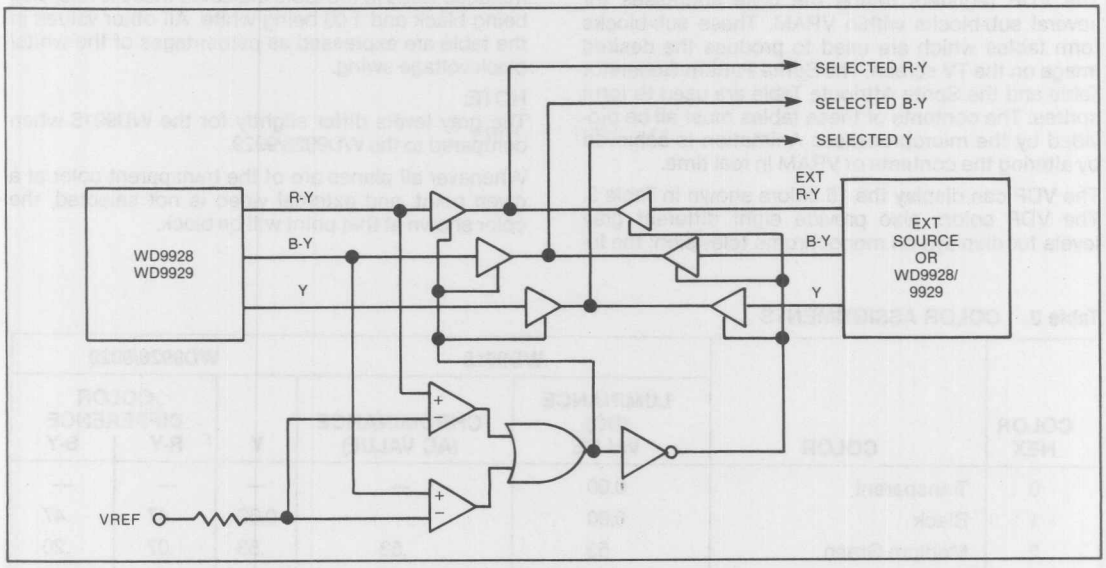


Figure 7.
USING COLOR DIFFERENCE SIGNALS TO MIX EXTERNAL COLOR DIFFERENCE TYPE SOURCE

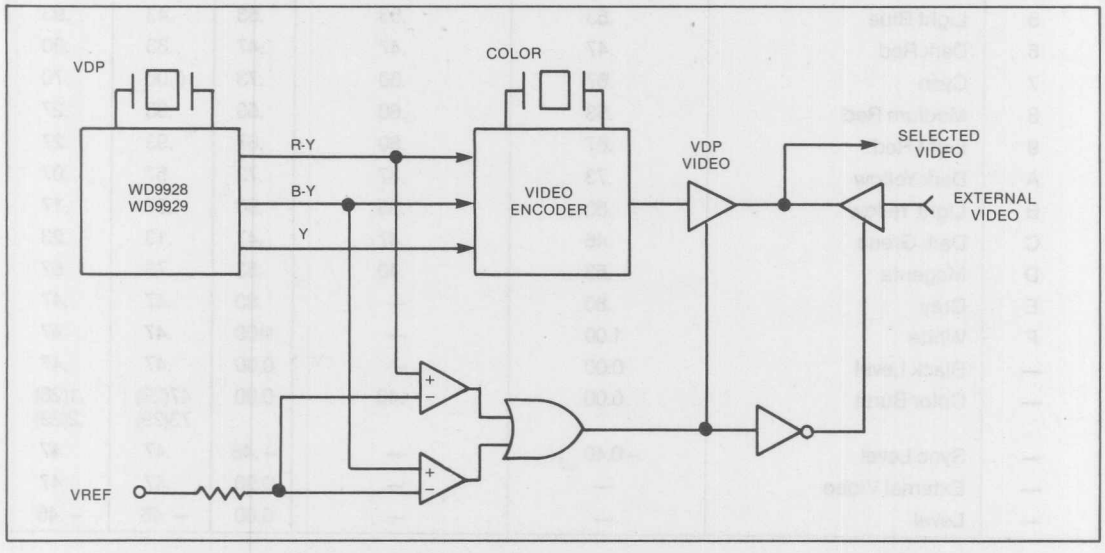


Figure 8. USING COLOR DIFFERENCE SIGNALS TO MIX EXTERNAL VIDEO SOURCES

In Graphics I mode, 256 possible patterns may be defined for the 768 pattern positions with two unique colors allowed for each line of a pattern definition. Thus, all 15 colors plus transparent may be used in a single pattern position.

In Text mode, the Pattern Plane is broken into groups of 6 x 8 pixels, called text positions. There are 40 x 24 text positions on the screen in this mode. In Text mode, sprites do not appear on the screen and two colors are defined for the entire screen by VDP Register 7.

In Multicolor mode, the screen is broken into a grid of 64 x 48 positions, each of which is a 4 x 4 pixel. Within each position, one unique color is allowed.

The VDP registers define the base addresses for several sub-blocks within VRAM. These sub-blocks form tables which are used to produce the desired image on the TV screen. The Sprite Pattern Generator Table and the Sprite Attribute Table are used to form sprites. The contents of these tables must all be provided by the microprocessor. Animation is achieved by altering the contents of VRAM in real time.

The VDP can display the 15 colors shown in Table 3. The VDP colors also provide eight different gray levels for displays on monochrome television; the luminance value in the table indicates these levels, 0.00 being black and 1.00 being white. All other values in the table are expressed as percentages of the white/black voltage swing.

NOTE:
The gray levels differ slightly for the WD9918 when compared to the WD9928/9929.

Whenever all planes are of the transparent color at a given point, and external video is not selected, the color shown at that point will be black.

Table 3. COLOR ASSIGNMENTS

COLOR HEX	COLOR	WD9918		WD9928/9929		
		LUMINANCE (DC) VALUE	CHROMINANCE (AC VALUE)	Y	COLOR DIFFERENCE R-Y	B-Y
0	Transparent	0.00	—	—	—	—
1	Black	0.00	—	0.00	.47	.47
2	Medium Green	.53	.53	.53	.07	.20
3	Light Green	.67	.40	.67	.17	.27
4	Dark Blue	.40	60	.40	.4	1.00
5	Light Blue	.53	.53	.53	.43	.93
6	Dark Red	.47	.47	.47	.83	.30
7	Cyan	.67	.60	.73	0.00	.70
8	Medium Red	.53	.60	.53	.93	.27
9	Light Red	.67	.60	.67	.93	.27
A	Dark Yellow	.73	.47	.73	.57	.07
B	Light Yellow	.80	.33	.80	.57	.17
C	Dark Green	.46	.47	.47	.13	.23
D	Magenta	.53	.40	.53	.73	.67
E	Gray	.80	—	.80	.47	.47
F	White	1.00	—	1.00	.47	.47
—	Black Level	0.00	—	0.00	.47	.47
—	Color Burst	0.00	.40	0.00	47(28) 73(29)	.1(28) .2(29)
—	Sync Level	– 0.40	—	– .46	.47	.47
—	External Video	—	—	0.00	.47	.47
—	Level	—	—	0.00	– .46	– .46

GRAPHICS I MODE

The VDP is in Graphics I mode when M1, M2, and M3 bits in VDP registers 1 and 0 are zero. When in this mode the Pattern Plane is divided into a grid of 32 columns by 24 rows of pattern positions as shown in Figure 9. Each of the pattern positions contains 8 x 8 pixel. The tables in VRAM used to generate the Pattern Plane are the Pattern Generator, Name, and Color Tables which require 2848 VRAM bytes. Figure 10 illustrates the mapping of these tables into the Pattern Plane. Less memory is required if all 256 possible pattern definitions are not required. The tables can be overlapped to reduce the amount of VRAM needed for pattern generation. Examples of VRAM memory allocation are provided in VRAM ADDRESSING EXAMPLE.

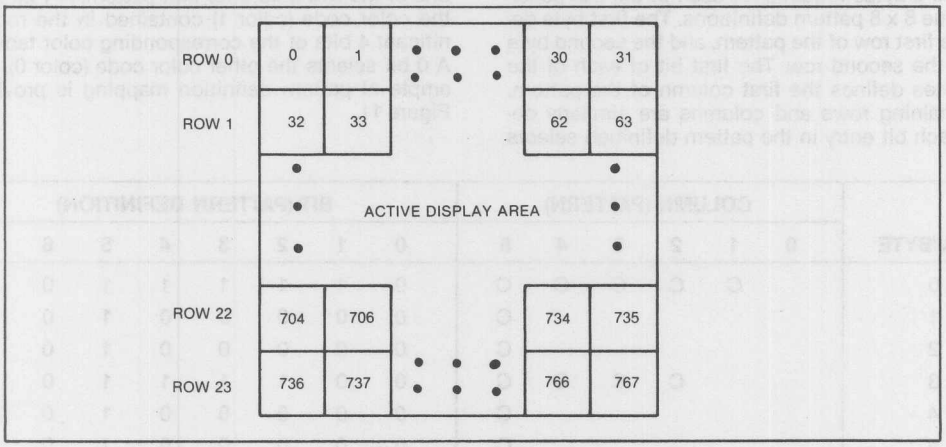


Figure 9. PATTERN GRAPHICS NAME TABLE MAPPING

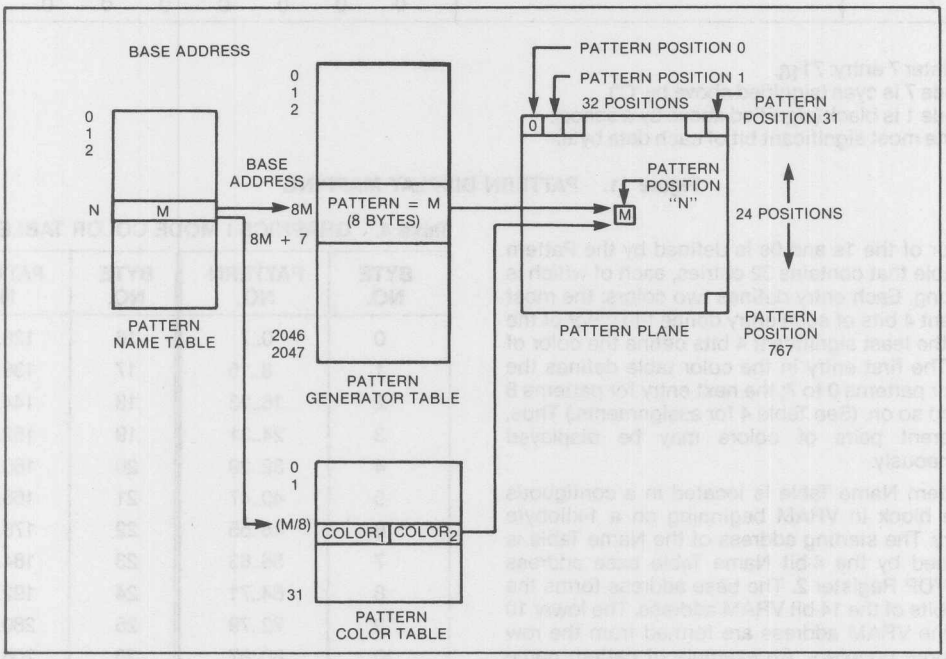


Figure 10. GRAPHICS I MODE MAPPING

The Pattern Generator Table contains a library of patterns that can be displayed in the pattern positions. It is 2048 bytes long and is arranged into 256 patterns, each of which is 8 bytes long, yielding 8 x 8 bits. All of the 1s in the 8-byte pattern can designate one color (color 1), while all the 0s can designate another color (color 0).

The full 8-bit pattern name is used to select one of the 256 pattern definitions in the Pattern Generator Table. The table is a 2048-byte block in VRAM beginning on a 2-kilobyte boundary. The starting address of the table is determined by the generator base address in VDP Register 4. The base address forms the three MSBs of the 14-bit VRAM address for each Pattern Generator Table entry. The next 8 bits indicate the 8-bit name of the selected pattern definition. The lowest 3 bits of the VRAM address indicate the row number within the pattern definition.

There are 8 bytes required for each of the 256 possible unique 8 x 8 pattern definitions. The first byte defines the first row of the pattern, and the second byte defines the second row. The first bit of each of the eight bytes defines the first column of the pattern. The remaining rows and columns are similarly defined. Each bit entry in the pattern definition selects one of the two colors for that pattern. A 1 bit selects the color code (color 1) contained in the most significant 4 bits of the corresponding color table byte. A 0 bit selects the other color code (color 0). An example of pattern definition mapping is provided in Figure 11.

	COLUMN (PATTERN)						BIT (PATTERN DEFINITION)							
ROW/BYTE	0	1	2	3	4	5	0	1	2	3	4	5	6	7
0		C	C	C	C	C	0	1	1	1	1	1	0	0
1						C	0	0	0	0	0	1	0	0
2						C	0	0	0	0	0	1	0	0
3			C	C	C	C	0	0	1	1	1	1	0	0
4						C	0	0	0	0	0	1	0	0
5						C	0	0	0	0	0	1	0	0
6		C	C	C	C	C	0	1	1	1	1	1	0	0
7							0	0	0	0	0	0	0	0

NOTES:
VDP register 7 entry: 71_{16}.
Color code 7 is cyan (signified above by 'C').
Color code 1 is black (signified above by a space).
Bit 0 is the most significant bit of each data byte.

Figure 11. PATTERN DISPLAY MAPPING

The color of the 1s and 0s is defined by the Pattern Color Table that contains 32 entries, each of which is 1 byte long. Each entry defines two colors: the most significant 4 bits of each entry define the color of the 1s, and the least significant 4 bits define the color of the 0s. The first entry in the color table defines the colors for patterns 0 to 7; the next entry for patterns 8 to 15, and so on. (See Table 4 for assignments.) Thus, 32 different pairs of colors may be displayed simultaneously.

The Pattern Name Table is located in a contiguous 768-byte block in VRAM beginning on a 1-kilobyte boundary. The starting address of the Name Table is determined by the 4-bit Name Table base address field in VDP Register 2. The base address forms the upper 4 bits of the 14-bit VRAM address. The lower 10 bits of the VRAM address are formed from the row and column counters. An example of pattern name table addressing is given in VRAM ADDRESSING EXAMPLE.

Each byte entry in the Name Table is either the name of or the pointer to a pattern definition in the Pattern Generator Table. The upper 5 bits of the 8-bit name identify the color group of the pattern. There are 32 groups of 8 patterns. The same two colors are used for all eight patterns in a group; the color codes are stored in the VDP Color Table. The Color Table is located in a 32-byte clock in VRAM beginning on a 64-byte boundary. The table starting address is determined by the 8-bit Color Table base address in VDP Register 3. The base address forms the upper 8 bits

Table 4. GRAPHICS I MODE COLOR TABLE

BYTE NO.	PATTERN NO.	BYTE NO.	PATTERN NO.
0	0..7	16	128..135
1	8..15	17	136..143
2	16..23	18	144..151
3	24..31	19	152..159
4	32..39	20	160..167
5	40..47	21	168..175
6	48..55	22	176..183
7	56..63	23	184..191
8	64..71	24	192..199
9	72..79	25	280..207
10	80..87	26	208..215
11	88..95	27	216..223
12	96..103	28	224..231
13	104..111	29	232..239
14	112..119	30	240..247
15	120..127	31	248..255

of the 14-bit Color Table entry VRAM address. The next bit is a 0 and the lowest 5 bits are equal to the upper 5 bits of the corresponding Name Table entries.

Since the tables in VRAM have their base addresses defined by the VDP registers, a complete switch of the values in the tables can be made by simply changing the values in the VDP registers. This is especially useful when one wishes to time-slice between two or more screens of graphics.

When the Pattern Generator Table is loaded with a pattern set, manipulation of the Pattern Name Table contents can change the appearance of the screen. Alternatively, a dynamically changing set of patterns throughout the course of a graphics session is easily accomplished since all tables are in VRAM. A total of 2848 VRAM bytes are required for the Pattern, Name, Color and Generator tables. Less memory is needed if all 256 possible pattern definitions are not required; the tables can be overlapped to reduce the amount of VRAM needed for pattern generation. Examples of VRAM memory allocation are provided in VRAM ADDRESSING EXAMPLE.

Graphics II Mode

The VDP is in the Graphics II mode bits (M1 = 0, M2 = 0 and M3 = 1). The Graphics II mode is similar to Graphics I mode except it allows a larger library of patterns so that a unique pattern generator entry may be made for each of the 768 (32 x 24) pattern positions on the video screen. Additionally, more color information is included in each 8 x 8 graphics pattern. Thuus, two unique colors may be specified for each byte of the 8 x 8 pattern. A larger amount of VRAM (12 kilobytes) is required to implement the full usage of the Graphics II mode.

Like Graphics I mode, the Graphics II mode Pattern Name Table contains 768 entries which correspond to the 768 pattern positions on the display screen. Because the Graphics I mode pattern names are only 8 bits in length, a maximum of 256 pattern definitions may be addressed using the addressing scheme discussed in VRAM ADDRESSING EXAMPLE. Graphics II mode, however, segments the display screen into three equal parts of 256 pattern positions each and also segments the Pattern Generator Table into three

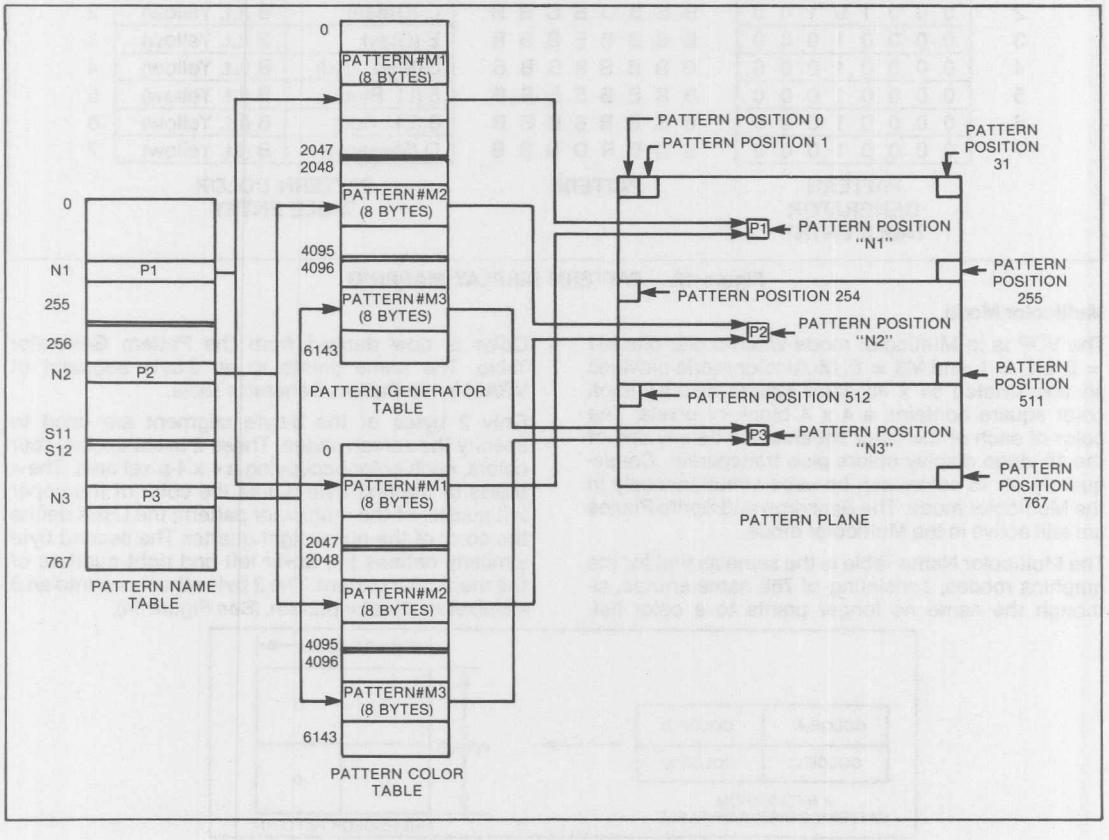


Figure 12. GRAPHICS II MODE MAPPING

equal blocks of 2048 bytes each. Pattern definitions in the first third of the display screen correspond to pattern positions in the upper third. Likewise, pattern definitions in the second and third blocks of the Pattern Generator Table correspond to the second and third areas of the Pattern Plane.

The Pattern Name Table is also segmented into three blocks of 256 names each so that names found in the upper third reference pattern definitions are found in the upper 2048 bytes in Pattern Generator Table. Similarly, the second and third blocks reference pattern definitions in the second 2048-byte block and third-2048 byte block, respectively. Thus, if 768 patterns are uniquely specified, an 8-bit pattern name will be used three times, once in each segment of the Pattern Name Table. The Pattern Generator Table falls on 8-kilobyte boundaries and may be located in the upper or lower half of 16K memory based on the MSB of the pattern generator base in VDP Register 4. The LSBs must be set to all 1s.

The Color Table is also 6144 bytes long and is segmented into three equal blocks of 2048 bytes. Each entry in the Pattern Color Table is 8 bytes which provides the capability to uniquely specify color 1 and color 0 for each of the 8 bytes of the corresponding pattern definition. The addressing scheme is exactly like that of the Pattern Generator Table except for the location of the table in VRAM. This is controlled by the loading of the MSB of the color base in VDP Register 3. The LSBs must be set to all 1s.

Figure 12 illustrates the Graphics II mode mapping scheme. Note that pattern names, P1, P2, and P3, correspond to pattern generator entries in the three blocks of the Pattern Generator Table. Note also how these three names map to the display screen. Figure 13 is an example of a Pattern Generator and Pattern Color Table entry.

ROW	PATTERN GENERATOR TABLE ENTRY	PATTERN	PATTERN COLOR TABLE ENTRY (0 … 3 / 4 … 7)	ROW
0	0 1 0 0 0 0 0 1	B 1 B B B B B 1	1 (Black) / B (Lt. Yellow)	0
1	0 0 1 0 0 0 1 0	B B 7 B B B 7 B	7 (Cyan) / B (Lt. Yellow)	1
2	0 0 0 1 0 1 0 0	B B B C B C B B	C (Green) / B (Lt. Yellow)	2
3	0 0 0 0 1 0 0 0	B B B B E B B B	E (Gray) / B (Lt. Yellow)	3
4	0 0 0 0 1 0 0 0	B B B B 8 B B B	8 (Med. Red) / B (Lt. Yellow)	4
5	0 0 0 0 1 0 0 0	B B B B 5 B B B	5 (Lt. Blue) / B (Lt. Yellow)	5
6	0 0 0 0 1 0 0 0	B B B B 6 B B B	6 (Dk. Red) / B (Lt. Yellow)	6
7	0 0 0 0 1 0 0 0	B B B B D B B B	D (Magenta) / B (Lt. Yellow)	7

Figure 13. PATTERN DISPLAY MAPPING

Multicolor Mode

The VDP is in Multicolor mode when mode bits M1 = 0, M2 = 1, and M3 = 0. Multicolor mode provides an unrestricted 64 x 48 color square display. Each color square contains a 4 x 4 block of pixels. The color of each of the color squares can be any one of the 15 video display colors plus transparent. Consequently, all 15 colors can be used simultaneously in the Multicolor mode. The Backdrop and Sprite Planes are still active in the Multicolor mode.

The Multicolor Name Table is the same as that for the graphics modes, consisting of 768 name entries, although the name no longer points to a color list. Color is now derived from the Pattern Generator Table. The name points to an 8-byte segment of VRAM in the Pattern Generator Table.

Only 2 bytes of the 8-byte segment are used to specify the screen image. These 2 bytes specify four colors, each color occupying a 4 x 4-pixel area. The 4 MSBs of the first byte define the color of the upper left quarter of the multicolor pattern; the LSBs define the color of the upper right quarter. The second byte similarly defines the lower left and right quarters of the multicolor pattern. The 2 bytes thus map into an 8 x 8-pixel multicolor pattern. (See Figure 14).

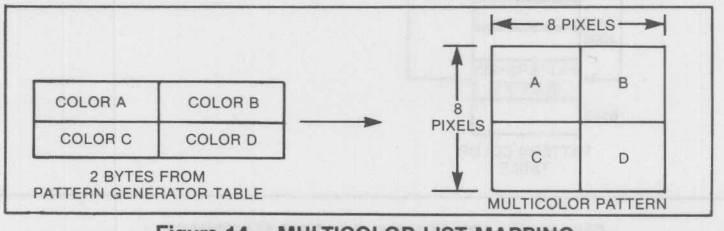


Figure 14. MULTICOLOR LIST MAPPING

The location of the 2 bytes within the 8-byte segment pointed to by the name is dependent upon the screen position where the name is mapped. For names in the top row (names 0-31), the 2 bytes are the first two within the groups of 8-byte segments pointed to by the names. The next row of names (32-63) uses the bytes 3 and 4 within the 8-byte segments. The next row of names uses bytes 5 and 6 while the last row of names uses bytes 7 and 8. This series repeats for the remainder of the screen.

For example, referring to Figure 15 if Name Table entry 0 (pattern position 0) multicolor block #N (name = N), the multicolor pattern displayed will be an 8 x 8-pixel block consisting of colors A, B, C, and D which comprise the first two bytes of the Multicolor Table. If, however, name #N is located in Name Table entry 33, (Pattern position 33), the colors displayed will be colors E, F, G, and H as specified by bytes 3 and 4 of the multicolor block pointed to by the name.

Likewise, pattern positions which lie in rows 2 and 3 would cause colors, I, J, K, L and colors M, N, O, P, respectively, to be displayed. Thus, it can be seen that the color displayed from the multicolor generator block is dependent upon pattern position on the screen. Figure 16 illustrates the Multicolor mode mapping scheme.

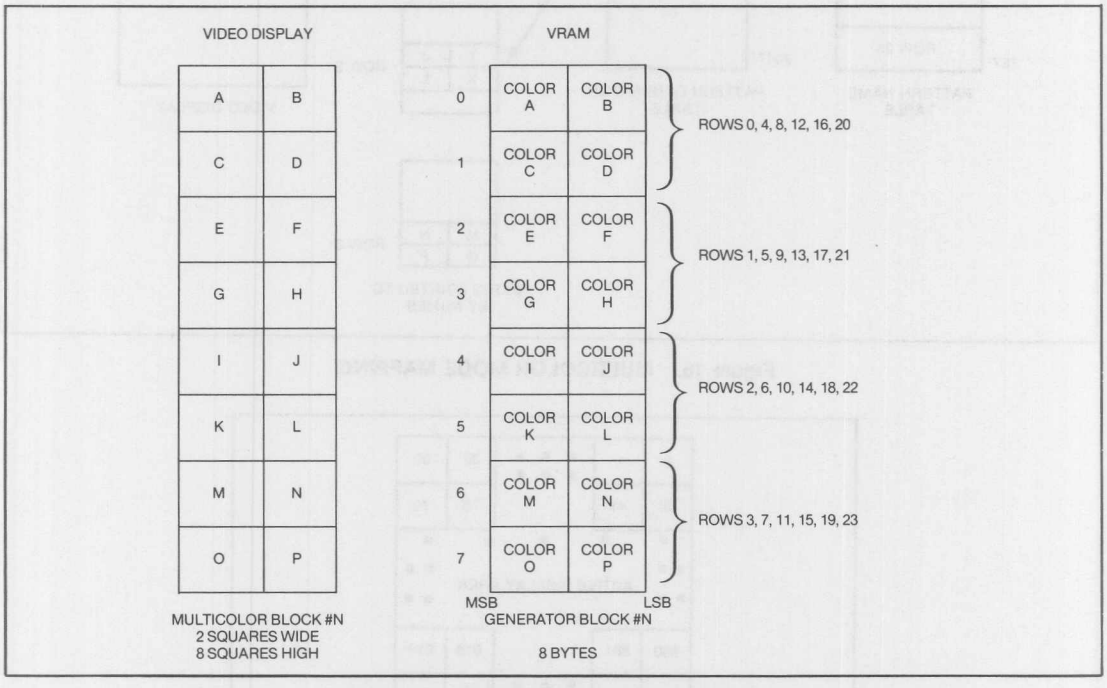


Figure 15. MULTICOLOR BLOCK DISPLAY

The mapping of VRAM contents to screen image is simplified by using duplicate names in the Name Table since the series of bytes used within the 8-byte segment specifies a 2 x 8 color square pattern on the screen as a straightforward translation from the 8-byte segment in VRAM pointed to by the common name.

When used in this manner, 768 bytes are still used for the Name Table and 1536 bytes are used for the color information in the Pattern Generator Table (24 rows x 32 columns x 8 bytes/pattern position). Thus, a total of 1728 bytes in VRAM are required. It should be noted that the tables begin on even 1K and 2K boundaries and are therefore not contiguous. An example of multicolor VRAM memory allocation is given in VRAM ADDRESSING EXAMPLE.

Text Mode

The VDP is in Text mode when mode bits M1 = 1, M2 = 0, and M3 = 0. In this mode, the screen is divided into a grid of 40 text positions across and 24 down. (See Figure 17). Each of the text positions contains 6 pixels across and 8 pixels down. The tables used to generate the Pattern Plane are the Pattern Name Table and the Pattern Generator Table. There can be up to 256 unique patterns defined at any time. The pattern definitions are stored in the Pattern Generator Table in VRAM and can be dynamically changed. The VRAM contains a Pattern Name Table which maps the pattern definition into each of the 960 pattern cells on the Pattern Plane (Figure 18). Sprites are not available in Text mode.

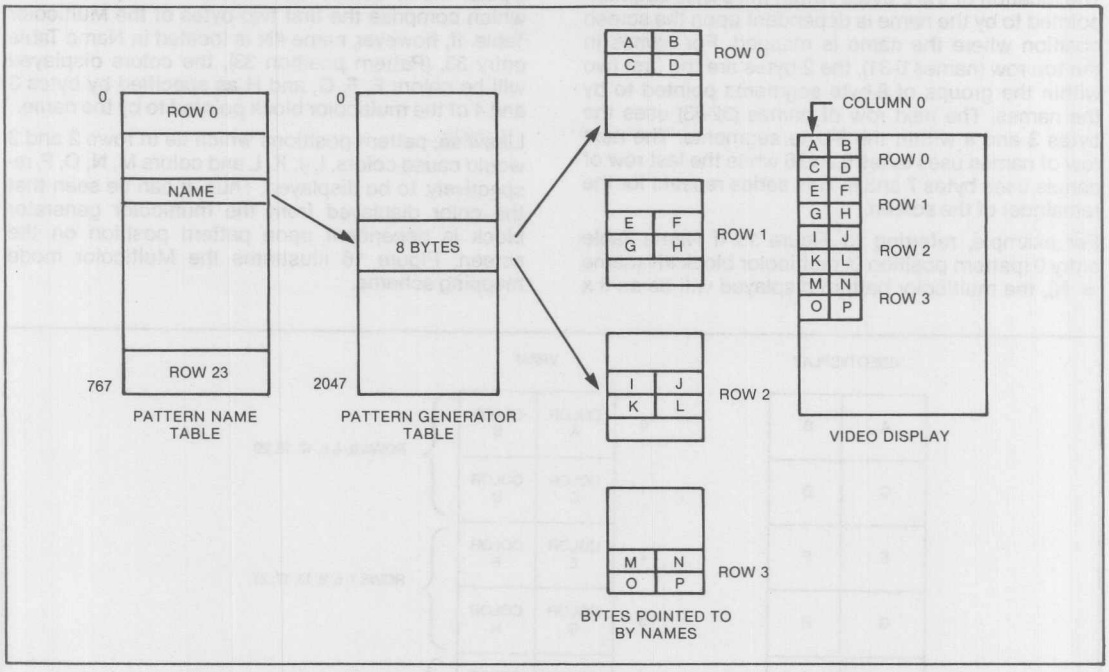


Figure 16. MULTICOLOR MODE MAPPING

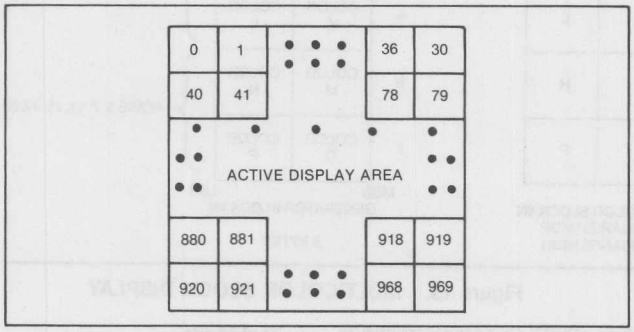


Figure 17. TEXT MODE NAME TABLE PATTERN POSITIONS

As with the Graphics modes, the Pattern Generator Table contains a library of text patterns that can be displayed in the text positions. It is 2048 bytes long and is arranged in 256 text patterns, each of which is 8 bytes long. Since each text position on the screen is only 6 pixels across, the least significant 2 bits of each text pattern are ignored, yielding 6 x 8 bits in each text pattern. Each 8-byte block defines a text pattern in which all the 1s in the text pattern take on one color when displayed on the screen, while all the 0s take on another color. These colors are chosen by loading VDP Register 7 with the color 1 and color 0 in the left and right nibbles, respectively WRITE ONLY REGISTERS.

In the Text mode, the Pattern Name Table determines the position of the text pattern on the screen as shown in Figure 18. There are 960 entries in the Pattern Name Table, each 1 byte long. There is a one-to-one correspondence between text pattern positions on the screen and entries in the Pattern Name Table (40 x 24 = 960). The first 40 entries correspond to the top row of text pattern positions on the screen, the next 40 to the second row, and so on. The value of an entry in the Pattern Name Table indicates which of the 256 text patterns is to be placed at that spot on the Pattern plane.

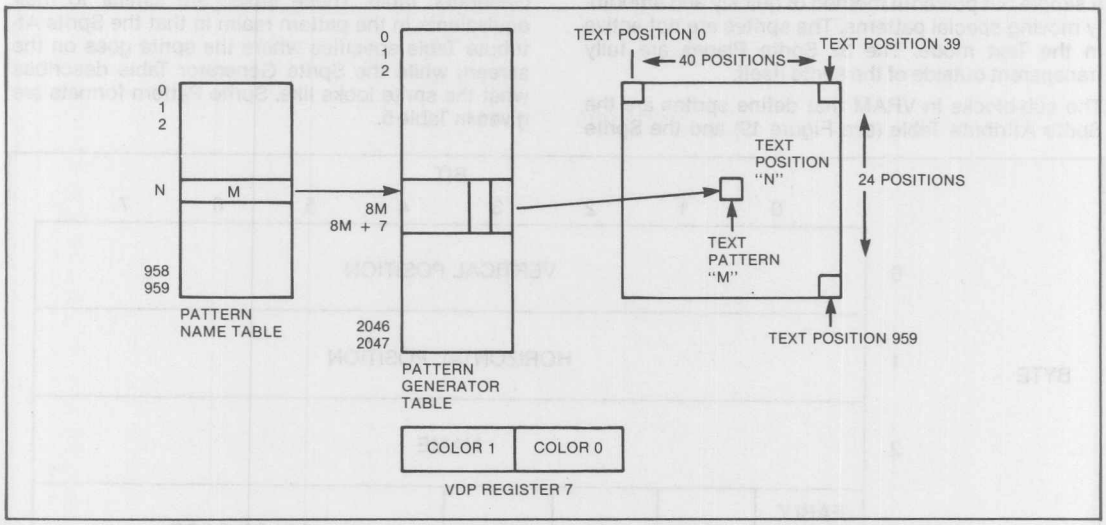


Figure 18. MAPPING OF VRAM INTO THE PATTERN PLANE IN TEXT MODE

The Pattern Name Table is located in a contiguous 960-byte block in VRAM, beginning on a 1-kilobyte boundary. The starting address of the name table is determined by the 4-bit name table base address field in VDP Register 2. The base address forms the upper 4 bits of the 14-bit VRAM address. The lower 10 bits of the VRAM address point to 1 of 960 pattern cells. The name table is organized by rows.

Each byte entry in the name table is the pointer to a pattern definition in the Pattern Generator Table. The same two colors are used for all 256 patterns; the color codes are stored in VDP Register 7.

As the name implies, the Text mode is intended mainly for textual applications, especially those in which the 32 patterns-per-line in Graphics modes is insufficient. The advantage is that eight more patterns can be fitted onto one line; the disadvantages are that sprites cannot be used, and only two colors are available for the entire screen.

With care, the same text pattern set that is used in Text mode can be also used in Graphics I mode. This is done by ensuring that the least significant 2 bits of all the character patterns are 0. Thus, a switch from Text mode to Pattern mode results in a stretching of the space between characters, and a reduction of the number of characters per line from 40 to 32. As with the Graphics Modes, once a character set has been defined and placed into the Pattern Generator, updating the Pattern Name Table will produce and manipulate textual material on the screen.

The full 8-bit pattern name is used to select 1 of the 256 pattern definitions in the pattern generator table. The table is a 2048-byte block in VRAM, beginning on a 2-kilobyte boundary. The starting address of the table is determined by the generator base address in VDP Register 4. The base address forms the 3 MSBs of the 14-bit VRAM address for each Pattern Generator Table entry. The next 8 bits are equal to the 8-bit name of the selected pattern definition. The lowest 3 bits of the VRAM address are equal to the row number within the pattern definition.

There are 8 bytes required for each of the 256 possible unique 6 x 8 pattern definitions. The first byte defines the first row of the pattern, and the second byte defines the second row. The least significant 2 bits in each byte are not used. However, it is strongly recommended that these bits be 0s. Each bit entry in the pattern definition selects one of the two colors for that pattern. A 1 bit selects the color code (color 1) contained in the most significant 4 bits of VDP Register 7. A 0 bit selects the other color code (color 0) which is in the least significant 4 bits of the same VDP Register. Figure 18 is an example of pattern definition mapping.

A total of 3008 VRAM bytes are required for the Pattern Name Generator Tables. Less memory is required if all 256 possible pattern definitions are not required; the tables can be overlapped to reduce the amount of VRAM needed for pattern generation. Examples of VRAM memory allocation are provided in VRAM ADDRESSING EXAMPLE.

Sprites

The video display can have up to 32 sprites on the highest priority video planes. The sprites are special animation patterns which provide smooth motion and multilevel pattern overlaying. The location of a sprite is defined by the top left-hand corner of the sprite pattern. The sprite can be easily moved pixel-by-pixel by redefining the sprite origin. This provides

a simple but powerful method of quickly and smoothly moving special patterns. The sprites are not active in the Text mode. The 32 Sprite Planes are fully transparent outside of the sprite itself.

The sub-blocks in VRAM that define sprites are the Sprite Attribute Table (see Figure 19) and the Sprite Generator Table. These tables are similar to their equivalents in the pattern realm in that the Sprite Attribute Table specifies where the sprite goes on the screen, while the Sprite Generator Table describes what the sprite looks like. Sprite Pattern formats are given in Table 5.

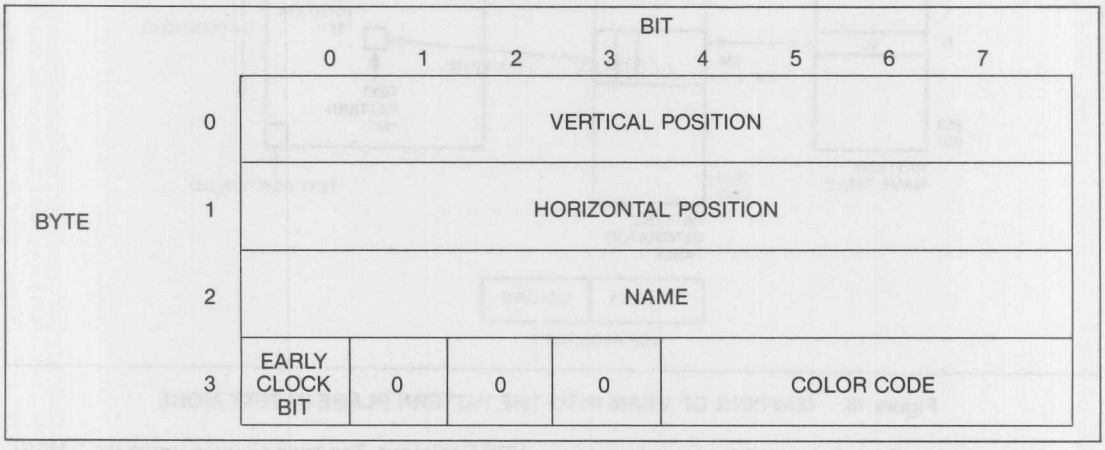


Figure 19. SPRITE ATTRIBUTE TABLE ENTRY

Table 5. SPRITE PATTERN FORMATS

SIZE	MAG	AREA	RESOLUTION	BYTES/PATTERN
0	0	8 x 8	single pixel	8
1	0	16 x 16	single pixel	32
0	1	16 x 16	2 x 2 pixels	8
1	1	32 x 32	2 x 2 pixels	32

Figure 20 illustrates the manner in which the VRAM tables map into the existence of sprites on the display. Since there are 32 sprites available for display, there are 32 entries in the Sprite Attribute Table. Each entry consists of four bytes. The entries are ordered so that the first entry corresponds to the sprite on the sprite 0 plane, the next to the sprite on the sprite 1 plane, and so on. The Sprite Attribute Table is 4 x 32 = 128 and is located in a contiguous 128-byte block in VRAM, beginning on a 128-byte boundary.

The starting address of the table is determined by the 7-bit Sprite Attribute Table base address in VDP Register 5. The base address forms the upper 7 bits of the 14-bit VRAM address. The next 5 bits of the VRAM address are equal to the sprite number. The lowest 2 bits select 1 of the 4 bytes in Sprite 2 Attribute Table entry for each sprite. Each table entry contains 4 bytes which specify the sprite position, sprite pattern name, and color, as shown in Figure 19.

The first two bytes of each entry of the Sprite Attribute Table determine the position of the sprite on the display. The first byte indicates the vertical distance of the sprite from the top of the screen, in pixels. It is defined such that a value of −1 puts the sprite butted up at the top of the screen, touching the backdrop area. The second byte describes the horizontal displacement of the sprite from the left edge of the display. A value of 0 butts the sprite up against the left edge of the backdrop. Note that all measurements are taken from the upper left pixel of the sprite.

When the first two bytes of an entry position a sprite so it overlaps backdrop, the part of the sprite that is within the backdrop is displayed normally. The part of the sprite that overlaps the backdrop is hidden from view by the backdrop. This allows the animator to move a sprite into display from behind the backdrop.

The displacement in the first byte is partially signed, in that values for vertical displacement between −31 and 0 (E116 to 0) allow a sprite to bleed-in from the top edge of the backdrop. Similarly, horizontal displacement values in the vicinity of 255 allow a sprite to bleed-in from the right side of the side of the screen. To allow sprites to bleed-in from the left edge

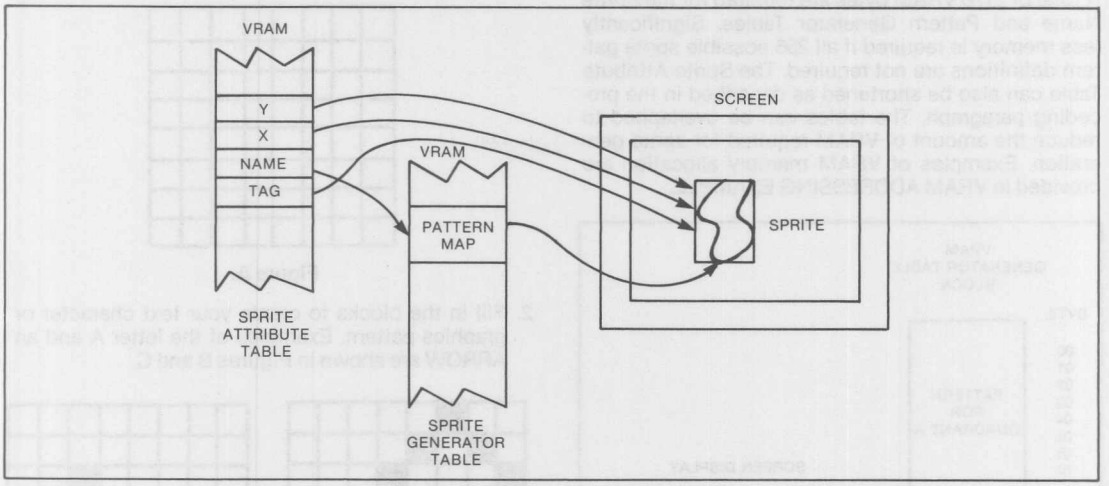


Figure 20. SPRITE MAPPING

of the backdrop, a special bit in the third byte of the Sprite Attribute Table entry is used.

Byte 3 of the Sprite Attribute Table entry contains the pointer to the Sprite Generator Table that specifies what the sprite should look like. This is an 8-bit pointer to the sprite patterns definition, the Sprite Generator Table. The sprite name is similar to that in the Graphics Modes.

Byte 4 of the Sprite Attribute Table entry contains the color of the sprite in its lower 4 bits (see Table 3 for color assignments). The MSB is the Early Clock (EC) bit. When set to 0, this bit does nothing. When set to 1, the horizontal position of the sprite is shifted to the left by 32 pixels. This allows a sprite to bleed-in from the left edge of the backdrop. Values for horizontal displacement (byte 2 in the entry) in the range 0 to 32 cause the sprite to overlap with the left-hand border of the backdrop.

The Sprite Generator Table is a maximum of 2048 bytes long beginning on the 2-kilobyte boundaries. It is arranged into 256 blocks of 8 bytes each. The third byte of the Sprite Attribute Table entry, then specifies which 8-byte block to use to specify a sprite's shape. The 1s in the Sprite Generator cause the sprite to be defined at the point; 0s cause the transparent color to be used. The starting address of the table is determined by the sprite generator base address in VDP Register 6. The base address forms the 3 MSB of the 14-bit VRAM address. The next 8 bits of the address are equal to sprite name, and the last 3 bits are equal to the row number within the sprite pattern. The address formation is slightly modified for $SIZE_1$ sprites.

There is a maximum limit of four sprites that can be displayed on one horizontal line. If this rule is violated, the four highest-priority sprites on the line are displayed normally. The fifth and subsequent sprites are not displayed on that line. Furthermore, the fifth-sprite bit in the VDP status register is set to a 1, and the number of the violating fifth sprite is loaded into the status register STATUS REGISTER.

Larger sprites than 8 x 8 pixels can be used if desired. The MAG and SIZE bits in VDP register 1 are used to select the various options described in the following paragraphs.

MAG = 0,SIZE = 0: No options chosen

MAG = 1,SIZE = 0: The Sprite Generator Table uses 8 bytes to describe the sprite; however, each bit in the Sprite Generator maps into 2 x 2 pixels on the TV screen, effectively doubling the size of the sprite to 16 x 16.

MAG = 0,SIZE = 1: The Sprite Generator Table uses 31 bytes to define the sprite shape; the result is a 16 x 16-pixel sprite. The mapping of the 32 bytes into the sprite image is as shown in Figure 21. Mapping is still 1 bit to 1 pixel.

MAG = 1,SIZE = 1: Same as MAG = 0,SIZE = 1 except each bit now maps into a 2-pixel area, yielding a 32 x 32 sprite.

The VDP provides sprite coincidence checking. The coincidence status flag in the VDP status register is set to a 1 whenever two active sprites have 1 bits at the same screen location.

Sprite processing is terminated if the VDP finds a value of 208 (D016) in the vertical position field of any entry in the Sprite Attribute Table. This permits the Sprite Attribute Table to be shortened to the minimum size required; it also permits the user to blank out part or all of the sprites by simply changing one byte in VRAM.

A total of 2176 VRAM bytes are required for the Sprite Name and Pattern Generator Tables. Significantly less memory is required if all 256 possible sprite pattern definitions are not required. The Sprite Attribute Table can also be shortened as described in the preceding paragraph. The tables can be overlapped to reduce the amount of VRAM required for sprite generation. Examples of VRAM memory allocation are provided in VRAM ADDRESSING EXAMPLE.

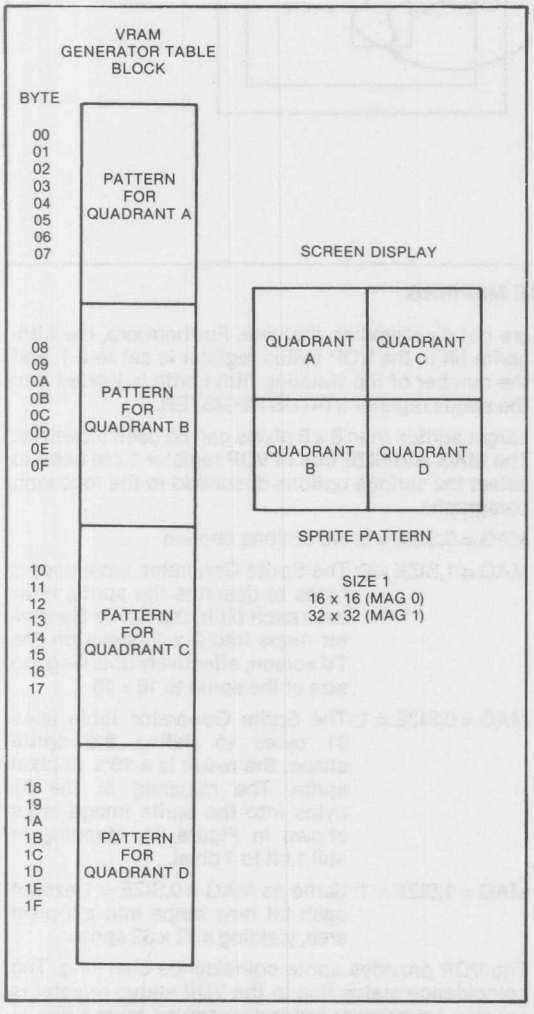


Figure 21. SIZE 1 SPRITE MAPPING

A Step-by-Step Approach to Create Patterns and Sprites

PATTERNS:

1. Use an 8 x 8 pattern similar to that in Figure A. Each small square represents one pixel on the screen.

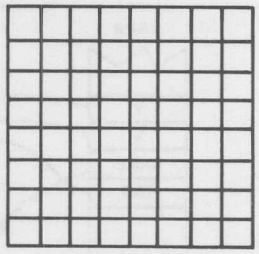


Figure A.

2. Fill in the blocks to create your text character or graphics pattern. Examples of the letter A and an ARROW are shown in Figures B and C.

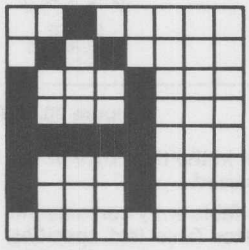


Figure B.

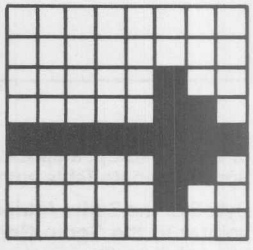


Figure C.

NOTE:
If these patterns are to be used in the Text mode, (40 patterns per line), the pattern should be inside a left-justified 6 x 8 block like the A shown in Figure B. If all of the Text patterns are inside this 6 x 8 block, they can be used for Text and Graphics 1 and 2 modes.

3. Assign 1s to the filled-in areas and 0s to the blanks. Then convert the 1s and 0s to their hexadecimal equivalents, as shown in Figure D.

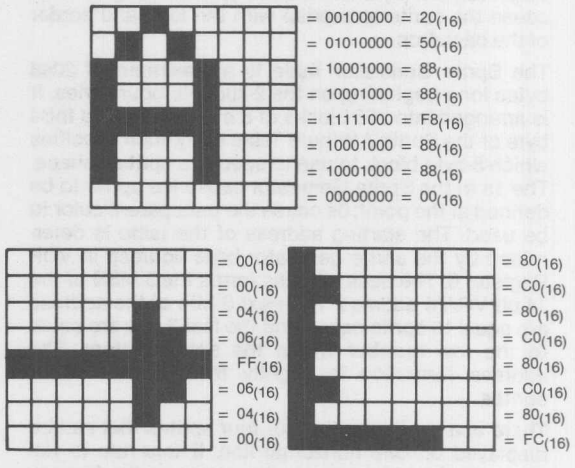
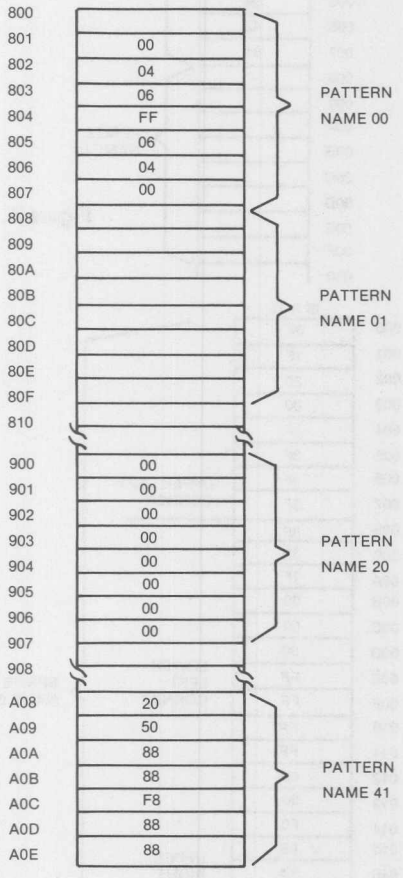


Figure D.

4. Now place the eight bytes defining the pattern into the Pattern Generator Table. Assume the Pattern Generator Table. Assume the Pattern Generator Table sub-block is located at 800_{16} and the arrow pattern is to be named 00_{16}. Then place the eight pattern bytes as follows:



NOTE:
When using text in your applications, you can place the eight bytes of the text character in its ASCII number location.

Example: ASCII SPACE = 20_{16}
? = $3F_{16}$
A = 41_{16}
B = 42_{16}
C = 43_{16}
Etc.

This simplifies writing text to the screen. Simply write the ASCII name directly to the Pattern Name Table. A space character is shown in Pattern Generator Table position 20, and A is shown in pattern name 41.

SPRITES

1. Determine whether to use 8 x 8 or 16 x 16 sprite patterns. Then use the appropriate work pattern, as shown in Figures E and F.

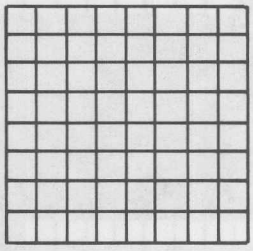


Figure E.

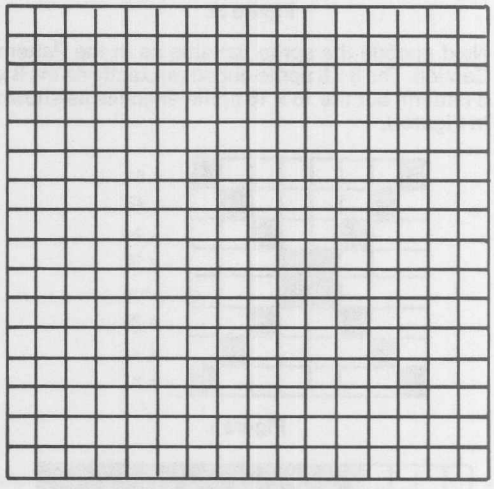


Figure F.

2. Fill in the blocks to create your sprite pattern. Examples are shown in Figures G and H.

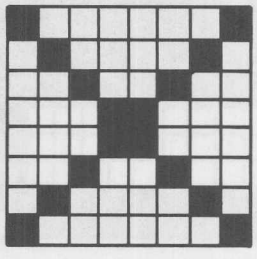


Figure G.

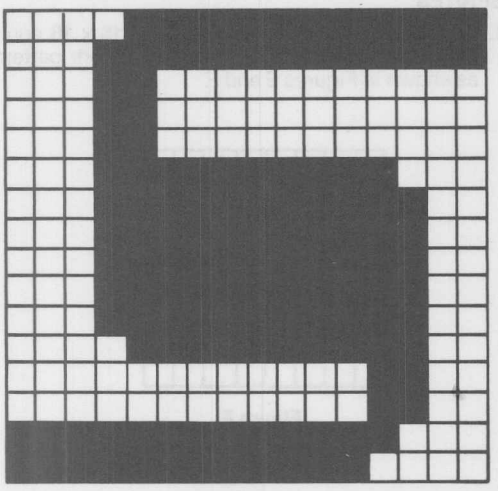


Figure H.

3. Next encode the sprite patterns as in the Pattern Section. The 8 x 8 sprite encodes exactly as the 8 x 8 pattern, but the 16 x 16 sprite encodes as shown in Figure J.

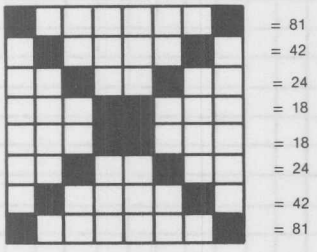


Figure I.

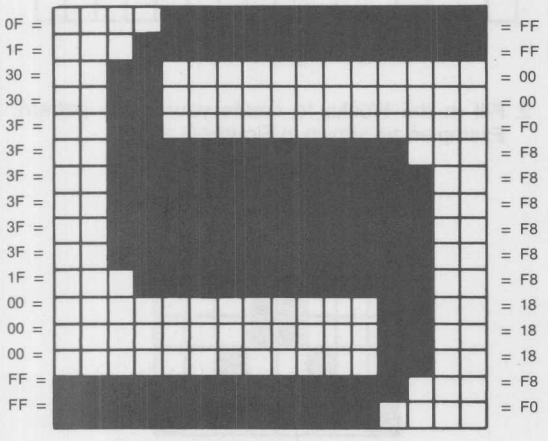


Figure J.

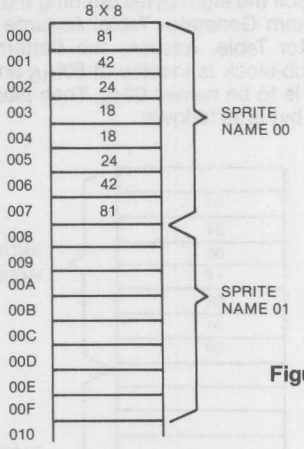


Figure K.

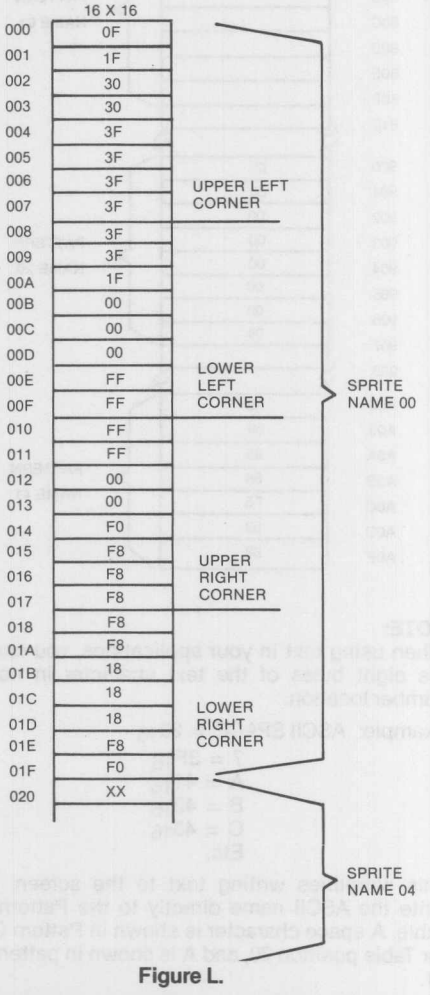


Figure L.

Break the 16 x 16 block pattern into four 8 x 8 patterns. Next, encode the 8 x 8 patterns starting in the upper left corner, then do the lower left, upper right, and lower right.

4. Place the 8 bytes for 8 x 8 sprites or 32 bytes for 16 x 16 sprites in the Sprite Generator Table. Assuming the sprite generator table is located at location 0000, Figures K and L show how the tables should look for 8 x 8 and 16 x 16 sprites.

16 x 16 sprite patterns start in the table with the byte from the upper left-hand corner. Then start with the upper right, going toward the lower right.

WRITE-ONLY REGISTERS

The eight VDP write-only registers are shown in Figure 22. They are loaded by the CPU as described in CPU Write to VDP Register. Registers 0 and 1 contain flags to enable or disable various VDP features and modes. Registers 2 through 6 contain values that specify starting locations of various sub-blocks of VRAM. The definitions of these sub-blocks are described in VIDEO DISPLAY MODE. Register 7 is used to define backdrop and text colors.

Each register is described in the following paragraphs.

Register 0

Register 0 contains two VDP option control bits. All other bits are reserved for future use and must be 0s.

BIT 6 — M3 (mode bit 3) (see Coincidence Flag (C) for table and description)

BIT 7 — External VDP enable/disable
0 disables external VDP input
1 enables external VDP input

NOTE:
Enabling bit 7 in the WD9928/9929 causes A-Y and B-Y to go the sync level only when all planes in front of the pixel under question are transparent.

Register 1 (contains 8 VDP option control bits)

BIT 0 — 4/16K selection
0 selects 4027 RAM operation
1 selects 4108/4116 RAM operation

BIT 1 — BLANK enable/disable
0 causes the active display area to blank
1 enables the active display
Blanking causes the display to show border color only

BIT 2 — IE (Interrupt Enable)
0 disables VDP interrupt
1 enables VDP interrupt

BIT 3,4 — M1, M2 (mode bits 1 and 2)
M1, M2 and M3 determine the operating mode of the VDP:

M1	M2	M3	
0	0	0	Graphics I mode
0	0	1	Graphics II mode
0	1	0	Multicolor Mode
1	0	0	Text mode

BIT 5 — Reserved

BIT 6 — Size (sprite size select)
0 selects Size 0 sprites (8 x 8 bit)
1 selects Size 1 sprites (16 x 16 bits)

BIT 7 — MAG (Magnification option for sprites)
0 selects MAG0 sprites (1X)
1 selects MAG1 sprites (2X)

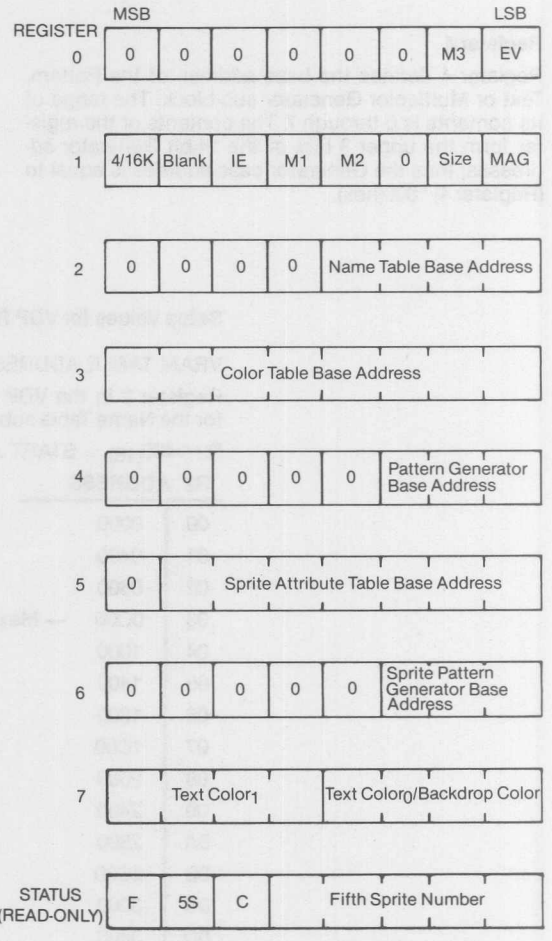


Figure 22. VDP REGISTERS

Register 2

Register 2 defines the base address of the Name Table sub-block. The range of its contents is from 0 to 15. The contents of the register form the upper 4 bits of the 14-bit Name Table addresses; thus the Name Table base address is equal to (Register 2) *400(hex).

Register 3

Register 3 defines the base address of the Color Table sub-block. The range of its contents is from 0 to 255. The contents of the register form the upper 8 bits of the 14-bit Color Table addresses; thus the Color Table base address is equal to (Register 3) *40(hex).

Register 4

Register 4 defines the base address of the Pattern, Text or Multicolor Generator sub-block. The range of its contents is 0 through 7. The contents of the register form the upper 3 bits of the 14-bit Generator addresses; thus the Generator base address is equal to (Register 4) *800(hex).

Register 5

Register 5 defines the base address of the Sprite Attribute Table sub-block. The range of its contents is from 0 through 127. The contents of the register form the upper 7 bits of the 14-bit Sprite Attribute Table addresses; thus the base address is equal to (Register 5) *80(hex).

Register 6

Register 6 defines the base address of the Sprite Pattern Generator sub-block. The range of its contents is 0 through 7. The contents of the register form the upper 3 bits of the 14-bit Sprite Pattern Generator addresses; thus the Sprite Pattern Generator base address is equal to (Register 6) *800(hex).

Register 7

The upper 4 bits of Register 7 contain the color code of color 1 in the Text mode. The lower 4 bits contain the color code for color 0 in the Text mode and the backdrop color in all modes.

Setup Values for VDP Registers 2 through 6.

VRAM TABLE ADDRESSING

Register 2 in the VDP contains the starting address for the Name Table sub-block.

$R2 * 400_{(16)}$ = START ADDRESS

R2	ADDRESS	
00	0000	
01	0400	
02	0800	
03	0C00	— Maximum Number for 4K RAMs
04	1000	
05	1400	
06	1800	
07	1C00	
08	2000	
09	2400	
0A	2800	
0B	2C00	
0C	3000	
0D	3400	
0E	3800	
0F	3C00	— Maximum Number

Register 3 in the VDP contains the starting address for the Color Table.

(R3) * $40_{(16)}$ STARTING ADDRESS

R3	START ADDRESS	R3	START ADDRESS	R3	START ADDRESS
00	0000	28	0A00	50	1400
01	0040	29	0A40	51	1440
02	0080	2A	0A80	52	1480
03	00C0	2B	0AC0	53	14C0
04	0100	2C	0B00	54	1500
05	0140	2D	0B40	55	1540
06	0180	2E	0B80	56	1580
07	01C0	2F	0BC0	57	15C0
08	0200	30	0C00	58	1600
09	0240	31	0C40	59	1640
0A	0280	32	0C80	5A	1680
0B	02C0	33	0CC0	5B	16C0
0C	0300	34	0D00	5C	1700
0D	0340	35	0D40	5D	1740
0E	0380	36	0D80	5E	1780
0F	03C0	37	0DC0	5F	17C0
10	0400	38	0E00	60	1800
11	0440	39	0E40	61	1840
12	0480	3A	0E80	62	1880
13	04C0	3B	0EC0	63	18C0
14	0500	3C	0F00	64	1900
15	0540	3D	0F40	65	1940
16	0580	3E	0F80	66	1980
17	05C0	3F	0FC0*	67	19C0
18	0600	40	1000	68	1A00
19	0640	41	1040	69	1A40
1A	0680	42	1080	6A	1A80
1B	06C0	43	10C0	6B	1AC0
1C	0700	44	1100	6C	1B00
1D	0740	45	1140	6D	1B40
1E	0780	46	1180	6E	1B80
1F	07C0	47	11C0	6F	1BC0
20	0800	48	1200	70	1C00
21	0840	49	1240	71	1C40
22	0880	4A	1280	72	1C80
23	08C0	4B	12C0	73	1CC0
24	0900	4C	1300	74	1D00
25	0940	4D	1340	75	1D40
26	0980	4E	1380	76	1D80
27	09C0	4F	13C0	77	1DC0

*Maximum number for 4K RAMs

(R3) * $40_{(16)}$ STARTING ADDRESS (Continued)

R3	START ADDRESS	R3	START ADDRESS	R3	START ADDRESS
78	1E00	A6	2980	D3	34C0
79	1E40	A7	29C0	D4	3500
7A	1E80	A8	2A00	D5	3540
7B	1EC0	A9	2A40	D6	3580
7C	1F00	AA	2A80	D7	35C0
7D	1F40	AB	2AC0	D8	3600
7E	1F80	AC	2B00	D9	3640
7F	1FC0	AD	2B40	DA	3680
80	2000	AE	2B80	DB	36C0
81	2040	AF	2BC0	DC	3700
82	2080	B0	2C00	DD	3740
83	20C0	B1	2C40	DE	3780
84	2100	B2	2C80	DF	37C0
85	2140	B3	2CC0	E0	2800
86	2180	B4	2D00	E1	3840
87	21C0	B5	2D40	E2	3880
88	2200	B6	2D80	E3	38C0
89	2240	B7	2DC0	E4	3900
8A	2280	B8	2E00	E5	3940
8B	22C0	B9	2E40	E6	3980
8C	2300	BA	2E80	E7	39C0
8D	2340	BB	2EC0	E8	3A00
8E	2380	BC	2F00	E9	1A40
8F	23C0	BD	2F40	EA	3A80
90	2400	BE	2F80	EB	3AC0
91	2440	BF	2FC0	EC	3B00
92	2480	C0	3000	ED	3B40
93	24C0	C1	3040	EE	3B80
94	2500	C2	3080	EF	3BCD
95	2540	C3	30C0	F0	3C00
96	2580	C4	3100	F1	3C40
97	25C0	C5	3140	F2	3C80
98	2600	C6	3180	F3	3CC0
99	2640	C7	31C0	F4	2D00
9A	2680	C8	3200	F5	3D40
9B	26C0	C9	3240	F6	3D00
9C	2700	CA	3280	F7	3DC0
9D	2740	CB	32C0	F8	3E00
9E	2780	CC	3300	F9	3E40
9F	27C0	CD	3340	FA	3E80
A0	2800	CE	3380	FB	3EC0
A1	2840	CF	33C0	FC	3F00

(R3) * $40_{(16)}$ STARTING ADDRESS (Concluded)

R3	START ADDRESS	R3	START ADDRESS	R3	START ADDRESS
A2	2880	D0	3400	FD	3F40
A3	28C0	D1	3440	FE	3F80
A4	2900	D2	3480	FF	3FC0
A5	2940				

Register 4 in the VDP contains the starting address for the Pattern Generator Sub-block.

(R4) * $800_{(16)}$ = START ADDRESS

R4	START ADDRESS	
00	0000	
01	0800	— Max # for 4K RAMs
02	1000	
03	1800	
04	2000	
05	2800	
06	3000	
07	3800	— Max # for 16K RAMs

Register 5 in the VDP contains the starting address for the Sprite Attribute Table.

(R5) * $80_{(16)}$ START ADDRESS

R5	START ADDRESS	R5	START ADDRESS	R5	START ADDRESS	R5	START ADDRESS
00	0000	21	1080	40	2000	60	3000
01	0080	22	1100	41	2080	61	3080
02	0400	23	1180	42	2100	62	3100
03	0180	24	1200	43	2180	63	3180
04	0200	25	1280	44	2200	64	3200
05	0280	26	1300	45	2280	65	3280
06	0300	27	1380	46	2300	66	3300
07	0380	28	1400	47	2380	67	3380
08	0400	29	1480	48	2400	68	3400
09	0480	2A	1500	49	2480	69	3480
0A	0500	2B	1580	4A	2500	6A	3500
0B	0580	2C	1600	4B	2580	6B	3580
0C	0600	2D	1680	4C	2600	6C	3600
0D	0680	2E	1700	4D	2680	6D	3680
0E	0700	2F	1780	4E	2700	6E	3700
0F	0780	30	1800	4F	2780	6F	3780
10	0800	31	1880	50	2800	70	3800
11	0880	32	1900	51	2880	71	3880

(R5) * 80(16) START ADDRESS

R5	START ADDRESS	R5	START ADDRESS	R5	START ADDRESS	R5	START ADDRESS
12	0900	33	1980	52	2900	72	3900
13	0980	34	1A00	53	2980	73	3980
14	0A00	35	1A80	54	2A00	74	3A00
15	0A80	36	1B00	55	2A80	75	3A80
16	0B00	37	1B80	56	2B00	76	3B00
17	0B80	38	1C00	57	2B80	77	3B80
18	0C00	39	1C80	58	2C00	78	3C00
19	0C80	3A	1D00	59	2C80	79	3C80
1A	0D00	3B	1D80	5A	2D00	7A	3D00
1B	0D80	3C	1E00	5B	2D80	7B	3D80
1C	0E00	3D	1E80	5C	2E00	7C	3E00
1D	0E80	3E	1F00	5D	2E80	7D	3E80
1E	0F00	3F	1F80	5E	2F00	7E	3F00
1F	0F80*			5F	2F80	7F	3F80
20	1000						

*Maximum number for 4K RAMs.

Register 6 contains the value for the starting address of the Sprite Pattern Generator sub-block.

STARTING ADDRESS = R6 * <800

R6	START ADDRESS	
00	0000	
01	0800	— Max # for 4K DRAMs
02	1000	
03	1800	
04	2000	
05	2800	
06	3000	
07	3800	— Max # for 16K RAMs

STATUS REGISTER

The VDP has a single 8-bit status register that can be accessed by the CPU. The status register contains the interrupt pending flag, the sprite coincidence flag, the fifth sprite flag, and the fifth sprite number, if one exists. The format of the status register is shown in Figure 22 and is discussed in the following paragraphs.

The status register may be read at any time to test the F, C, and 5S status bits. Reading the status register will clear the interrupt flag, F. However, asynchronous reads will cause the frame flag (F) bit to be reset and therefore missed. Consequently, the status register should be read only when the VDP interrupt is pending.

Interrupt Flag (F)

The F status flag in the status register is set to 1 at the end of the raster scan of the last line of the active display. It is reset to a 0 after the status register is read or when the VDP is externally reset. If the Interrupt Enable bit in VDP Register 1 is active (1), the VDP interrupt output (INT) will be active (low) whenever the F status flag is a 1.

Note that the status register needs to be read frame by frame in order to clear the interrupt the receive the new interrupt of the next frame.

Coincidence Flag (C)

The C status flag in the status register is set to a 1 if two or more sprites coincide. Coincidence occurs if any two sprites on the screen have one overlapping pixel. Transparent colored sprites, as well as those that are partially or completely off the screen, are also considered. Sprites beyond the Sprite Attribute Table terminator (D016) are not considered. The C flag is cleared to a 0 after the status register is read or the VDP is externally reset. The status register should be read immediately upon powerup to ensure that the coincidence flag is reset.

The VDP checks each pixel position for coincidence during the generation of the pixel regardless of where it is located on the screen. This occurs every 1/60th of a second for the WD9918 and WD9928 and every 1/50th of a second for the WD9929. Thus, when moving sprites more than one pixel position during these intervals, it is possible for the sprites to have multiple pixels overlapping or even to have passed completely over one another when the VDP checks for coincidence.

Fifth Sprite Flag (5S) and Number

The 5S status flag in the status register is set to a 1 whenever there are five or more sprites on a horizontal line (lines 0 to 192) and the frame flag is equal to a 0. The 5S status flag is cleared to a 0 after the status register is read or the VDP is externally reset. The number of the fifth sprite is placed into the lower 5 bits of the status register when the 5S flag is set and is valid whenever the 5S flag is 1. The setting of the fifth sprite flag will not cause an interrupt.

VDP/VRAM INTERFACE

The VDP can access up to 16,384 bytes of VRAM using a 14-bit VRAM address. The VDP fetches data from the VRAM in order to process the video image described later. The VDP also stores data in or reads in data from the VRAM during a CPU-VRAM data transfer. The VDP automatically refreshes the VRAM.

VRAM Interface Control Signals

The VDP-VRAM interface consists of two 8-bit data buses (RD0-RD7 unidirectional, AD0-AD7 bidirectional) and three control lines, as shown in Figure 23. The VRAM outputs data to the VDP on the VRAM read data bus (RD0-RD7). The VDP outputs both the address and data to the VRAM over the VRAM address/data bus (AD0-AD7). The VRAM row address is output when RAS is active (low). The column address is output when CAS is active (low). Data is output to the VRAM when R/W is active (low).

VRAM Memory Types

The VDP can use 4K, 8K, or 16K dynamic RAMs. The 4/16K bit in VDP register 1 is a 0 for 4K RAMs and a 1 for 8K or 16K RAMs. There is a minor difference between the way 4K and 8K/16K RAMs are wired to the VDP. In the 4K, all CE pins are ties to ground. In the 8K/16K the A6 lines (the same pin as CE) are all tied to AD1 on the WD9918. A jumper can be used to select the VRAM type.

VDP to DRAM Address Connections

The VDP can be easily connected to either the 4K or 16K DRAMs. However, due to different pin numbering standards, it is possible to connect the VDP to the DRAMs incorrectly. Table 6 shows the recommended way to connect a VDP to either DRAM. Other DRAMs, such as the single +5V supply type, can also be used by following the 4K or 16K columns in Table 6.

Table 6.
VDP TO DRAM ADDRESS CONNECTIONS

VDP	16K DRAM	4K DRAM
AD0	Data Only	Data Only
AD1	A6	Data Only
AD2	A5	A5
AD3	A4	A4
AD4	A3	A3
AD5	A2	A2
AD6	A1	A1
AD7	A0	A0

When connecting the data ports together, ensure that corresponding RAMs (assuming 8 by 1 DRAMs) are properly connected to the corresponding input or output of the VDP. For example, AD0 of the corresponding input or output D input of the RAM, and RD0 of the VDP should connect to the Q output of the same RAM. The same is true for all AD and RD corresponding pins for each of the eight DRAMs.

NOTE:
CD0 is the MSB of the CD bus; CD7 is the LSB.
AD0 is the MSB of the AD bus; AD7 is the LSB.
RD0 is the MSB of the RD bus; RD7 is the LSB.
RAMs have the reverse convention.
AD7 is the MSB of the AD bus, and AD0 is the LSB.

Therefore, AD7 of the VDP connects to AD, and AD1 connects to A6 of the 16K DRAM. Data coming into the VDP on CD0 goes to VRAM on AD0 and returns to the VDP on RD0.

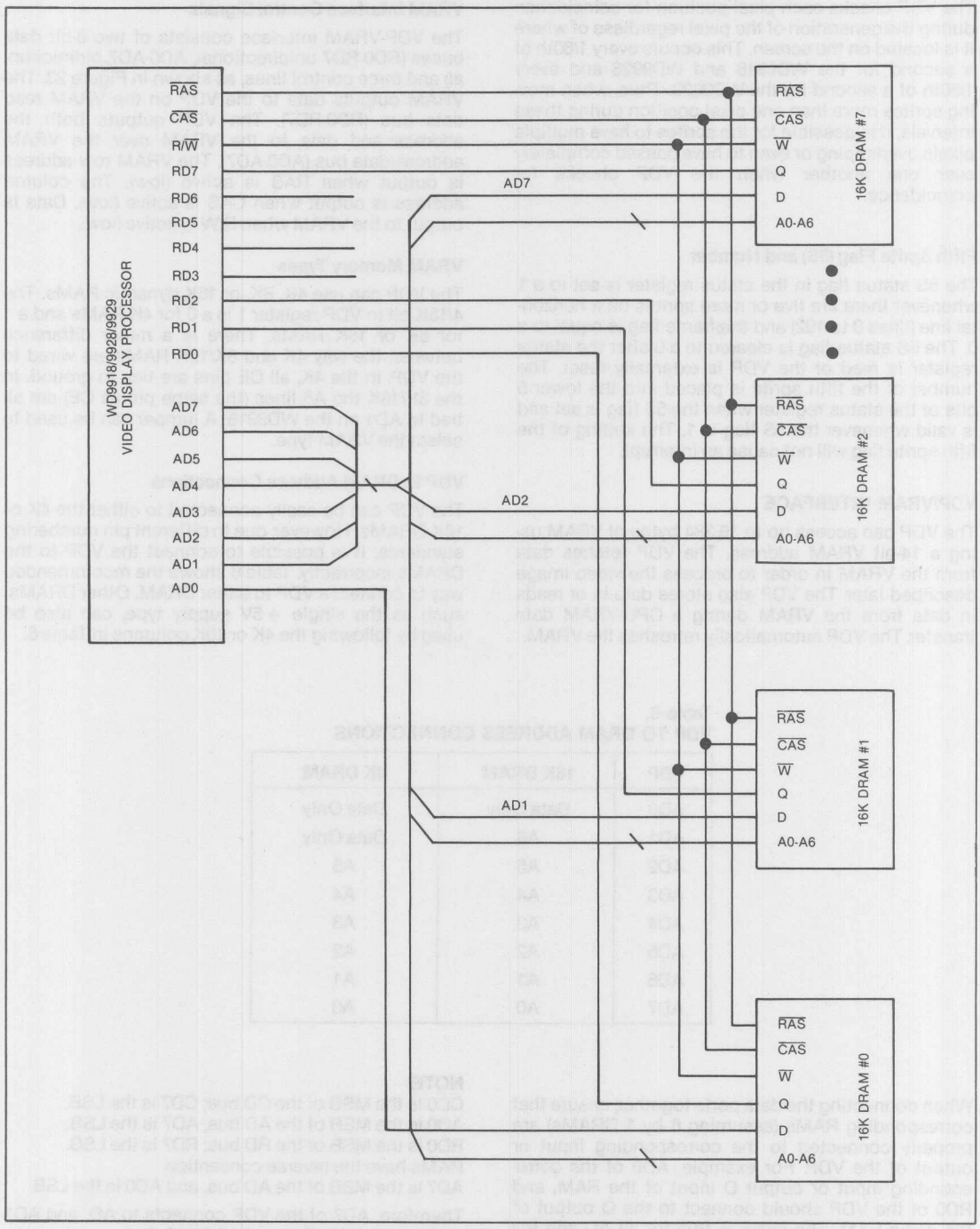


Figure 23. VRAM INTERFACE

VRAM MEMORY ADDRESS DERIVATION

Table 7 summarizes the VRAM address derivation for all VDP modes of operation.

Table 7. PATTERN GRAPHICS ADDRESS LOCATION TABLES

GRAPHICS I MODE ADDRESS LOCATION

ADDRESS TYPE	0 1 2 3 4 5 6 7 8 9 10 11 12 13	COMMENTS
1) Pattern Name Address	NTB / Row / Column	Pattern name table base (VDP REG2) Pattern position
2) Pattern Color Address	COLB / 0 / Name (0-4)	Pattern color table base (VDP REG3) Always "0" in Bit 8 Five most significant bits of name
3) Pattern Generator Address	PGB / Name / XXX	Pattern generator base (VDP REG4) All 8 bits of name Three LSB's form pattern row position

GRAPHICS II MODE ADDRESS LOCATION

ADDRESS TYPE	0 1 2 3 4 5 6 7 8 9 10 11 12 13	COMMENTS
1) Pattern Name Address	NTB / Row / Column	Pattern name table base (VDP REG2) Pattern position row Pattern position column
2) Pattern Color Address	XX / Name / XXX	Pattern color table base MSB (VDP REG3) Two MSB from vertical counter All 8 bits of name Color table byte/line
3) Pattern Generator Address	XX / Name / XXX	Pattern name table base MSB (VDP REG4) Two MSB from vertical counter All 8 bits of name Pattern generator byte/line number

TEXT MODE ADDRESS LOCATION

ADDRESS TYPE	0 1 2 3 4 5 6 7 8 9 10 11 12 13	COMMENTS
Text Mode Name Address	NTB / Text Position	Pattern name table base (VDP REG2) Equal (text position row # times 40) plus (text position column number)
Text Mode Pattern Address	PGB / Name / XXX	Pattern generator base (VDP REG4) Name Byte/line number

Table 7. PATTERN GRAPHICS ADDRESS LOCATION TABLES (CONTINUED)

SPRITE ADDRESS LOCATION

ADDRESS TYPE	0	1	2	3	4	5	6	7	8	9	10	11	12	13	COMMENTS
Sprite Attribute Address	SAB														Sprite attribute table base (VDP REG5)
											Sprite				Sprite number
														XX	Attribute number: 00 for vertical position 01 for horizontal position 10 for name 11 for TAG (early clock and color)
Size = 0 Sprite Pattern Generator	SPGB														Sprite pattern generator base (VDP REG4)
					Name										Name attribute of Sprite
													XXX		Three LSB's give byte/line number
Size = 1 Sprite Pattern Generator	SPGB														Sprite pattern generator base (VDP REG4)
					Name (0-5)										Six MSB of name
											XXXXX				Size = 1 Sprite byte number (See Figure 4-4)

MULTICOLOR ADDRESS LOCATION

ADDRESS TYPE	0	1	2	3	4	5	6	7	8	9	10	11	12	13	COMMENTS
4) Multicolor Name Address	NTB														Name table base (VDP REG2)
					Row										Pattern position row
											Column				Pattern position column
5) Multicolor Color Generator Address	PGB														Pattern generator base (VDP REG4)
					Name										Name from name fetch
													XXX		Three LSB's form byte/square row

The WD9918/9928 operates at 262 lines per frame and approximately 60 frames per second in a noninterlaced mode of operation. The WD9929 operates at 313 lines per frame and approximately 50 frames per second in a noninterlaced mode of operation.

VRAM ADDRESSING EXAMPLE

A typical application might require up to 256 unique 8 x 8 patterns with no more than 2 colors per pattern and up to 32 8 x 8 sprites.

These conditions dictate in which mode the VDP is to be used. The sprite requirement and the 8 x 8 pattern blocks eliminate the text and multicolor modes, respectively. This leaves only the Graphics I and Graphics II modes, and since two colors per block are all that are necessary, Graphics I is employed due to its ease of use.

Figure 24 shows a memory map that allows these functions to fit into a 4K memory area.

Register values for Figure 24 are as follows:

Register 0 = 00 External VDP disabled, M3 = 0
Register 1 = C0 16K DRAM selected, Blank = 1, Graphics 1 mode selected, SIZE = 0, MAG = 0
Register 2 = 01 Name Table Start Address @ >400
Register 3 = 08 Color Table Start Address @ >0200
Register 4 = 01 Pattern Generator Start Address @ >800
Register 5 = 02 Sprite Attribute Table Start Address >100
Register 6 = 00 Sprite Pattern Generator Start Address @ >0000
Register 7 = XX Determined by user.

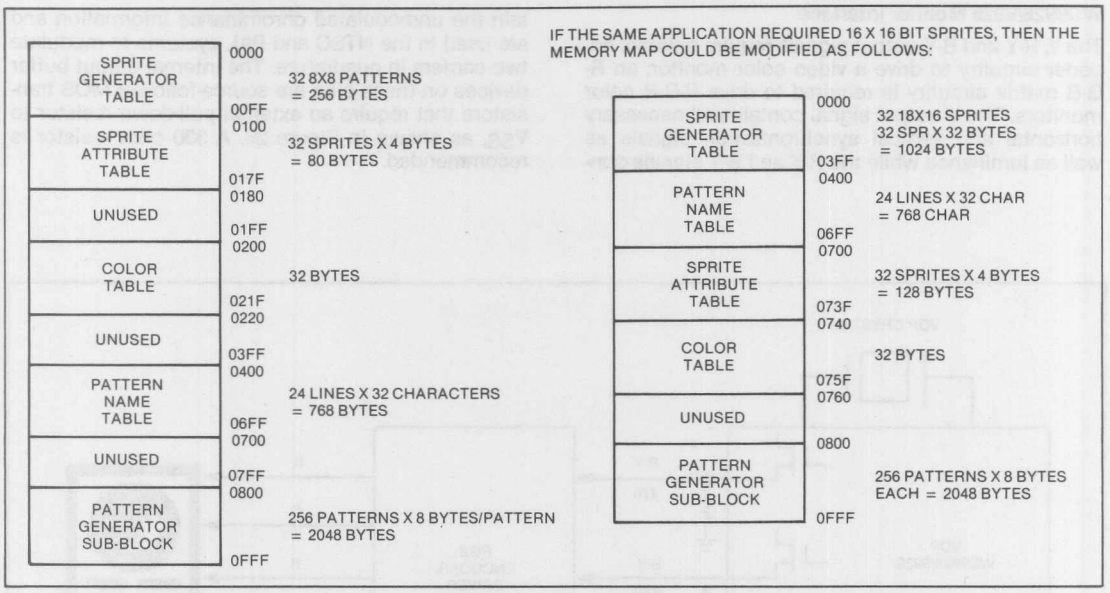


Figure 24. VDP-VRAM MEMORY ALLOCATION

MONITOR INTERFACES

WD9918 Monitor Interface

The composite video output signal from the WD9918 drives a color monitor. This signal incorporates all necessary horizontal and vertical synchronization signals as well as luminance and chrominance information. In monitor applications, the requirements of the monitor should be studied to determine if the VDP can be connected directly to it. The internal output buffer device on the composite video pin is a source-follower MOS transistor that requires an external pull-down resistor to V_{SS} as shown in Figure 25. Typically a 330-ohm resistor is recommended to provide a 1.9-volt synchronization level. The load resistor (R_L) defines the sharpness of the edges on the video signals. A lower resistor value gives faster fall times and a sharper picture.

In some cases, it may be necessary to provide a simple interface circuit to match the VDP output voltages with the monitor specifications. To drive a standard television that is not outfitted with a composite video input, the signal can be run into the television antenna terminals by using an appropriate RF modulator of the VDP output. Take care to ensure a proper match between VDP, RF modulator, and TV.

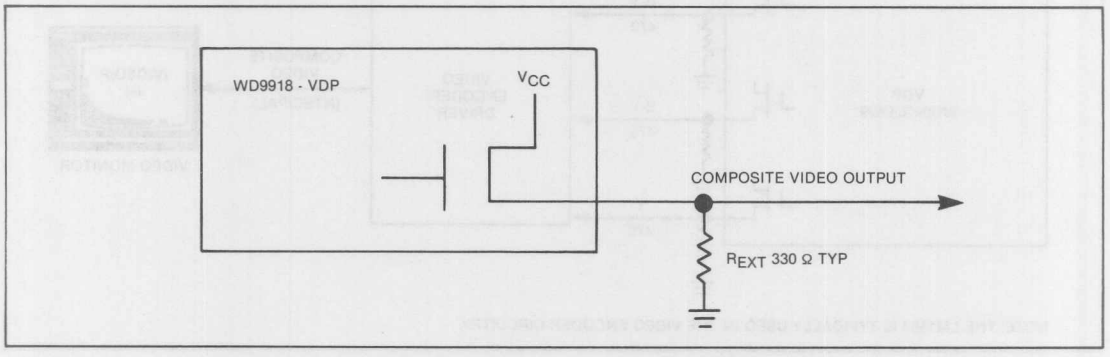


Figure 25. COMPOSITE VIDEO PULL-DOWN CIRCUIT

WD9928/9929 Monitor Interface

The Y, R-Y and B-Y output signals require external encoder circuitry to drive a video color monitor; an R-G-B matrix circuitry is required to drive R-G-B color monitors. The Y output signal contains all necessary horizontal and vertical synchronization signals as well as luminance while the R-Y and B-Y signals contain the unmodulated chrominance information and are used in the NTSC and PAL systems to modulate two carriers in quadrature. The internal output buffer devices on these pins are source-follower MOS transistors that require an external pull-down resistor to V_{SS}, as shown in Figure 26. A 330 ohm resistor is recommended.

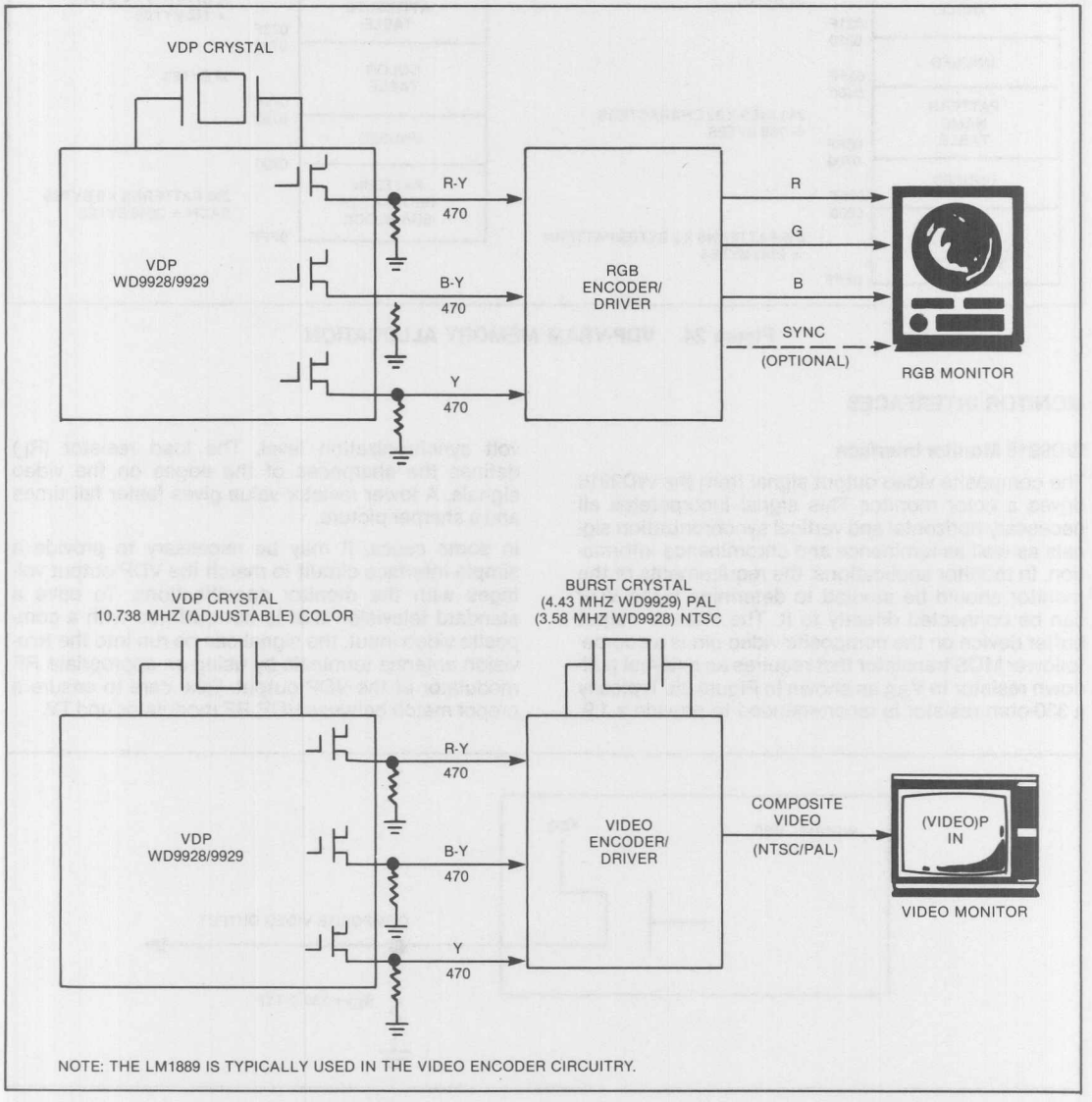


Figure 26. USE OF WD9928/9929 WITH DIFFERENT MONITORS

WD9918 EXTERNAL VDP OPERATION

The external VDP interface allows cascading multiple VDPs. Figures 27 and 28 illustrate cascading two VDPs. Note that the VDPs must be reset by a common reset source to assure synchronization on an open loop basis. This reset source should have fast edges so that rise and fall times are less than 30 ns. Occasionally, synchronization is not obtained after reset, in which case, reset should be reapplied.

The video matching circuit ensures that the video signal of external VDP is biased correctly and of the proper amplitude. This ensures the luminance levels of the external and VDP colors are matched and external VDP video does not bleed through into the composite video output of the first VDP. The internal circuit assures that a perfect match results if the external video is of the same amplitude as the composite video of the VDP and its dc level is increased by a MOS threshold voltage (typically 0.7 volts). This adjustment can be varied to change the relative luminance levels of the two video signals and thus modify the picture appearance.

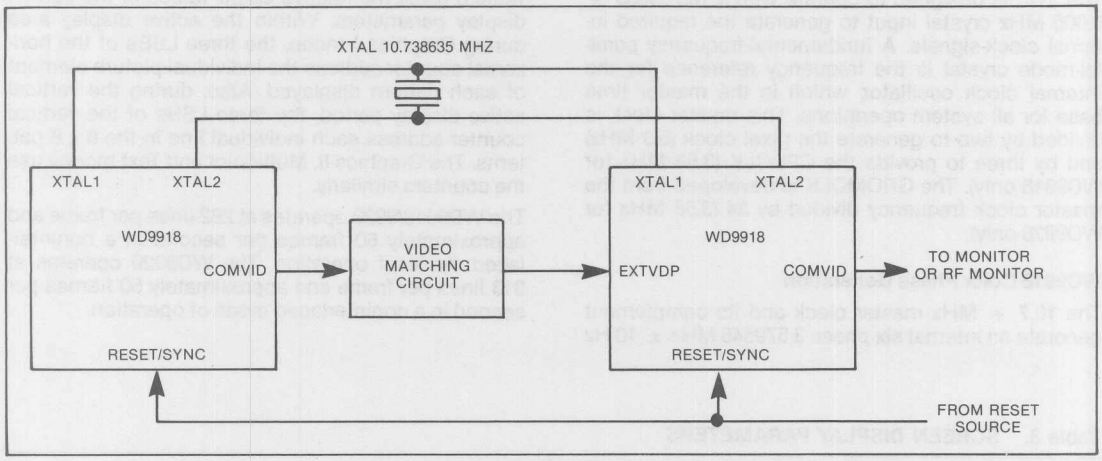


Figure 27. CASCADING TWO WD9918 VDPS

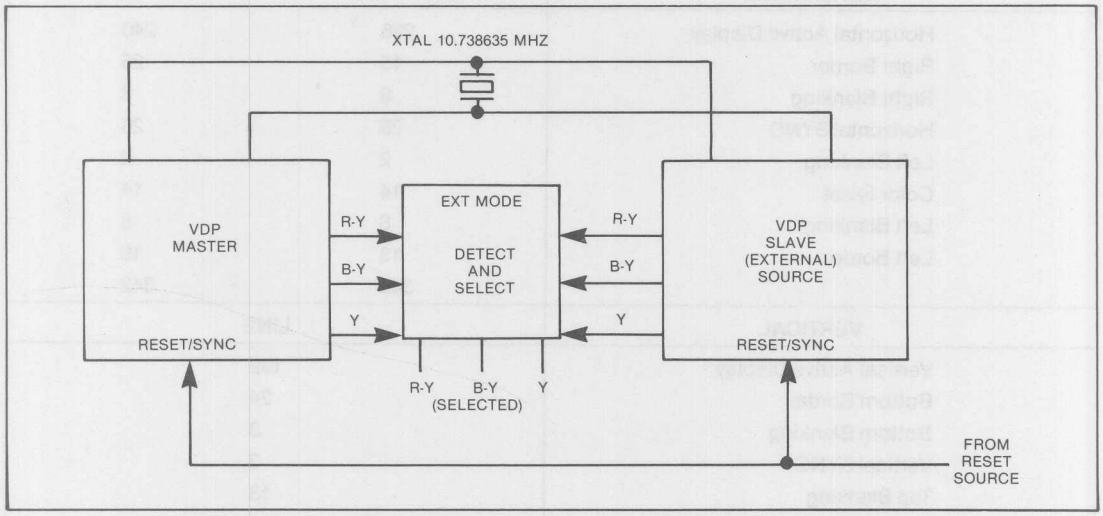


Figure 28. CASCADING TWO WD9918/9929 VDPS

For the External VDP input plane to be visible, the External VDP Enable bit in VDP Register 0 (EXVID) should be set to a 1. The backdrop color (VDP Register 7, lower 4 bits) should be set to transparent (0). For the external VDP plane to show through at a given spot on the screen, the pattern color at that spot should be transparent, and all sprites should not be in the way (alternatively, a sprite that was in the way could be made transparent in color). Note that the external VDP feature can be used in either Graphics I, Graphics II, Text, or Multicolor mode.

OSCILLATOR AND CLOCK GENERATION

The VDP is designed to operate with a 10.738635 ± 0.005 MHz crystal input to generate the required internal clock-signals. A fundamental-frequency parallel-mode crystal is the frequency reference for the internal clock oscillator, which is the master time base for all system operations. This master clock is divided by two to generate the pixel clock (5.3 MHz) and by three to provide the CPUCLK (3.58 MHz for WD9918 only). The GROMCLK is developed from the master clock frequency divided by 24 (3.58 MHz for WD9928 only).

WD9918 Color Phase Generation

The 10.7 + MHz master clock and its complement generate an internal six-phase 3.579545 MHz ± 10 Hz clock to provide the video color signals and the color burst reference used in developing the composite video output signal. While the VDP signals are not exact equivalents to the standard NTSC colors, the differences can easily be adjusted with the color and tint controls of the target color monitor.

Video Sync and Control Generation

Decoding the outputs of the horizontal and vertical counters generates the horizontal and vertical control signals. The pixel clock drives the horizontal counter which in turn increments the vertical counter.

Table 8 gives the relative count values of the screen display parameters. Within the active display area during Graphics I mode, the three LSBs of the horizontal counter address the individual picture element of each pattern displayed. Also, during the vertical active display period, the three LSBs of the vertical counter address each individual line in the 8 x 8 patterns. The Graphics II, Multicolor and Text modes use the counters similarly.

The WD9918/9929 operates at 262 lines per frame and approximately 60 frames per second in a noninterlaced mode of operation. The WD9929 operates at 313 lines per frame and approximately 50 frames per second in a noninterlaced mode of operation.

Table 8. SCREEN DISPLAY PARAMETERS

PARAMETER	PIXEL CLOCK CYCLES	
HORIZONTAL	PATTERN OR MULTICOLOR	TEXT
Horizontal Active Display	256	240
Right Border	15	25
Right Blanking	8	8
Horizontal SYNC	26	26
Left Blanking	2	2
Color Burst	14	14
Left Blanking	8	8
Left Border	13	19
	342	342
VERTICAL	**LINE**	
Vertical Active Display	192	
Bottom Border	24	
Bottom Blanking	3	
Vertical SYNC	3	
Top Blanking	13	
Top Border	27	
	262	

WD9918/9928/9929 Crystals

Crystals for the WD9918/9928/9929 can be purchased from the following:

NDK
10080 North Wolfe Rd., Suite 220
Cuppertino, CA 95014
Telephone: (408) 255-0831
Telex: 352057

CTS Knights, Inc.
400 Reiman Ave.
Sandwich, Ill. 60548
Telephone: (815) 786-8411

WD9918/9928/9929 ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS OVER OPERATING FREE-AIR TEMPERATURE RANGE (unless otherwise noted)*

Supply voltage, V_{CC} . . . . . – 0.3 to 20V
All input voltages . . . . . – 0.3 to 20V
Output voltage . . . . . – 2 to 7V
Continuous power dissipation . . . . . 1.3 W
Operating free-air temperature range . . . 0°C to 70°C
Storage temperature range . . . . . – 55°C to + 150°C

*Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the Recommended Operating Conditions section of this specification is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS*

PARAMETER	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.75		5.25	V
Supply voltage, V_{SS}		0		V
Input Voltage V_I, RESET/SYNC pin				
SYNC active	10		12	V
$\overline{\text{RESET}}$ active			0.6	V
SYNC and RESET inactive	3		6	V
High-level input, V_{IH}				
XTAL1, XTAL2	2.75			V
All other inputs	2.2			V
Input voltage, V_I, EXT VDP pin (WD9918 only)				
SYNC level		2.6		V
White level		3.7		V
Black level		3		V
Low-level input voltage, V_{IL}			0.8	V
Operating free-air temperature, T_A	0		70	°C

*All voltage values are with respect to V_{SS}.

ELECTRICAL CHARACTERISTICS OVER FULL RANGES OF RECOMMENDED OPERATING CONDITIONS (unless otherwise noted)

WD9918/9928/9929

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{OH}	High-level Output voltage $\overline{RAS}$, $\overline{CAS}$, R/$\overline{W}$	I_{OH} = 400 μA	2.7	3.4		V
	All other outputs	I_{OH} = 400 μA	2.4	3.2		V
V_{OL}	Low-level Output voltage CPU data	I_{OL} = 1.2 mA		0.3	0.6	V
	DRAM interface	I_{OL} = 800 μA			0.6	V
I_{OZH}	Off-state output current high-level voltage applied, D0-D7 outputs	V_O = 5.25 V		1	100	μA
I_{OZL}	Off-state output current high-level voltage applied, D0-D7 outputs	V_O = 0.4 V		1	– 100	μA
I_{IH}	High-level input current	V_I = 5.25 V, all other pins at 0 V			10	μA
I_{IL}	Low-level input current	V_I = 0 V, all other pins at 0 V			– 10	μA

WD9918 Only (Figure 29)

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	NOM	MAX	UNIT
V_{white}	Video voltage level of white, COMVID	R_L = 470 Ω	2.8	3.0	3.2 V	
V_{black}	Video voltage level of black (blank), COMVID	R_L = 470 Ω	2.1	2.3	2.5 V	
V_{sync}	Video voltage level of sync, COMVID	R_L = 470 Ω	1.85	2.0	2.1 V	

† All typical values are at V_{CC} = 5.25 V, T_A = 25°C.

ELECTRICAL CHARACTERISTICS OVER FULL RANGES OF RECOMMENDED OPERATING CONDITIONS (unless otherwise noted) (Continued)

WD9928/9929 Only (Figure 29)

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	NOM	MAX	UNIT
V_{white}	Video voltage level of white, Y, R-Y, B-Y outputs	R_L = 470 Ω	2.5	3	3.6	V
V_{black}	Video voltage level of black (blank), Y, R-Y, B-Y outputs	R_L = 470 Ω	1.6	2.3	2.5	V
V_{sync}	Video voltage level of sync, Y output	R_L = 470 Ω	1.2	1.8	2	V

WD9929 Only

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{PS}	Color burst video voltage level with respect to V no color	R-Y output		0.25		V
V_{neg}	Color burst video voltage level with respect to V no color	B-Y output		– 0.25		V

WD9918/9928/9929 (Figure 30)

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	NOM	MAX	UNIT
	Video voltage difference, white-black, Y, R-Y, B-Y outputs		0.7	1.0		V
I_{CC}	Average supply current from V_{CC}	T_A = 25°C		200	250	mA
C_i	Input capacitance D0-D7 All other inputs	unmeasured f = 11 MHz, pins at 0 V			20 10 10	pF
C_o	Output capacitance	unmeasured f = 11 MHz, pins at 0 V			20	pF

† All typical values are at V_{CC} = 5.25 V, T_A = 25°C.

TIMING REQUIREMENTS OVER FULL RANGES OF RECOMMENDED OPERATING CONDITIONS (WD9918/9928/9929)

CPU - VDP Interface (Figures 31 and 32)

SYMBOL	PARAMETER	MIN	NOM	MAX	UNIT
$t_{su(A-RL)}$	Address setup time before CSR low		0		ns
$t_{su(A-WL)}$	Address setup time before CSW low		30		ns
$t_{h(WL-A)}$	Address hold time after CSW low		30		ns
$t_{su(D-WH)}$	Data setup time before CSW high		100		ns
$t_{h(WH-D)}$	Data hold time after CSW high		30		ns
$t_{w(WL)}$	Pulse width, CSW low		200		ns
$t_{w(CS-H1)}$	Pulse width, chip select high (requesting memory access)		8		μs
$t_{w(CS-H2)}$	Pulse width, chip select high (not requesting memory access)		2		μs

VDP - VRAM Interface (Figures 33 and 34)

SYMBOL	PARAMETER	MIN	NOM	MAX	UNIT
t_c	Memory read or write cycle time	372			ns
$t_{su(D-CH)}$	Input data setup time before CAS high	60			ns
$t_{h(CH-D)}$	Input data hold time after CAS high	0			ns

External Clock Source (Figure 35)

SYMBOL	PARAMETER	MIN	NOM	MAX	UNIT
f_{ext}	External source frequency	10.738098	10.738635	10.739172	MHz
t_r/t_f	External source rise/fall time		10	15	ns
t_{wH}	External source high-level pulse width	42	47	52	ns
t_{wL}	External source low-level pulse width	42	47	52	ns
t_{pD}	External source phase delay from XTAL1 falling edge to XTAL2 falling edge	42	47	52	ns

SWITCHING CHARACTERISTICS OVER FULL RANGE OF RECOMMENDED OPERATING CONDITIONS (WD9918/9928/9929)

CPU - VDP Interface

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
$T_{A(CSR)}$	Data access time from CSR low	C_L = 300 pF		100	150	ns
t_{PVX}	Data disable time after CSR high	C_L = 300 pF		65	100	ns
$t_{PVX,A}$	Data invalid time from address changes	C_L = 300 pF		0		ns
f_{CPUCLK}	CPU clock output clock frequency (f_{ext} + 3)	C_l = 300 pF	3.4	3.58	3.76	MHz
$f_{GROMCLK}$	GROM clock output clock frequency (f_{ext} + 24)	C_L = 300 pF	425.12	447.5	469.88	kHz

VDP - VRAM Interface (Figures 33 and 34)

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_w	Pulse width, $\overline{CAS}$ high	C_L = 50 pF	80	100	120	ns
$t_{w(CL)}$	Pulse width, $\overline{CAS}$ low	C_L = 50 pF	220	230	250	ns
$t_{w(RH)}$	Pulse width, $\overline{RAS}$ high	C_L = 50 pF	100	125	150	ns
$t_{w(RL)}$	Pulse width, $\overline{RAS}$ low	C_L = 50 pF	190	210	230	ns
$t_{w(W)}$	Pulse width, write pulse	C_L = 50 pF	170	190	210	ns
t_{CA-CL}	Delay time, column address to $\overline{CAS}$ low	C_L = 50 pF	– 10	– 2		ns
t_{RA-RL}	Delay time, row address to $\overline{RAS}$ low	C_L = 50 pF	25	45	65	ns
t_{d-WL}	Delay time, data to R/$\overline{W}$ low	C_L = 50 pF	0	6	20	ns
t_{WH-CL}	Delay time, R/$\overline{W}$ high to $\overline{CAS}$ low	C_L = 50 pF	25	50	75	ns
t_{W-CH}	Delay time, R/$\overline{W}$ low to $\overline{CAS}$ high	C_L = 50 pF	120	140	160	ns
t_{W-RH}	Delay time, R/$\overline{W}$ low to $\overline{RAS}$ high	C_L = 50 pF	60	75	90	ns

SWITCHING CHARACTERISTICS OVER FULL RANGE OF RECOMMENDED OPERATING CONDITIONS (WD9918/9928/9929) (Continued)

WD9918 Composite video output (Figures 36 and 37)

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{CL-CA}	Column address valid after $\overline{CAS}$ low	C_L = 50 pF	45	65	85	ns
t_{RL-RA}	Row address valid after $\overline{RAS}$ low	C_L = 50 pF	20	25	30	ns
t_{RL-CA}	Column address valid after $\overline{RAS}$ low	C_L = 50 pF	95	110	130	ns
t_{CL-D}	Data valid after $\overline{CAS}$ low	C_L = 50 pF	240	260	280	ns
t_{RL-D}	Data valid after $\overline{RAS}$ low	C_L = 50 pF	95	110	125	ns
t_{WL-D}	Data valid after R/$\overline{W}$ low	C_L = 50 pF	135	165	195	ns
t_{CH-WL}	Read command valid after $\overline{CAS}$ high	C_L = 50 pF	0			ns
t_{CL-W}	Write command valid after $\overline{CAS}$ low	C_L = 50 pF	270	290	310	ns
t_{CH-RL}	Delay time, $\overline{CAS}$ high to $\overline{RAS}$ low	C_L = 50 pF	45	65		ns
t_{CL-RH}	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ high	C_L = 50 pF	150	170	190	ns
t_{RL-CL}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ low	C_L = 50 pF	30	40	50	ns
t_{fl}	Fall time, V_{black} to V_{sync}			10		ns
$t_{w(HS)}$	Pulse width, horizontal sync			4.84		µs
t_{rl}	Rise time, V_{sync} to V_{black}			20		ns
t_{HS-CD}	Delay time, sync to color burst			372		ns

WD9918 Composite video output (Figures 36 and 37) (CONTINUED)

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{w(CB)}$	Width, color burst			261		µs
t_{CB-LB}	Delay time, color burst to left border			1.49		µs
t_{r2}	Rise time, V_{black} to V_{white}	R_L = 470 Ω		60		ns
$t_{w(LB)}$	Left border video width	C_L = 150 pF		2.42		µs
t_{f2}	Fall time, V_{white} to V_{black}			110		ns
$t_{w(AD)}$	Width of active display area			47.68		µs
$t_{w(RB)}$	Right border video width			2.79		µs
t_{RB-HS}	Delay time, right border to horizontal sync			1.49		µs
t_{VFB}	Vertical front blanking			191.1		µs
t_{VS}	Vertical sync			191.1		µs
V_{VBB}	Vertical back blanking			828		µs
t_{ABA}	Active plus border area time			18.8		ms

NOTE: Fall times depend on external pull-down resistor.

SWITCHING CHARACTERISTICS OVER FULL RANGE OF RECOMMENDED OPERATING CONDITIONS (WD9918/9928/9929) (Continued)

WD9928/9929 Y, R-Y, B-Y outputs (Figures 38 through 41)

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{f3}	Fall time, V_{black} to V_{sync}			100		ns
$t_{w(HSI)}$	Pulse width, horizontal sync			4.84		µs
t_{r3}	Rise time, V_{sync} to V_{black}			150		ns
$t_{w(BP)}$	Width, back porch			4.47		µs
$t_{w(LBI)}$	Width, left border			2.8		µs
$t_{w(P)}$	Pulse width, pixel			186.24		ns
$t_{w(horz)}$	Width, horizontal line			63.695		µs
$t_{w(ADI)}$	Width, active display area			47.67		µs
t_{r4}	Rise time, V_{black} to V_{white}			75		ns
t_{r4}	Fall time, V_{white} to V_{black}			50		ns
$t_{w(RBI)}$	Width, right border			2.42		µs
$t_{w(FP)}$	Width, front porch	R_L = 470 Ω		1.49		µs
t_{r5}	Rise time, V no color to V pos CB	C_L = 15 pF		150		ns
$t_{w(CB1)}$	Pulse width, pos color burst			2.6		µs
t_{f5}	Fall time, V pos CB to V no color			100		ns
$t_{w(CB-LBI)}$	Delay time, pos CB to left border			1.49		µs
t_{f6}	Fall time, V no color to V neg CB			100		ns
t_{r6}	Rise time, V neg CB to V no color			150		ns
$t_{w(VSI)}$	Pulse width, vertical sync			465		ns
t_{VFBI}	Vertical front blanking			191.09		µs
t_{VSI}	Vertical sync			191.09		µs
t_{VBBI}	Vertical back blanking			828.04		µs
t_{ABAI}	Active area plus border area total			18.70		mS
	Vertical time			19.91		mS

NOTE: Fall times depend on external pull-down resistor.

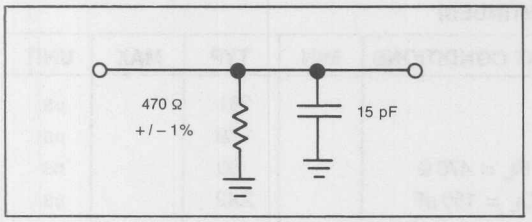


Figure 29.
LOAD CIRCUIT FOR COMVID (ALL DEVICES)
AND R-Y, Y, B-Y SWITCHING CHARACTERISTICS
(WD9928/9929)

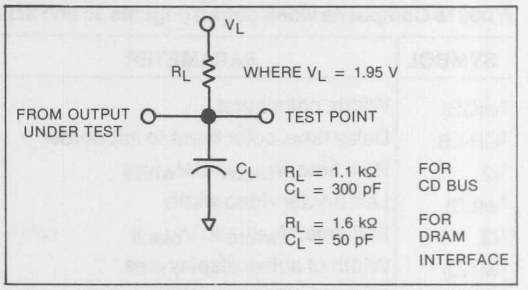


Figure 30. LOAD CIRCUITS FOR ALL OUTPUTS
EXCEPT COMVID, R-Y, Y, B-Y

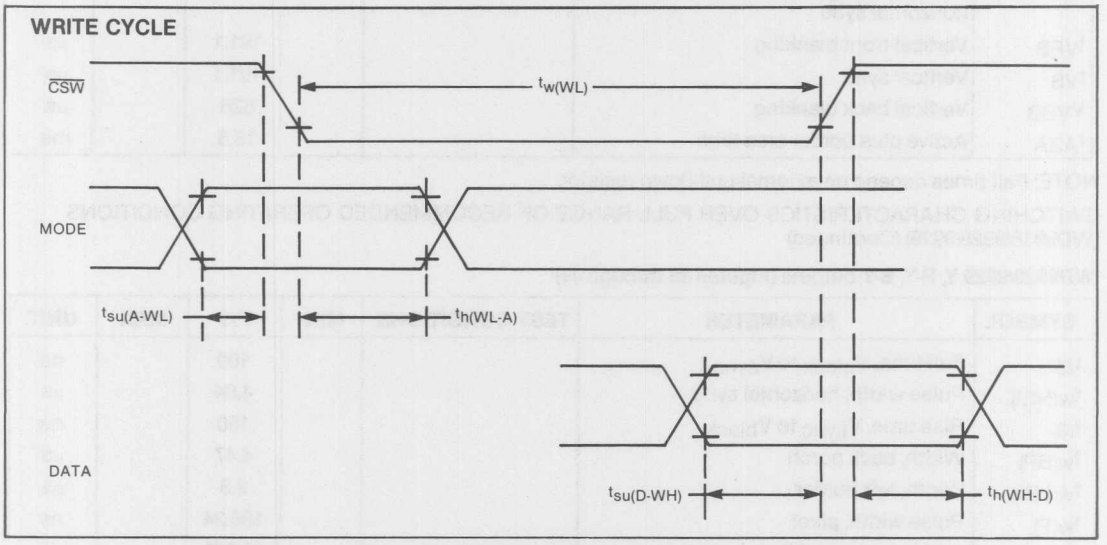


Figure 31. CPU - VDP WRITE CYCLE FOR WD9918/9928/9929

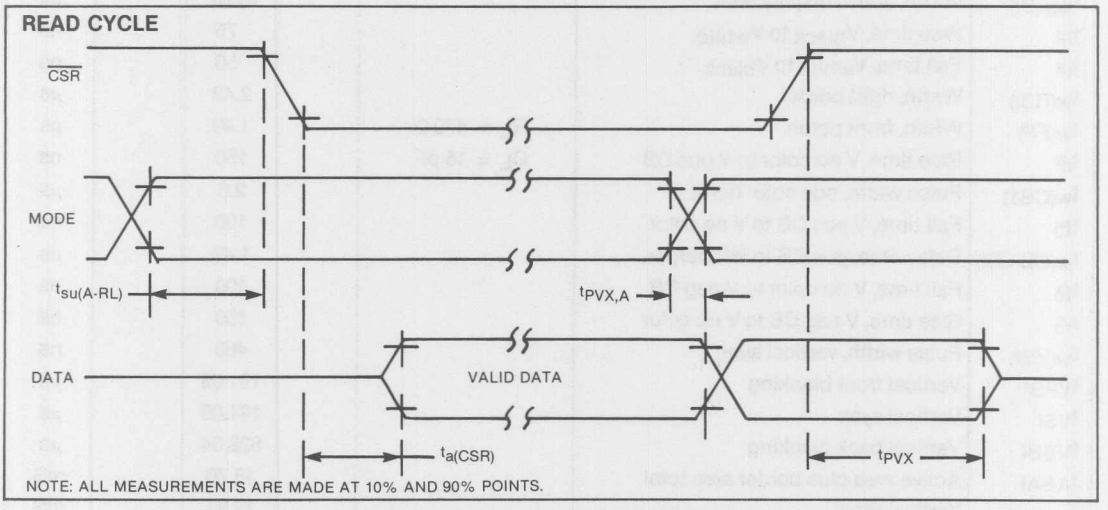


Figure 32. CPU - VDP READ CYCLE FOR WD9918/9928/9929

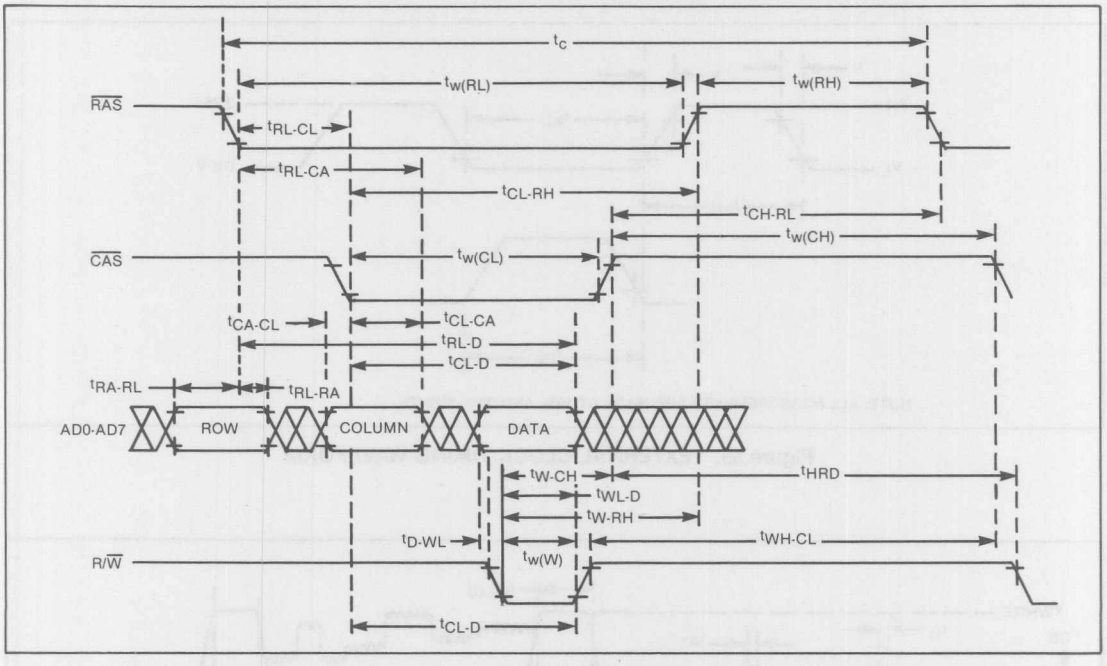


Figure 33. VRAM WRITE CYCLE

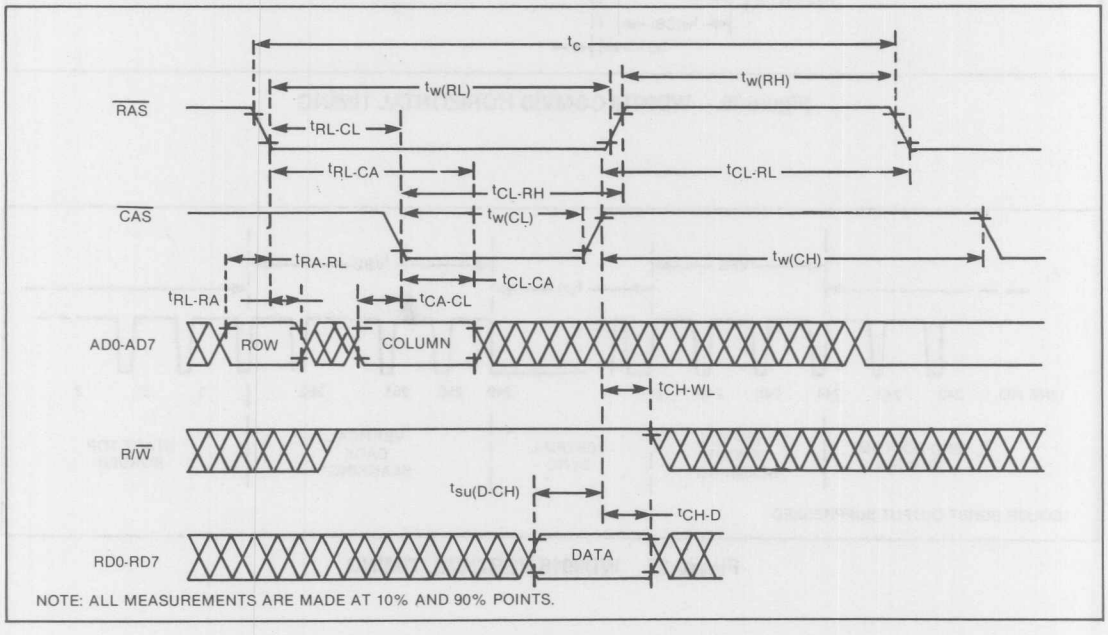


Figure 34. VRAM READ CYCLE

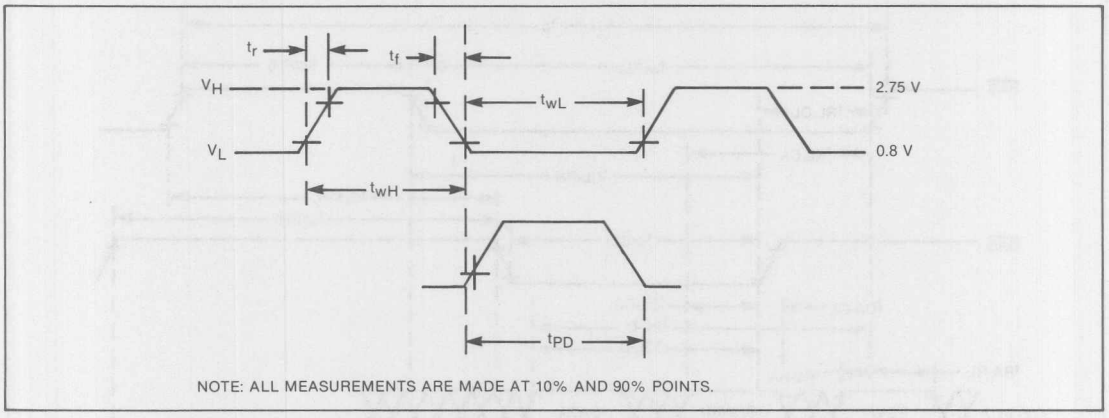


Figure 35. EXTERNAL CLOCK TIMING WAVEFORM

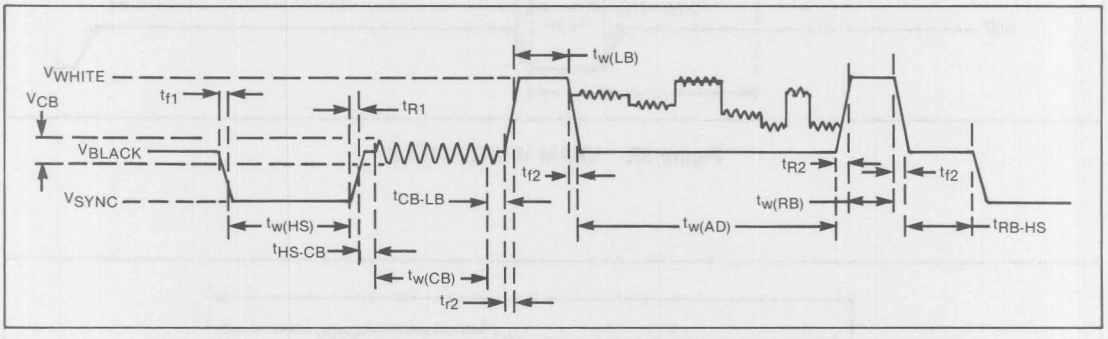


Figure 36. WD9918 COMVID HORIZONTAL TIMING

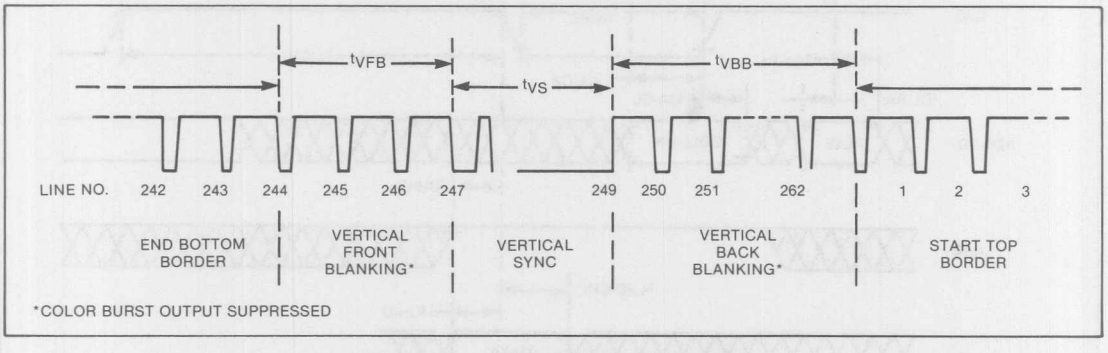


Figure 37. WD9918 VERTICAL TIMING

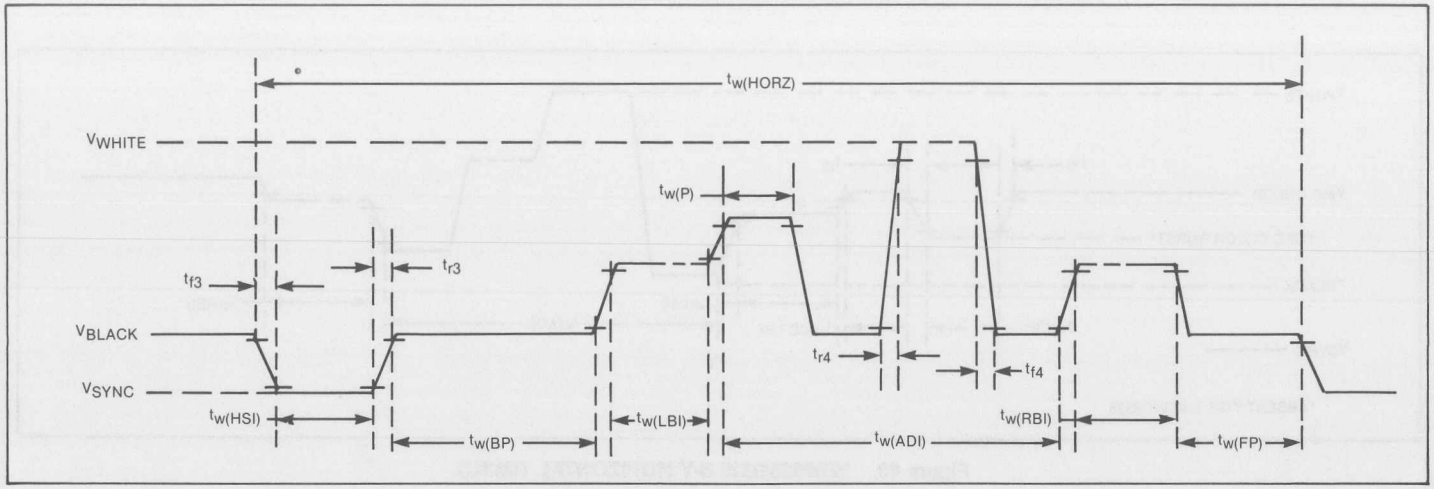


Figure 38. WD9928/9929 Y HORIZONTAL TIMING

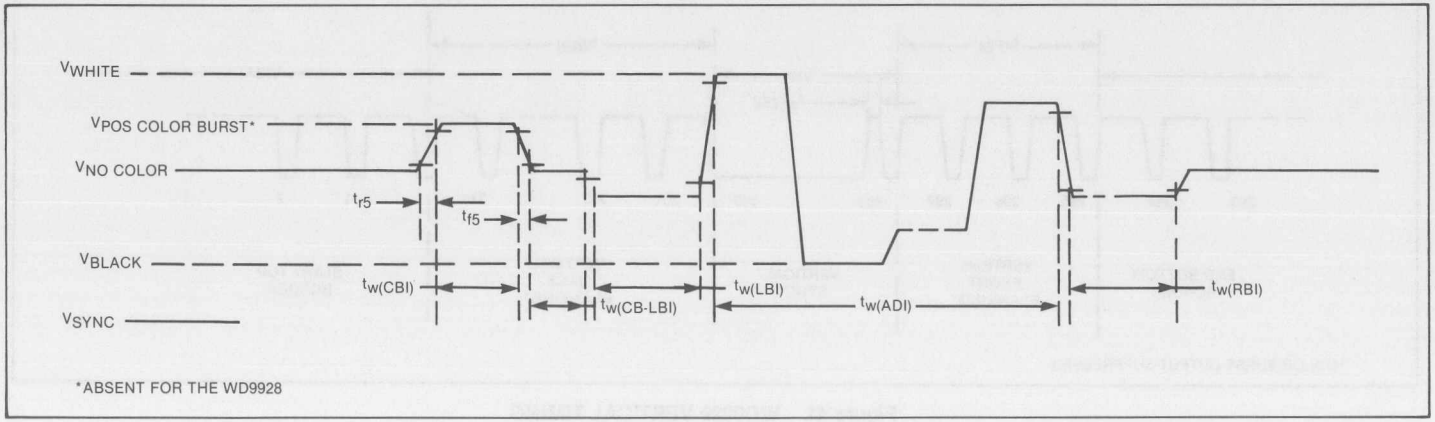


Figure 39. WD9928/9929 R-Y HORIZONTAL TIMING

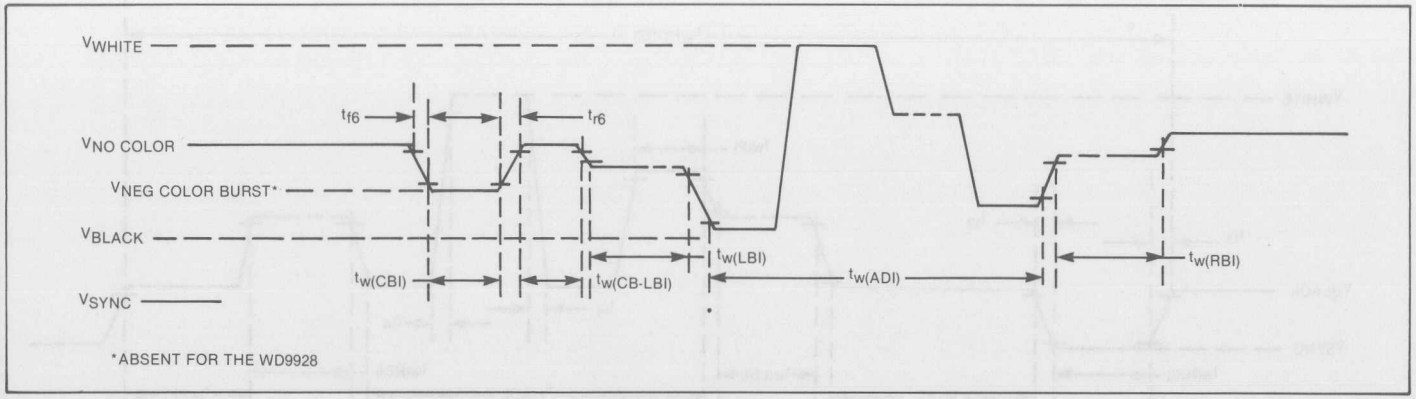


Figure 40. WD9928/9929 B-Y HORIZONTAL TIMING

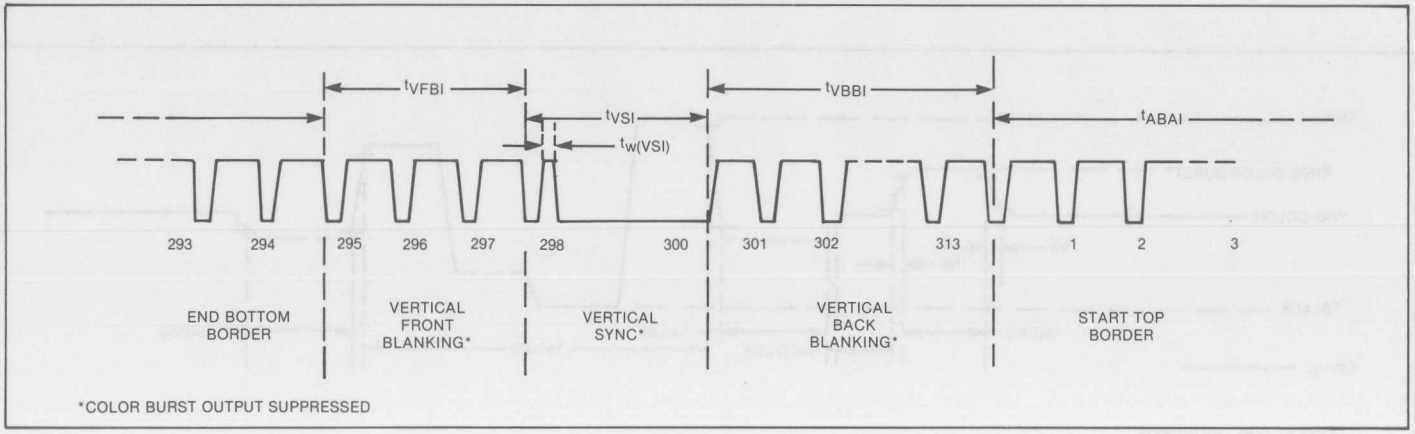


Figure 41. WD9929 VERTICAL TIMING

See page 429 for ordering information.

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CORPORATION

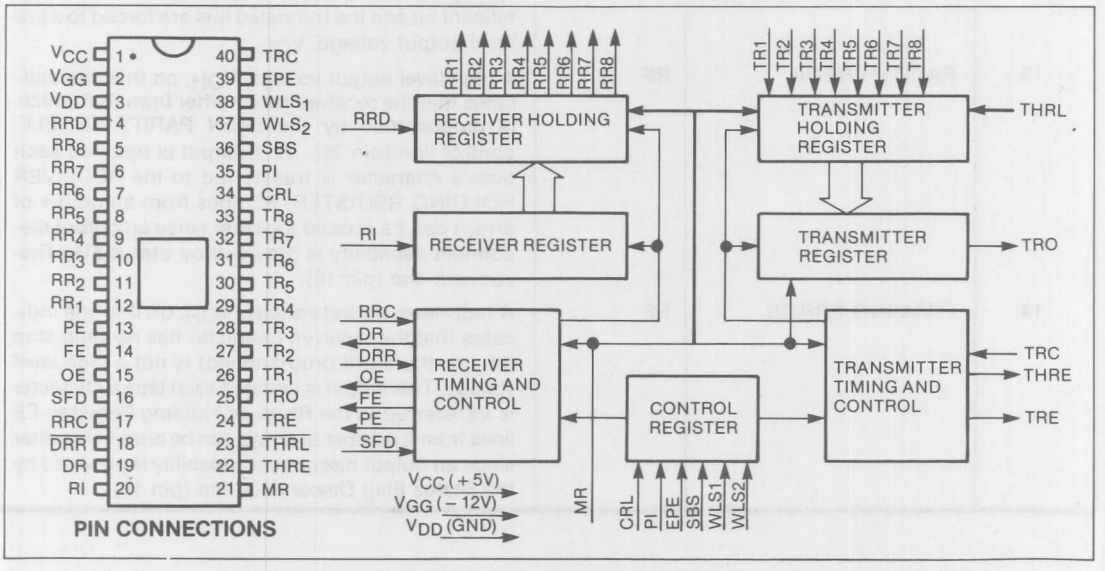
TR1402/TR1602
Universal Asynchronous Receiver/Transmitter (UART)

FEATURES

- FULL DUPLEX OR HALF DUPLEX OPERATION
- AUTOMATIC INTERNAL SYNCHRONIZATION OF DATA AND CLOCK
- AUTOMATIC START BIT GENERATION
- EXTERNALLY SELECTABLE
  Word Length
  Baud Rate
  Even/Odd Parity (Receiver/Verification — Transmitter/Generation)
  Parity Inhibit
  One, One and One-Half, or Two Stop Bit Generation (1½ at 5 Bit Level for TR1602)
- AUTOMATIC DATA RECEIVED/TRANSMITTED STATUS GENERATION
  Transmission Complete
  Buffer Register Transfer Complete
  Received Data Available
  Parity Error
  Framing Error
  Overrun Error
- BUFFERED RECEIVER AND TRANSMITTER REGISTERS
- THREE-STATE OUTPUTS
  Receiver Register Outputs
  Status Flags
- TTL COMPATIBLE
- PULL-UP RESISTORS ON ALL INPUTS

APPLICATIONS

- PERIPHERALS
- TERMINALS
- MINI COMPUTERS
- FACSIMILE TRANSMISSION
- MODEMS
- CONCENTRATORS
- ASYNCHRONOUS DATA MULTIPLEXERS
- CARD AND TAPE READERS
- PRINTERS
- DATA SETS
- CONTROLLERS
- KEYBOARD ENCODERS
- REMOTE DATA ACQUISITION SYSTEMS
- ASYNCHRONOUS DATA CASSETTES



PIN CONNECTIONS

TR1602/TR1402 BLOCK DIAGRAM

convert parallel data to a serial data format on the transmit side, and converts a serial data format to parallel data on the receive side.

The serial format in order of transmission and reception is a start bit, followed by five to eight data bits, a parity bit (if selectedl) and one, one and one-half (1602 bit data format only) or two stop bits.

Three types of error conditions are available on each received character: parity error, framing error bit time. The receiver clock is also used to sample in the center of the serial data bits to allow for line distortion.

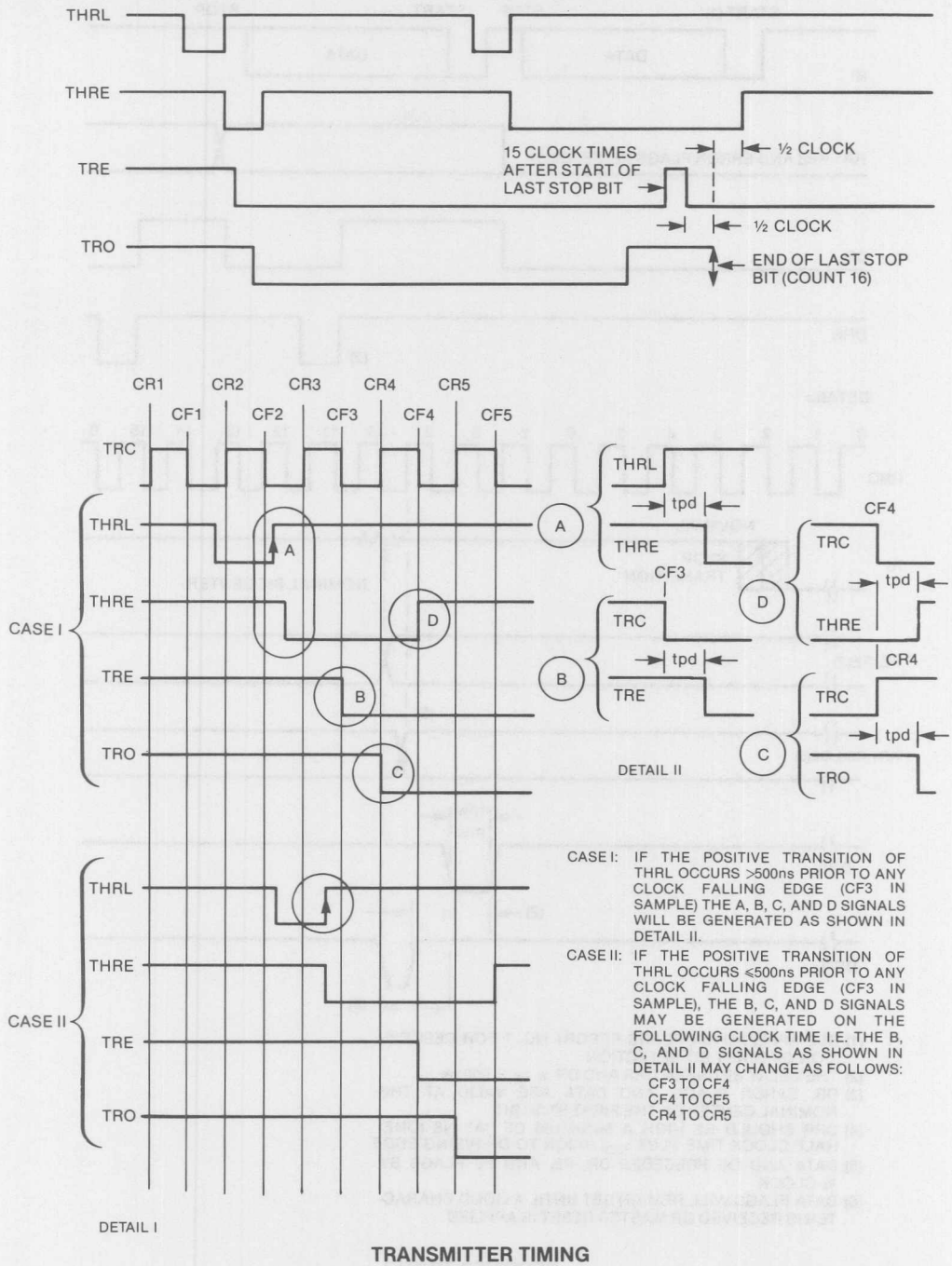
Both transmitter and receiver are double buffered allowing a one character time maximum between a data read or write. Independent handshake lines for receiver and transmitter are also included. All inputs and outputs are TTL compatible with three-state outputs available on the receiver, and error flags for bussing multiple devices.

PIN DEFINITIONS

PIN NUMBER	NAME	SYMBOL	FUNCTION
1	POWER SUPPLY	VSS	+5 volts supply
2	POWER SUPPLY	V_{GG}	-12 volts supply
3	POWER SUPPLY	V_{DD}	Ground = 0V
4	RECEIVER REGISTER DISCONNECT	RRD	A high level input voltage, V_{IH}, applied to this line disconnects the RECEIVER HOLDING REGISTER outputs from the RR_{1-8} data outputs (pins 5-12).
5-12	RECEIVER HOLDING REGISTER DATA	RR_8-RR_1	The parallel contents of the RECEIVER HOLDING REGISTER appear on these lines if a low-level input voltage, V_{IL}, is applied to RRD. For character formats of fewer than eight bits received characters are right-justified with RR1 (pin 12) as the least significant bit and the truncated bits are forced to a low level output voltage, V_{OL}.
13	PARITY ERROR	PE	A high level output voltage, V_{OH}, on this line indicates that the received parity differ from that which is programmed by the EVEN PARITY ENABLE control line (pin 39). This output is updated each time a character is transferred to the RECEIVER HOLDING REGISTER. PE lines from a number of arrays can be bussed together since an output disconnect capability is provided by Status Flag Disconnect line (pin 16).
14	FRAMING ERROR	FE	A high-level output voltage, V_{OH}, on this line indicates that the received character has no valid stop bit, i.e., the bit (if programmed) is not a high level voltage. This output is updated each time a character is transferred to the Receiver Holding Register. FE lines from a number of arrays can be bussed together since an output disconnect capability is provided by the Status Flag Disconnect line (pin 16).

PIN NUMBER	NAME	SYMBOL	FUNCTION
15	OVERRUN ERROR	OE	A high-level output voltage, V_{OH}, on this line indicates that the Data Received Flag (pin 19) was not reset before the next character was transferred to the Receiver Holding Register. OE lines from a number of arrays can be bussed together since an output disconnect capability is provided by the Status Flag Disconnect line (pin 16).
16	STATUS FLAGS DISCONNECT	SFD	A high-level input voltage, V_{IH}, applied to this pin disconnects the PE, FE, OE, DR and THRE allowing them to be buss connected.
17	RECEIVER REGISTER CLOCK	RRC	The receiver clock frequency is sixteen (16) times times the desired receiver shift rate.
18	DATA RECEIVED RESET	$\overline{DRR}$	A low-level input voltage, V_{IL}, applied to this line resets the DR line.
19	DATA RECEIVED	DR	A high-level output voltage, V_{OH}, indicates that an entire character has been received and transferred to the RECEIVER HOLDING REGISTER.
20	RECEIVER INPUT	RI	Serial input data. A high-level input voltage, V_{IH}, must be present when data is not being received.
21	MASTER RESET	MR	This line is strobed to a high-level input voltage, V_{IH}, to clear the logic. It resets the TRANSMITTER and RECEIVER HOLDING REGISTERS, the TRANSMITTER REGISTER, FE, OE, PE, DR and sets TRO, THRE, and TRE to a high-level output voltage, V_{OH}.
22	TRANSMITTER HOLDING REGISTER EMPTY	THRE	A high-level output voltage, V_{OH}, on this line indicates the TRANSMITTER HOLDING REGISTER has transferred its contents to the TRANSMITTER REGISTER and may be loaded with a new character.
23	TRANSMITTER HOLDING REGISTER LOAD	$\overline{THRL}$	A low-level input voltage, V_{IL}, applied to this line enters a character into the TRANSMITTER HOLDING REGISTER. A transition from a low-level input voltage, V_{IL}, to a high-level input voltage, V_{IH}, transfers the character into the TRANSMITTER REGISTER if it is not in the process of transmitting a character. If a character is being transmitted, the transfer is delayed until its transmission is completed. Upon completion, the new character is automatically transferred simultaneously with the initiation of the serial transmission of the new character.
24	TRANSMITTER REGISTER EMPTY	TRE	A high-level output voltage, V_{OH}, on this line indicates that the TRANSMITTER REGISTER has completed serial transmission of a full character including STOP bit(s). It remains at this level until the start of transmission of the next character.

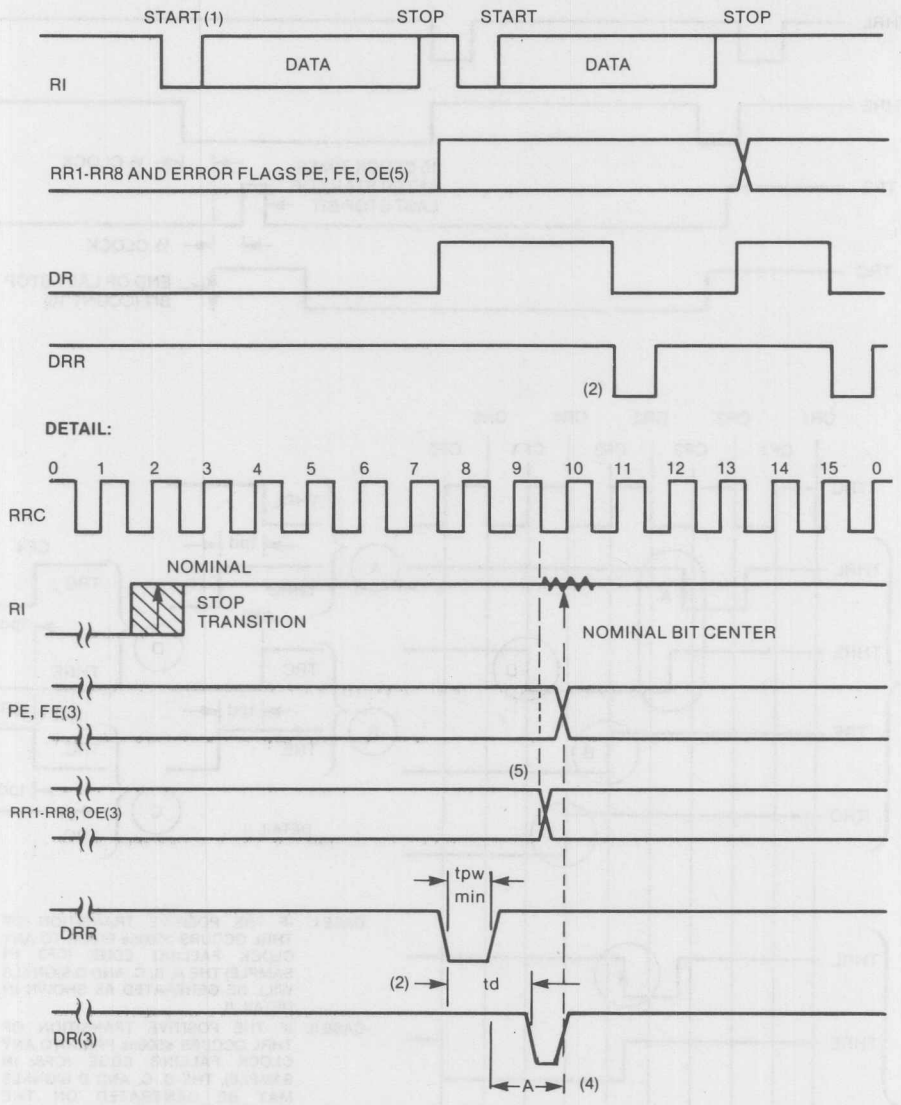
PIN NUMBER	NAME	SYMBOL	FUNCTION
25	TRANSMITTER REGISTER OUTPUT	TRO	The contents of the TRANSMITTER REGISTER (START bit, DATA bits, PARITY bit, and STOP bits) are serially shifted out on this line. When no data is being transmitted, this line will remain at a high-level output voltage, V_{OH}. Start of transmission is defined as the transition of the START bit from a high-level output voltage VOH, to a low-level output voltage, V_{OL}.
26-33	TRANSMITTER REGISTER DATA INPUTS	TR_1-TR_8	The character to be transmitted is loaded into the TRANSMITTER HOLDING REGISTER on these lines with the THRL Strobe. If a character of less than 8 bits has been selected (by WLS_1 and WLS_2), the character is right justified to the least significant bit, TR1, and the excess bits are disregarded. A high-level input voltage, V_{IH}, will cause a high-level output voltage, V_{OH}, to be transmitted.
34	CONTROL REGISTER LOAD	CRL	A high-level input voltage, V_{IH}, on this line loads the CONTROL REGISTER with the control bits (WLS_1, WLS_2, EPE, PI, SBS). This line may be strobed or hard wired to a high-level input voltage, V_{IH}.
35	PARITY INHIBIT	PI	A high-level input voltage, V_{IH}, on this line inhibits the parity generation and verification circuits and will clamp the PE output (pin 13) to V_{OL}. If parity is inhibited, the STOP bit(s) will immediately follow the last data bit of transmission.
36	STOP BIT(S) SELECT	SBS	This line selects the number of STOP bits to be transmitted after the parity bit. A high-level input voltage V_{IH}, on this line selects two STOP bits, and a low-level input voltage, V_{IL}, selects a single STOP bit. The TR1602 generates 1½ stop bits when word length is 5 bits and SBS is High VIH.
37-38	WORD LENGTH SELECT	WLS_1-WLS_2	These two lines select the character length (exclusive of parity) as follows: WLS_2 / WLS_1 / Word Length V_{IL} / V_{IL} / 5 bits V_{IL} / V_{IH} / 6 bits V_{IH} / V_{IL} / 7 bits V_{IH} / V_{IH} / 8 bits
39	EVEN PARITY ENABLE	EPE	This line determines whether even or odd PARITY is to be generated by the transmitter and checked by the receiver. A high-level input voltage, V_{IH}, selects even PARITY and a low-level input voltage, V_{IL}, selects odd PARITY.
40	TRANSMITTER REGISTER	TRC	The transmitter clock frequency is sixteen (16) times the desired transmitter shift rate.



TRANSMITTER TIMING

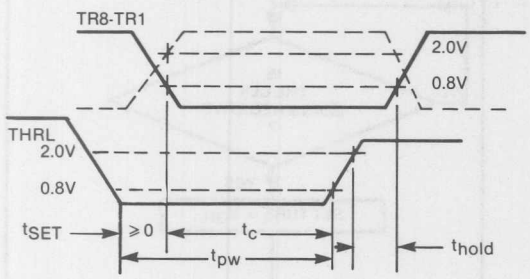
CASE I: IF THE POSITIVE TRANSITION OF THRL OCCURS >500ns PRIOR TO ANY CLOCK FALLING EDGE (CF3 IN SAMPLE) THE A, B, C, AND D SIGNALS WILL BE GENERATED AS SHOWN IN DETAIL II.

CASE II: IF THE POSITIVE TRANSITION OF THRL OCCURS ≤500ns PRIOR TO ANY CLOCK FALLING EDGE (CF3 IN SAMPLE), THE B, C, AND D SIGNALS MAY BE GENERATED ON THE FOLLOWING CLOCK TIME I.E. THE B, C, AND D SIGNALS AS SHOWN IN DETAIL II MAY CHANGE AS FOLLOWS:
CF3 TO CF4
CF4 TO CF5
CR4 TO CR5

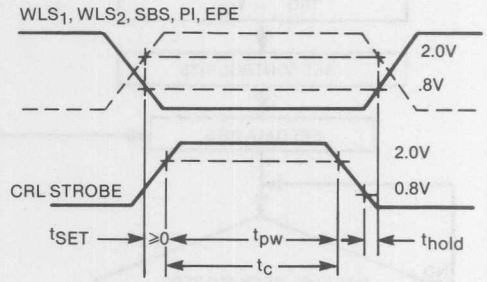


(1) SEE APPLICATION FLAGS REPORT NO. 1 FOR DESCRIPTION OF START BIT DETECTION
(2) THE DELAY BETWEEN DRR AND DR = t_d = 500 ns
(3) DR. ERROR FLAGS, AND DATA ARE VALID AT THE NOMINAL CENTER OF THE FIRST STOP BIT
(4) DRR SHOULD BE HIGH A MINIMUM OF "A" NS (ONE-HALF CLOCK TIME PLUS t_{pd}) PRIOR TO DR RISING EDGE
(5) DATA AND OE PRECEDES DR, PE, AND FE FLAGS BY ½ CLOCK
(6) DATA FLAGS WILL REMAIN SET UNTIL A GOOD CHARACTER IS RECEIVED OR MASTER RESET IS APPLIED.

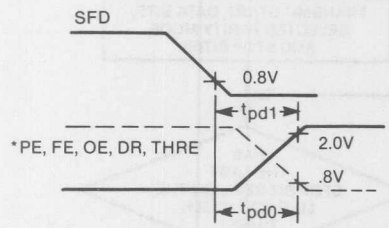
RECEIVER TIMING



DATA INPUT LOAD CYCLE

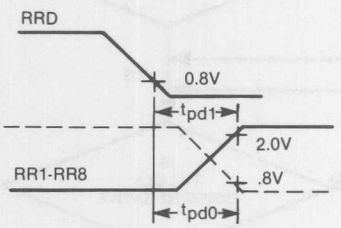


CONTROL REGISTER LOAD CYCLE



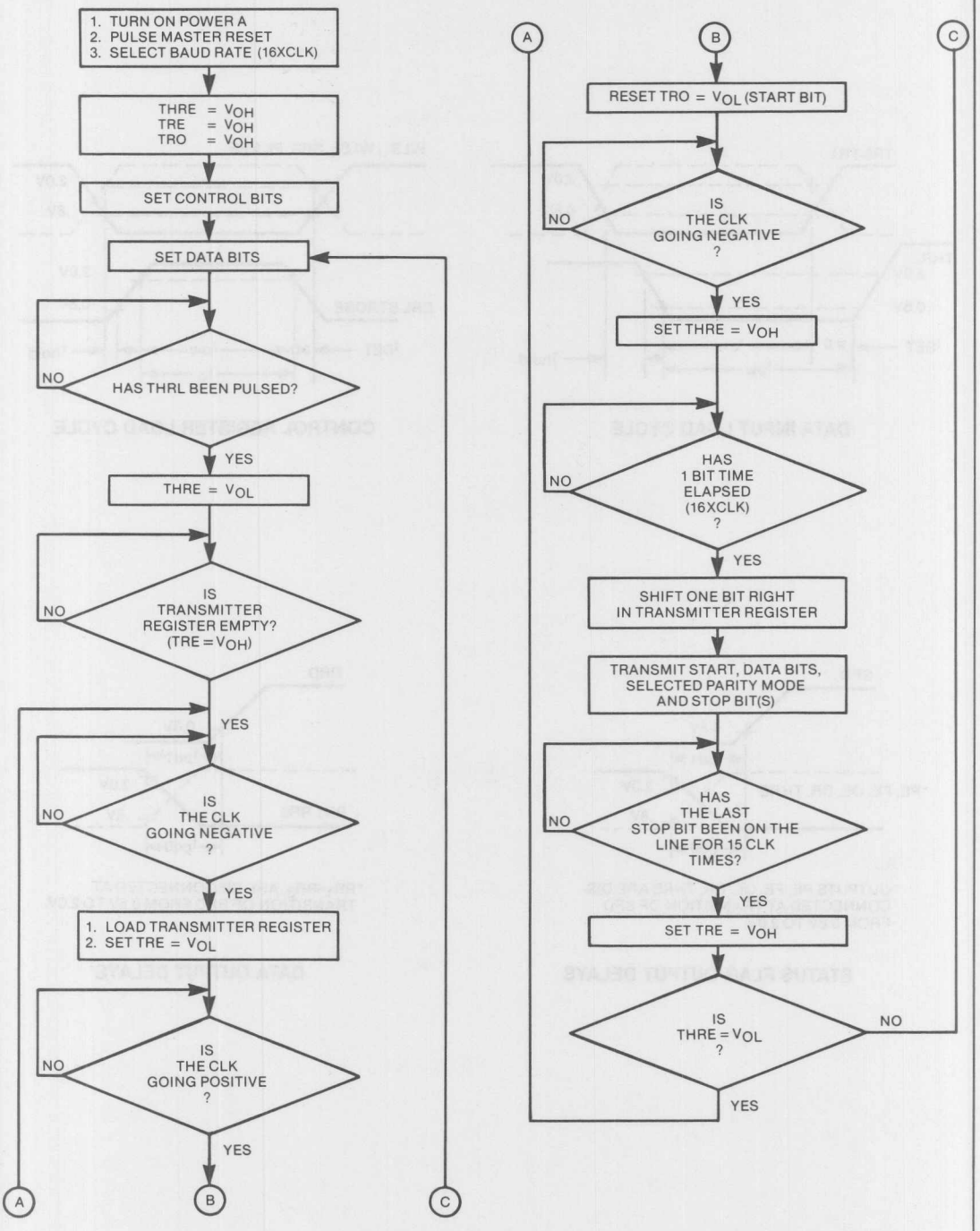
*OUTPUTS PE, FE, OE, DR, THRE ARE DISCONNECTED AT TRANSITION OF SFD FROM 0.8V TO 2.0V.

STATUS FLAG OUTPUT DELAYS

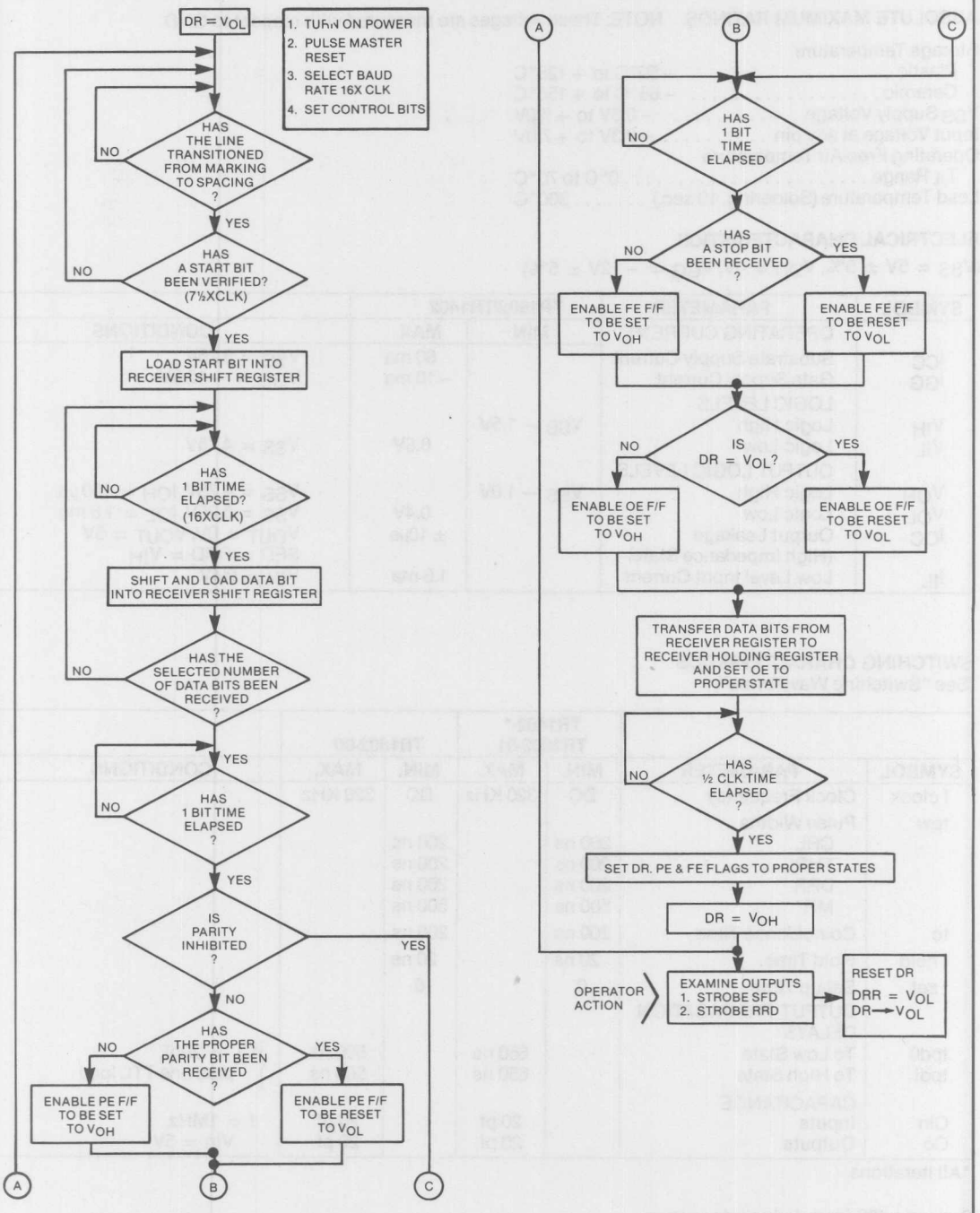


*RR_1–RR_3, ARE DISCONNECTED AT TRANSITION OF RRD FROM 0.8V TO 2.0V.

DATA OUTPUT DELAYS



TRANSMITTER FLOW CHART



RECEIVER FLOW CHART

ABSOLUTE MAXIMUM RATINGS NOTE: These voltages are measured with respect to GND

Storage Temperature
Plastic ..... −55°C to +125°C
Ceramic ..... −65°C to +150°C
V_{SS} Supply Voltage ..... −0.3V to +7.0V
Input Voltage at any pin ..... −0.3V to +7.0V
Operating Free-Air Temperature
T_A Range ..... 0°C to 70°C
Lead Temperature (Soldering, 10 sec.) ..... 300°C

ELECTRICAL CHARACTERISTICS
(V_{SS} = 5V ± 5%, V_{DD} = 0V, V_{GG} = −12V ± 5%)

SYMBOL	PARAMETER	TR1602/TR1402		
	OPERATING CURRENT	MIN	MAX	CONDITIONS
I_{CC}	Substrate Supply Current		60 ma	V_{SS} = 5.25V
I_{GG}	Gate Supply Current		−10 ma	V_{GG} = −12.6V
	LOGIC LEVELS			
V_{IH}	Logic High	V_{SS} — 1.5V		
V_{IL}	Logic Low		0.8V	V_{SS} = 4.75V
	OUTPUT LOGIC LEVELS			
V_{OH}	Logic High	V_{SS} — 1.0V		V_{SS} = 4.75V, I_{OH} = 100 μa
V_{OL}	Logic Low		0.4V	V_{SS} = 5.25V, I_{OL} = 1.6 ma
I_{OC}	Output Leakage (High Impedance State)		± 10μa	V_{OUT} = 0V, V_{OUT} = 5V SFD = RRD = V_{IH}
I_{IL}	Low Level Input Current		1.6 ma	V_{IN} = 0.4V

SWITCHING CHARACTERISTICS
(See "Switching Waveforms")

		TR1402-* TR1602-01		TR1602-00		
SYMBOL	PARAMETER	MIN.	MAX.	MIN.	MAX.	CONDITIONS
f clock	Clock Frequency	DC	320 KHz	DC	320 KHz	
tpw	Pulse Widths					
	CRL	200 ns		200 ns		
	THRL	200 ns		200 ns		
	DRR	200 ns		200 ns		
	MR	500 ns		500 ns		
tc	Coincidence Time	200 ns		200 ns		
t hold	Hold Time	20 ns		20 ns		
t set	Set-up Time	0		0		
	OUTPUT PROPAGATION DELAYS					
tpd0	To Low State		650 ns		500 ns	C_L = 20pf,
tpdl	To High State		650 ns		500 ns	plus one TTL load
	CAPACITANCE					
Cin	Inputs		20 pf		20 pf	f = 1MHz,
Co	Outputs		20 pf		20 pf	Vin = 5V

*All iterations

See page 429 for ordering information.

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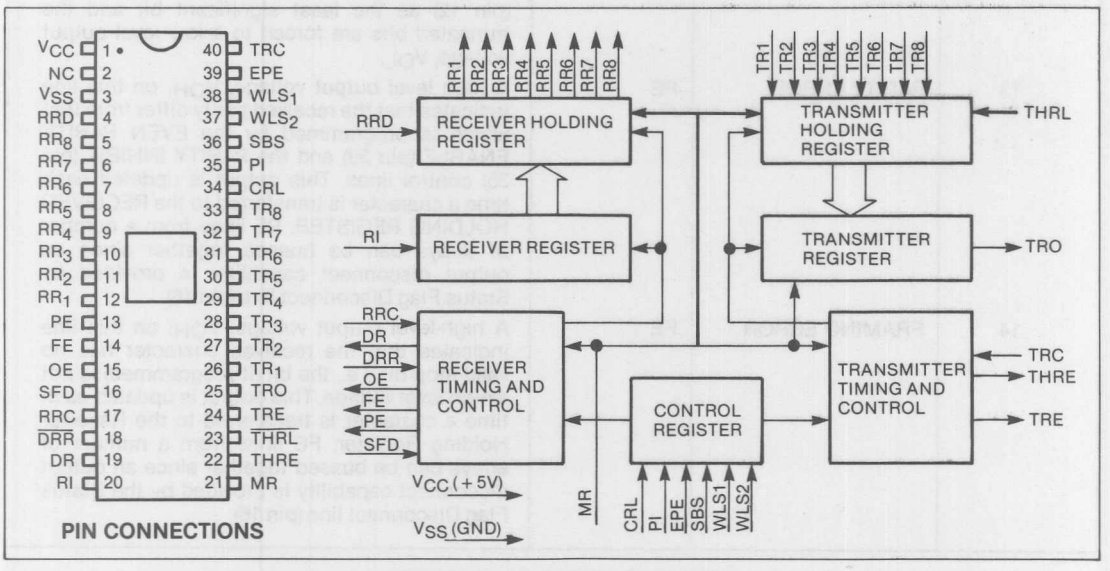
TR1863/TR1865
Universal Asynchronous Receiver/Transmitter (UART)

FEATURES

- SINGLE POWER SUPPLY — +5VDC
- D.C. TO 1 MHZ (64 KB) (STANDARD PART) TR1863/5
- FULL DUPLEX OR HALF DUPLEX OPERATION
- AUTOMATIC INTERNAL SYNCHRONIZATION OF DATA AND CLOCK
- AUTOMATIC START BIT GENERATION
- EXTERNALLY SELECTABLE
  Word Length
  Baud Rate
  Even/Odd Parity (Receiver/Verification — Transmitter/Generation)
  Parity Inhibit
  One, One and One-Half, or Two Stop Bit Generation (1½ at 5 Bit Level)
- AUTOMATIC DATA RECEIVED/TRANSMITTED STATUS GENERATION
  Transmission Complete
  Buffer Register Transfer Complete
  Received Data Available
  Parity Error
  Framing Error
  Overrun Error
- BUFFERED RECEIVER AND TRANSMITTER REGISTERS
- THREE-STATE OUTPUTS
  Receiver Register Outputs
  Status Flags
- TTL COMPATIBLE
- TR1865 HAS PULL-UP RESISTORS ON ALL INPUTS

APPLICATIONS

- PERIPHERALS
- TERMINALS
- MINI COMPUTERS
- FACSIMILE TRANSMISSION
- MODEMS
- CONCENTRATORS
- ASYNCHRONOUS DATA MULTIPLEXERS
- CARD AND TAPE READERS
- PRINTERS
- DATA SETS
- CONTROLLERS
- KEYBOARD ENCODERS
- REMOTE DATA ACQUISITION SYSTEMS
- ASYNCHRONOUS DATA CASSETTES



PIN CONNECTIONS

TR1863/TR1865 BLOCK DIAGRAM

hardwired MOS/LSI device. The UART is used to convert parallel data to a serial data format on the transmit side, and converts a serial data format to parallel data on the receive side.

The serial format in order of transmission and reception is a start bit, followed by five to eight data bits, a parity bit (if selected) and one, one and one-half, or two stop bits.

Three types of error conditions are available on each received character: parity error, framing error (no valid stop bit) and overrun error.

time. The receiver clock is also used to sample in the center of the serial data bits to allow for line distortion.

Both transmitter and receiver are double buffered allowing a one character time maximum between a data read or write. Independent handshake lines for receiver and transmitter are also included. All inputs and outputs are TTL compatible with three-state outputs available on the receiver, and error flags for bussing multiple devices.

PIN DEFINITIONS

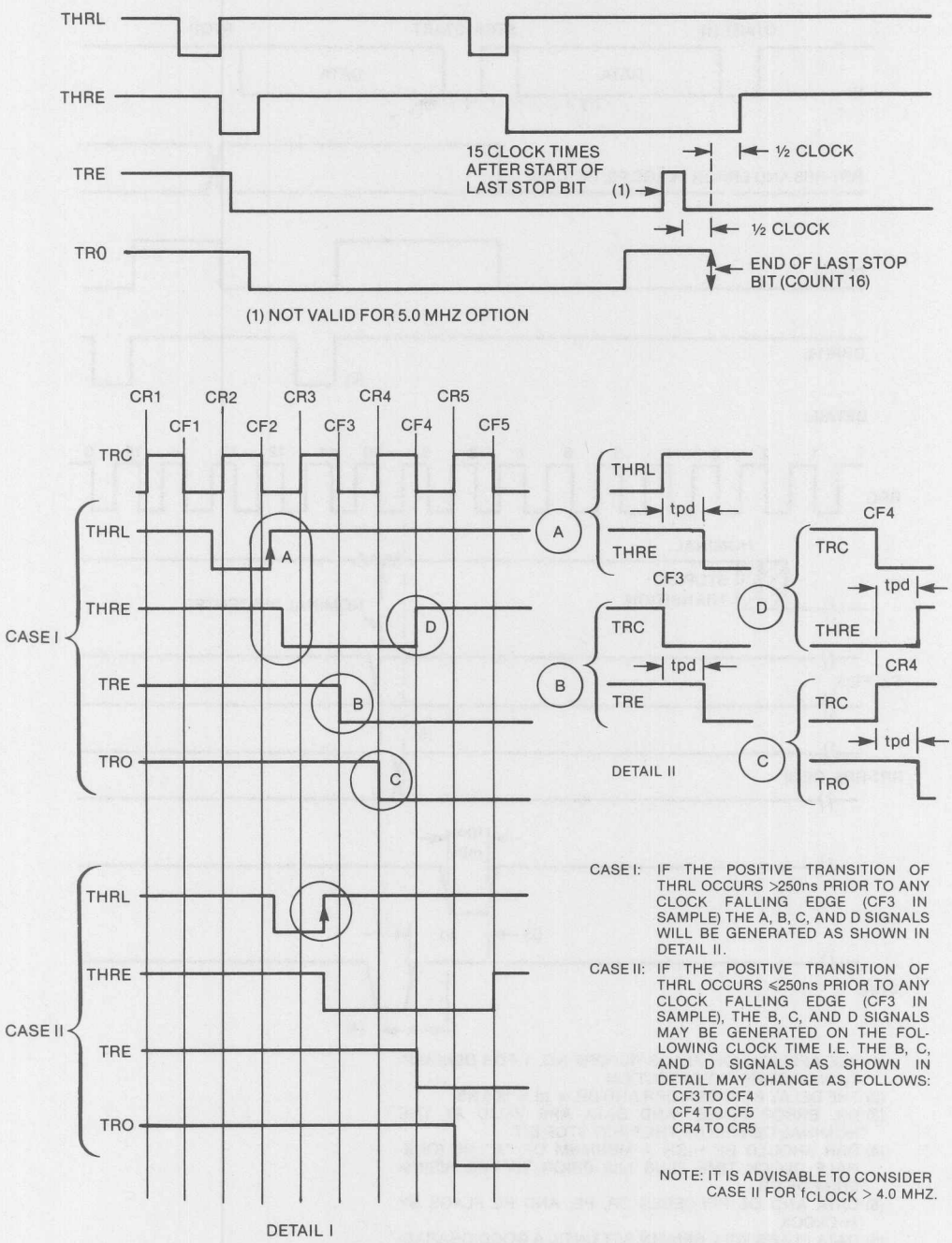
PIN NUMBER	NAME	SYMBOL	FUNCTION
1	POWER SUPPLY	V_{CC}	+5 volts supply
2	NC	NC	No Internal Connection
3	GROUND	V_{SS}	Ground = 0V
4	RECEIVER REGISTER DISCONNECT	RRD	A high level input voltage, V_{IH}, applied to this line disconnects the RECEIVER HOLDING REGISTER outputs from the RR_{1-8} data outputs (pins 5-12).
5-12	RECEIVER HOLDING REGISTER DATA	RR_8-RR_1	The parallel contents of the RECEIVER HOLDING REGISTER appear on these lines if a low-level input voltage, V_{IL}, is applied to RRD. For character formats of fewer than eight bits received characters are right-justified with RR1 (pin 12) as the least significant bit and the truncated bits are forced to a low level output voltage, V_{OL}.
13	PARITY ERROR	PE	A high level output voltage, V_{OH}, on this line indicates that the received parity differ from that which is programmed by the EVEN PARITY ENABLE (pin 39) and the PARITY INHIBIT (pin 35) control lines. This output is updated each time a character is transferred to the RECEIVER HOLDING REGISTER. PE lines from a number of arrays can be bussed together since an output disconnect capability is provided by Status Flag Disconnect line (pin 16).
14	FRAMING ERROR	FE	A high-level output voltage, V_{OH}, on this line indicates that the received character has no valid stop bit, i.e., the bit (if programmed) is not a high level voltage. This output is updated each time a character is transferred to the Receiver Holding Register, FE lines from a number of arrays can be bussed together since an output disconnect capability is provided by the Status Flag Disconnect line (pin 16).

PIN DEFINITIONS

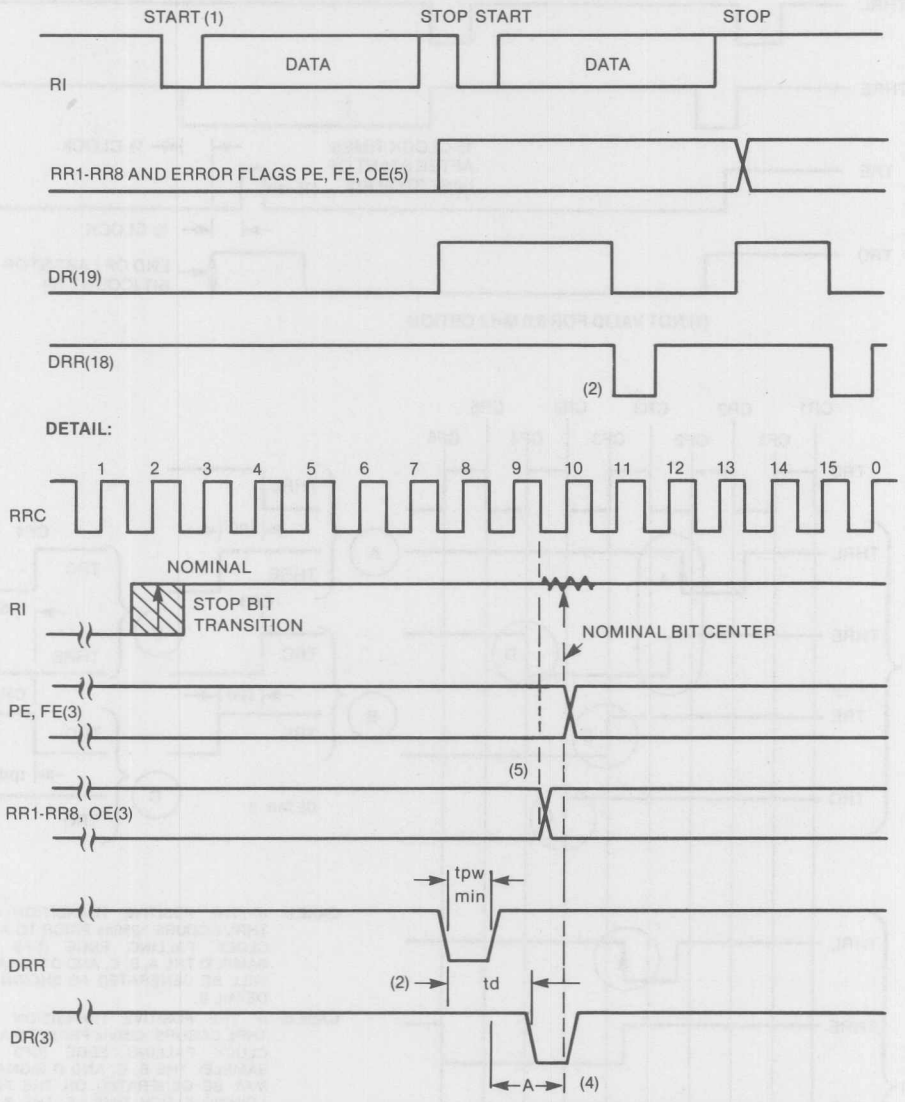
PIN NUMBER	NAME	SYMBOL	FUNCTION
15	OVERRUN ERROR	OE	A high-level output voltage, V_{OH}, on this line indicates that the Data Received Flag (pin 19) was not reset before the next character was transferred to the Receiver Holding Register. OE lines from a number of arrays can be bussed together since an output disconnect capability is provided by the Status Flag Disconnect line (pin 16).
16	STATUS FLAGS DISCONNECT	SFD	A high-level input voltage, V_{IH}, applied to this pin disconnects the PE, FE, OE, DR and THRE allowing them to be buss connected.
17	RECEIVER REGISTER CLOCK	RRC	The receiver clock frequency is sixteen (16) times the desired receiver shift rate.
18	DATA RECEIVED RESET	$\overline{DRR}$	A low-level input voltage, V_{IL}, applied to this line resets the DR line.
19	DATA RECEIVED	DR	A high-level output voltage, V_{OH}, indicates that an entire character has been received and transferred to the RECEIVER HOLDING REGISTER.
20	RECEIVER INPUT	RI	Serial input data. A high-level input voltage, V_{IH}, must be present when data is not being received.
21	MASTER RESET	MR	This line is strobed to a high-level input voltage, V_{IH}, to clear the logic. It resets the TRANSMITTER and RECEIVER HOLDING REGISTERS, the TRANSMITTER REGISTER, FE, OE, PE, DR and sets TRO, THRE, and TRE to a high-level output voltage, V_{OH}.
22	TRANSMITTER HOLDING REGISTER EMPTY	THRE	A high-level output voltage, V_{OH}, on this line indicates the TRANSMITTER HOLDING REGISTER has transferred its contents to the TRANSMITTER REGISTER and may be loaded with a new character.
23	TRANSMITTER HOLDING REGISTER LOAD	$\overline{THRL}$	A low-level input voltage, V_{IL}, applied to this line enters a character into the TRANSMITTER HOLDING REGISTER. A transition from a low-level input voltage, V_{IL}, to a high-level input voltage, V_{IH}, transfers the character into the TRANSMITTER REGISTER if it is not in the process of transmitting a character. If a character is being transmitted, the transfer is delayed until its transmission is completed. Upon completion, the new character is automatically transferred simultaneously with the initiation of the serial transmission of the new character.
24	TRANSMITTER REGISTER EMPTY	TRE	A high-level output voltage, V_{OH}, on this line indicates that the TRANSMITTER REGISTER has completed serial transmission of a full character including STOP bit(s). It remains at this level until the start of transmission of the next character.

PIN DEFINITIONS

PIN NUMBER	NAME	SYMBOL	FUNCTION
25	TRANSMITTER REGISTER OUTPUT	TRO	The contents of the TRANSMITTER REGISTER (START bit, DATA bits, PARITY bit, and STOP bits) are serially shifted out on this line. When no data is being transmitted, this line will remain at a high-level output voltage, V_{OH}. Start of transmission is defined as the transition of the START bit from a high-level output voltage V_{OH}, to a low-level output voltage V_{OL}.
26-33	TRANSMITTER REGISTER DATA INPUTS	TR_1-TR_8	The character to be transmitted is loaded into the TRANSMITTER HOLDING REGISTER on these lines with the THRL Strobe. If a character of less than 8 bits has been selected (by WLS_1 and WLS_2), the character is right justified to the least significant bit, TR_1, and the excess bits are disregarded. A high-level input voltage, V_{IH}, will cause a high-level output voltage, V_{OH}, to be transmitted.
34	CONTROL REGISTER LOAD	CRL	A high-level input voltage, V_{IH}, on this line loads the CONTROL REGISTER with the control bits (WLS_1, WLS_2, EPE, PI, SBS). This line may be strobed or hard wired to a high-level input voltage, V_{IH}.
35	PARITY INHIBIT	PI	A high-level input voltage, V_{IH}, on this line inhibits the parity generation and verification circuits and will clamp the PE output (pin 13) to V_{OL}. If parity is inhibited, the STOP bit(s) will immediately follow the last data bit of transmission.
36	STOP BIT(S) SELECT	SBS	This line selects the number of STOP bits to be transmitted after the parity bit. A high-level input voltage V_{IH}, on this line selects two STOP bits, and a low-level input voltage, V_{IL}, selects a single STOP bit. The TR1863 and TR1865 generate 1½ stop bits when word length is 5 bits and SBS is High V_{IH}.
37-38	WORD LENGTH SELECT	WLS_2-WLS_1	These two lines select the character length (exclusive of parity) as follows: WLS_2 / WLS_1 / Word Length V_{IL} / V_{IL} / 5 bits V_{IL} / V_{IH} / 6 bits V_{IH} / V_{IL} / 7 bits V_{IH} / V_{IH} / 8 bits
39	EVEN PARITY ENABLE	EPE	This line determines whether even or odd PARITY is to be generated by the transmitter and checked by the receiver. A high-level input voltage, V_{IH}, selects even PARITY and a low-level input voltage, V_{IL}, selects odd PARITY.
40	TRANSMITTER REGISTER	TRC	The transmitter clock frequency is sixteen (16) times the desired transmitter shift rate.

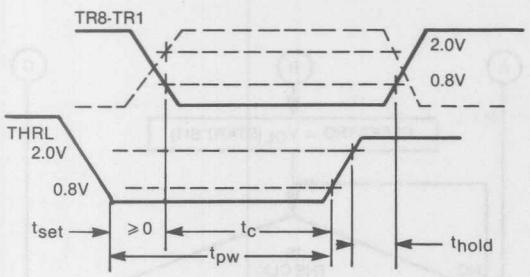


TRANSMITTER TIMING

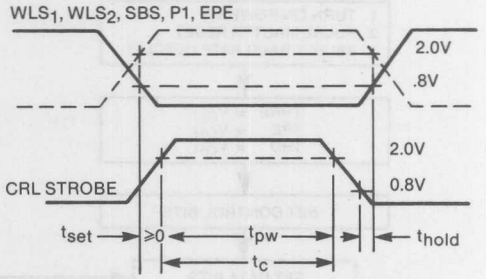


(1) SEE APPLICATION FLAGS REPORT NO. 1 FOR DESCRIPTION OF START BIT DETECTION
(2) THE DELAY BETWEEN DRR AND DR = td = 500 NS
(3) DR. ERROR FLAGS, AND DATA ARE VALID AT THE NOMINAL CENTER OF THE FIRST STOP BIT
(4) DRR SHOULD BE HIGH A MINIMUM OF "A" NS (ONE-HALF CLOCK TIME PLUS tpd) PRIOR TO THE RISING EDGE OF DR
(5) DATA AND OE PRECEDES DR, PE, AND FE FLAGS BY ½ CLOCK
(6) DATA FLAGS WILL REMAIN SET UNTIL A GOOD CHARACTER IS RECEIVED OR MASTER RESET IS APPLIED.

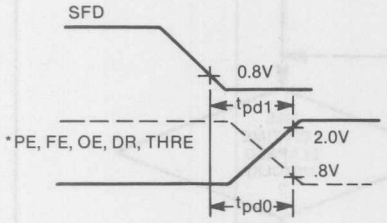
RECEIVER TIMING



DATA INPUT LOAD CYCLE

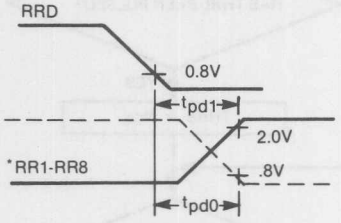


CONTROL REGISTER LOAD CYCLE



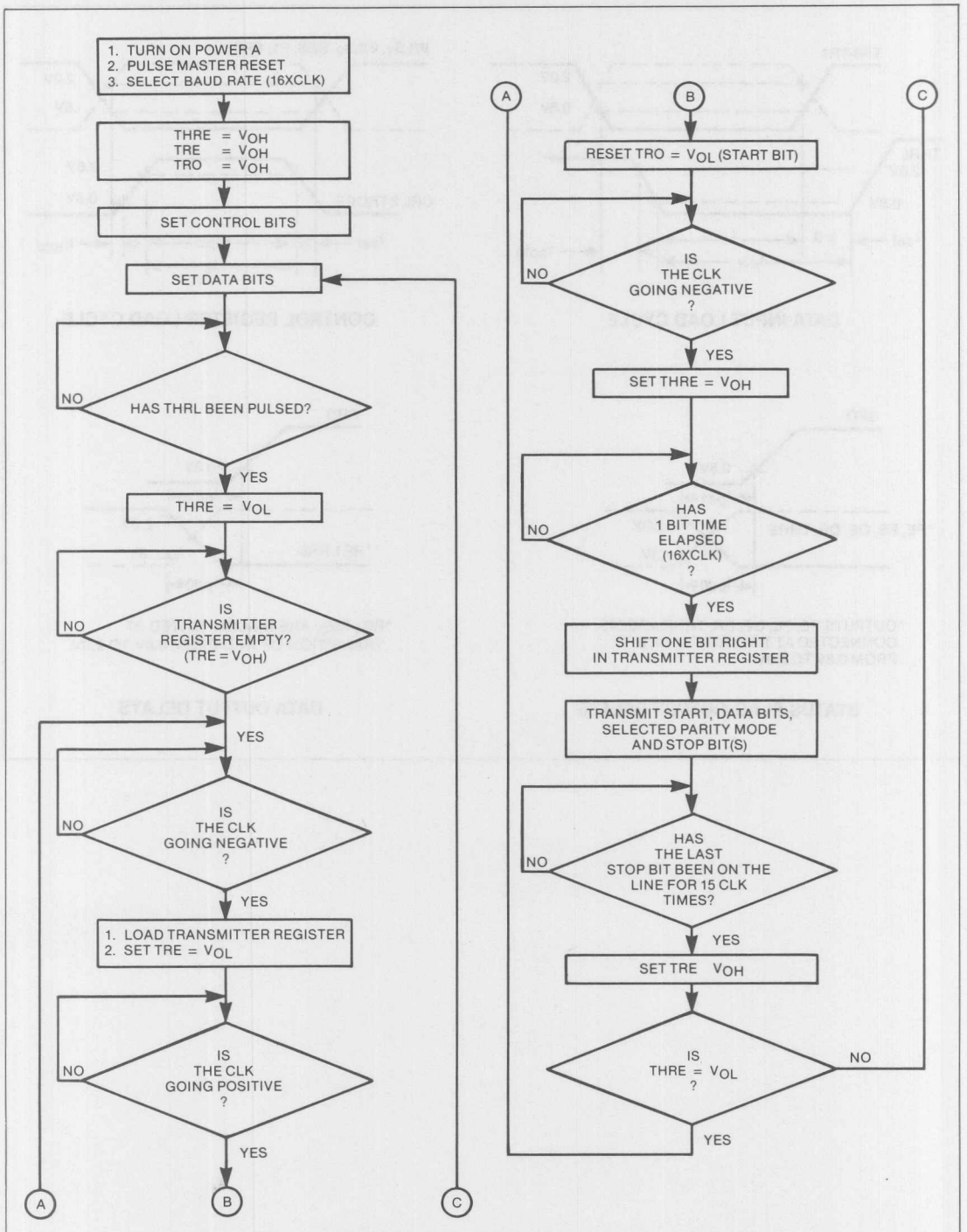
*OUTPUTS PE, FE, OE, DR, THRE ARE DISCONNECTED AT TRANSITION OF SFD FROM 0.8V TO 2.0V.

STATUS FLAG OUTPUT DELAYS

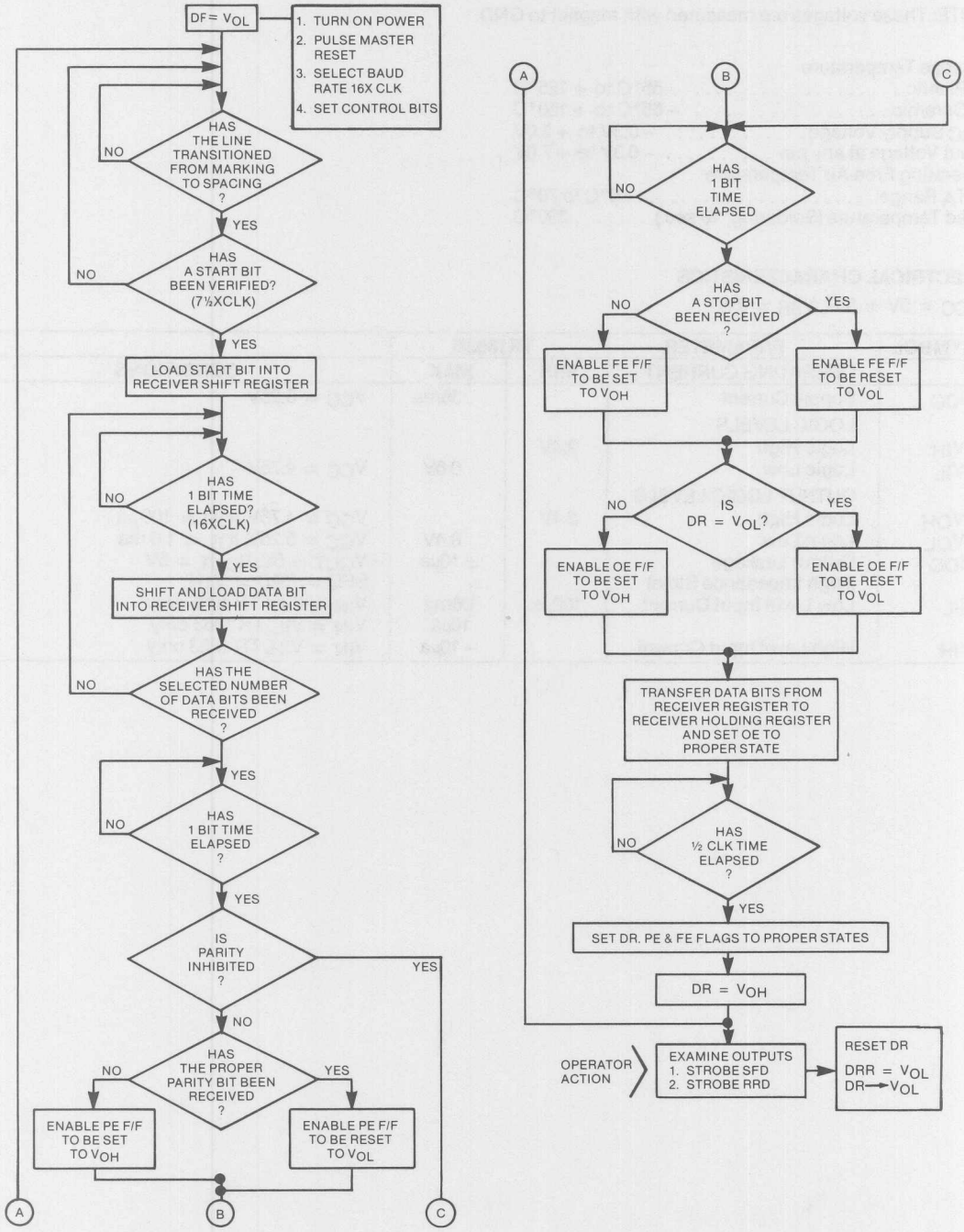


*RR_1-RR_3 ARE DISCONNECTED AT TRANSITION OF RRD FROM 0.8V TO 2.0V.

DATA OUTPUT DELAYS



TRANSMITTER FLOW CHART



RECEIVER FLOW CHART

ABSOLUTE MAXIMUM RATINGS

NOTE: These voltages are measured with respect to GND

Storage Temperature
- Plastic . . . . . −55°C to +125°C
- Ceramic . . . . . −65°C to +150°C

V_{CC} Supply Voltage . . . . . −0.3V to +7.0V
Input Voltage at any pin . . . . . −0.3V to +7.0V
Operating Free-Air Temperature
- T_A Range . . . . . 0°C to 70°C

Lead Temperature (Soldering, 10 sec.) . . . . . 300°C

ELECTRICAL CHARACTERISTICS

(V_{CC} = 5V ± 5%, V_{SS} = 0V)

SYMBOL	PARAMETER	TR1863/5		
	OPERATING CURRENT	MIN	MAX	CONDITIONS
I_{CC}	Supply Current		35ma	V_{CC} = 5.25V
	LOGIC LEVELS			
V_{IH}	Logic High	2.4V		
V_{IL}	Logic Low		0.6V	V_{CC} = 4.75V
	OUTPUT LOGIC LEVELS			
V_{OH}	Logic High	2.4V		V_{CC} = 4.75V, I_{OH} = 100 μa
V_{OL}	Logic Low		0.4V	V_{CC} = 5.25V, I_{OL} = 1.6 ma
I_{OC}	Output Leakage (High Impedance State)		± 10μa	V_{OUT} = 0V, V_{OUT} = 5V SFD = RRD = V_1H
I_{IL}	Low Level Input Current	100μa	1.6ma	V_{IN} = 0.4V TR 1865 only
			10μa	V_{IN} = V_{IL}, TR 1863 only
I_{IH}	High Level Input Current		− 10μa	V_{IN} = V_{IH}, TR 1863 only

SWITCHING CHARACTERISTICS
(See "Switching Waveforms")

SYMBOL	PARAMETER	MIN	MAX	CONDITIONS
f_{clock}	Clock Frequency			V_{CC} = 4.75V
	TR1863-00	DC	1.0 MHz	
	TR1863-02	DC	2.5 MHz	
	TR1863-04	DC	3.5 MHz	
	TR1865-00	DC	1.0 MHz	with internal pull-ups on all inputs
	TR1865-02	DC	2.5 MHz	with internal pull-ups on all inputs
	TR1865-04	DC	3.5 MHz	with internal pull-ups on all inputs
t_{pw}	Pulse Widths			
	CRL	200 ns		
	THRL	200 ns		
	DRR	200 ns		
	MR	500 ns		
t_c	Coincidence Time	200 ns		
t_{hold}	Hold Time	20 ns		
t_{set}	Set Time	0		
	OUTPUT PROPAGATION DELAYS			
t_{pd0}	To Low State		250 ns	
t_{pd1}	To High State		250 ns	C_L = 20 pf, plus one TTL load
	CAPACITANCE			
c_{in}	Inputs		20 pf	f = 1 MHz, V_{IN} = 5V
c_o	Outputs		20 pf	f = 1 MHz, V_{IN} = 5V

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TR1602/TR1863/TR1865 MOS/LSI Application Notes
Asynchronous Receiver/Transmitter

INTRODUCTION

The transfer of digital data over relatively long distances is generally accomplished by sending the data in serial form thru a single communications channel using one of two general transmission techniques; asynchronous or synchronous. Synchronous data transmission requires that a clock signal be transmitted with the data in order to mark the location of the data bits for receiver. A specified clock transition (either rising or falling) marks the start of each data bit interval as shown in Figure 1. In addition, special synchronization data patterns are added to the start of the transmission in order for the receiver to locate the first bit of the message. With synchronous transmission, each data bit must follow contiguously after the sync word, since one data bit is assumed for every clock period or a fixed multiple of clock periods.

With asynchronous transmission, a clock signal is not transmitted with the data and the characters need not be contiguous. In order for the receiver to properly recover the message, the bits are grouped into data characters (generally from 5 to 8 bits in length) and synchronizing start and stop elements are added to each character as shown in Figure 2.

The start element is a single logic zero (space) data bit that is added to the front of each character. The stop element is a logic one (mark) that is added to the end of each character. The logic one (mark) level is maintained until the next data character is ready to be transmitted. (Asynchronous transmission is often referred to as start-stop transmission for obvious reasons). Although there is no upper limit to the length of the stop element, there is a lower limit that depends on the system characteristics. Typical lower limits are 1.0, 1.42 or 2.0 data bit intervals, although

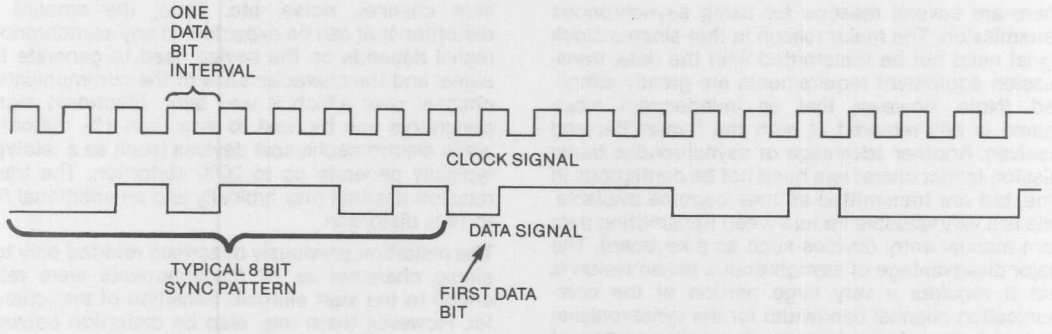


Figure 1. SYNCHRONOUS DATA

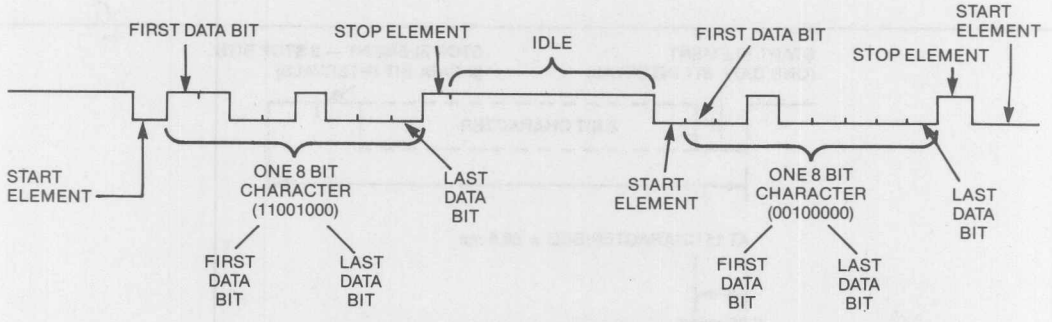


Figure 2. ASYNCHRONOUS DATA

most modern systems use 1.0 or 2.0. The negative going transition of the start element defines the location of the data bits in one character. A clock source at the receiver is reset by this transition and is used to locate the center of each data bit.

The rate at which asynchronous data is transmitted is usually measured in baud, where a baud is defined to be the reciprocal of the shortest signal element (usually one data bit interval). It is interesting to note that the variable stop bits is what makes the baud rate differ from the bit rate. For synchronous transmission, each data element is equal to the clock period therefore the baud rate equals the bit rate. The same is true for asynchronous transmission if the stop element is always one bit in duration (this is referred to as isochronous transmission). However, when the stop code is longer than one bit, as shown in Figure 3, the baud rate differs from the bit rate.

Each character in Figure 3 is 11 data bit intervals in length, and if 15 characters are transmitted per second, then the shortest signal element (one data bit interval) is 66.6 ms/11 = 6.06 ms; giving a rate of 1/6.06 ms = 165 baud. However, since only 10 bits of information (8 data bits, one start bit and 1 stop bit) are transmitted every 66.6 msec, the bit rate is 150 bit/sec. (Even though the stop element lasts for two data intervals, it still is only one bit of information.)

There are several reasons for using asynchronous transmission. The major reason is that since a clock signal need not be transmitted with the data, transmission equipment requirements are greatly simplified. (Note, however, that an independent clock source is still required at both the transmitter and receiver). Another advantage of asynchronous transmission is that characters need not be contiguous in time, but are transmitted as they become available. This is a very valuable feature when transmitting data from manual entry devices such as a keyboard. The major disadvantage of asynchronous transmission is that it requires a very large portion of the communication channel bandwidth for the synchronizing start and stop elements (a much smaller portion of the bandwidth is required for the sync words used in synchronous transmission).

Asynchronous transmission over a simple twisted wire pair can be accomplished at moderately high baud rates (10K baud or higher depending on the length of the wire, type of line drivers, etc.) while it is generally limited to approximately 2K baud over the telephone network. Other types of asynchronous transmission can be as high as 300K baud. When operating over the telephone network, a modem is required to convert the data pulses to tones that can be transmitted through the network.

One of the major limiting factors in the speed of asynchronous transmission is the distortion of the signal elements. Distortion is defined as the time displacement between the actual signal level transmission and the nominal transition ($\Delta\dagger$), divided by the nominal data bit interval (See Figure 4).

The nominal data bit interval is equal to the reciprocal of the nominal transmission baud rate and all data transitions should ideally occur at an integer number of intervals from the negative transition of the start bit. Actual data transitions may not occur at these nominal points in time as shown in the lower waveform of Figure 4. The distortion of any bit transition is equal to $\Delta\dagger$ x NOMINAL BAUD RATE.

This distortion is generally caused by frequency jitter and frequency offset in the clock source, used to generate the actual waveform as well as transmission channel, noise, etc. Thus, the amount of distortion that can be expected on any asynchronous signal depends on the device used to generate the signal and the characteristics of the communication channel over which it was sent. Electronic signal generators can be held to less than 1% distortion while electromechanical devices (such as a teletype) typically generate up to 20% distortion. The transmission channel may typically add an additional 5% to 15% distortion.

The distortion previously described referred only to a single character as all measurements were referenced to the start element transition of that character. However, there may also be distortion between characters when operating at the maximum possible baud rate (i.e., stop elements are of minimum length).

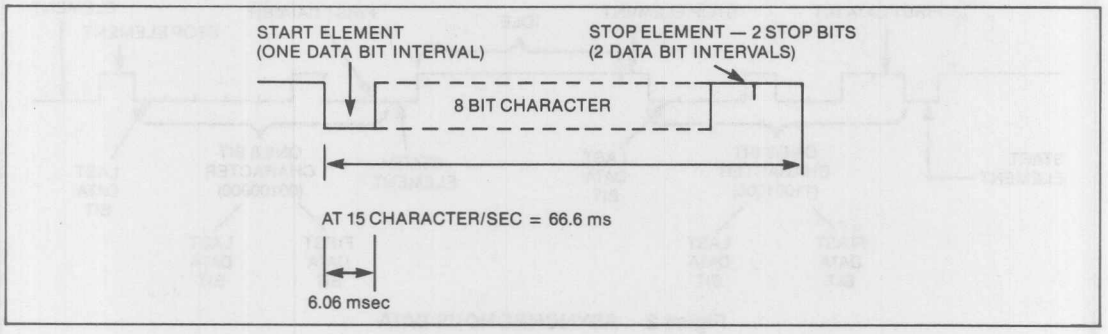


Figure 3.

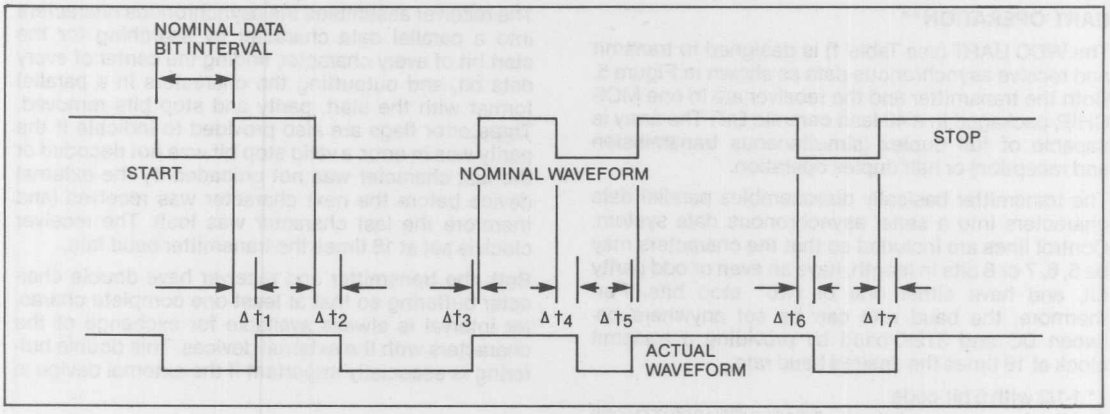


Figure 4A.

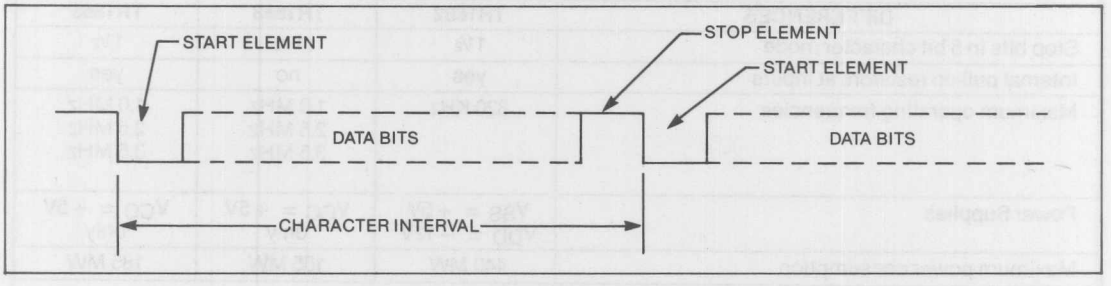


Figure 4B.

This type of distortion is usually measured by the minimum character interval as shown in Figure 4B.

The minimum character interval distortion is generally specified as the percentage of a nominal data bit interval that any character interval may be shortened from its nominal length. Since many of the same parameters that cause distortion of the data bits are also responsible for the character length distortion, the two distortions are often equal. However, some systems may exhibit character interval distortions of up to 50% of a data bit interval. This parameter is important when operating at the maximum baud rate since the receiver must be prepared to detect the next start bit transition after the minimum character interval.

Asynchronous receivers operate by locating the nominal center of the data bits as measured from the start bit negative going transition. However, due to receiver inaccuracies, the exact center may not be properly located. In electromechanical devices such as teletypes, the inaccuracy may be due to mechanical tolerances or variations in the power line frequency. With electronic receivers, the inaccuracies are due to frequency offset, jitter and resolution of the clock source used to find the bit centers. (The bit centers are located by counting clock pulses). For example, even if the receiver clock had no jitter or offset, and it was 16 times the baud rate, then the center of the bit could only be located within 1/16 of a bit interval (or 6.25%) due to clock resolution. However, by properly phasing the clock, this tolerance can be adjusted so that the sampling will always be within ±3.125% of the bit center. Thus, signals with up to 46.875% distortion could be received. This number (the allowable receiver input distortion) is often referred to as the receiver distortion margin. Electromechanical receivers have distortion margins of 25 to 30%. The receiver must also be prepared to accept a new character after the minimum character interval. Most receivers are specified to operate with a minimum character interval distortion of 50%.

Both the transmitter and the receiver are in one MOS CHIP, packaged in a 40 lead ceramic DIP. The array is capable of full duplex (simultaneous transmission and reception) or half duplex operation.

The transmitter basically disassembles parallel data characters into a serial asynchronous data system. Control lines are included so that the characters may be 5, 6, 7 or 8 bits in length, have an even or odd parity bit, and have either one or two* stop bits. Furthermore, the baud rate can be set anywhere between DC and 312K baud by providing a transmit clock at 16 times the desired baud rate.

* 1-1/2 with 5 bit code

** All references apply to the TR1602/TR1863/TR1865 operation.

format with the start, parity and stop bits removed. Three error flags are also provided to indicate if the parity was in error, a valid stop bit was not decoded or the last character was not unloaded by the external device before the next character was received (and therefore the last character was lost). The receiver clock is set at 16 times the transmitter baud rate.

Both the transmitter and receiver have double character buffering so that at least one complete character interval is always available for exchange of the characters with the external devices. This double buffering is especially important if the external device is

Table 1.

DIFFERENCES	TR1602	TR1863	TR1865
Stop bits in 5 bit character mode	1½	1½	1½
Internal pull-up resistors at inputs	yes	no	yes
Maximum operating frequencies	320 KHz	1.0 MHz 2.5 MHz 3.5 MHz	1.0 MHz 2.5 MHz 3.5 MHz
Power Supplies	V_{SS} = +5V V_{DD} = −12V	V_{CC} = +5V only	V_{CC} = +5V only
Maximum power consumption	440 MW	185 MW	185 MW

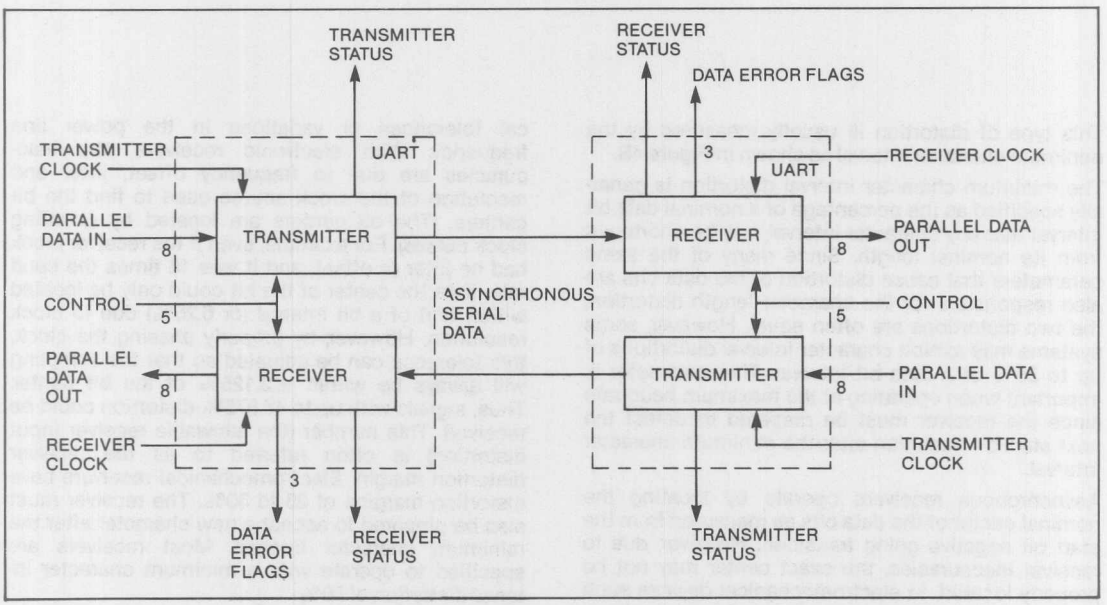


Figure 5.

a computer, since this provides a much longer permissible interrupt latency time (the time required for the computer to respond to the interrupt).

The status of the transmitter buffer and the receiver buffer (empty or full) is also provided as an output.

Another feature of the UART is that the control information can be strobed into the transmitter and receiver and stored internally. This allows a common bus from a computer to easily maintain the controls for a large number of transmitter/receivers.

The UART data and error flag outputs are designed for direct compatibility with bus organized systems. This feature is achieved by providing completely TTL compatible Three-state outputs (no external components are required). Three-state outputs may be set to a logic one or logic zero when enabled, or set to an open circuit (very high impedance) when disabled. A separate control line is provided to enable the data outputs and another one to enable the error flags so that the data outputs can be tied to a separate bus from the flag outputs.

The TR1602/1865 inputs are also directly compatible with TTL logic elements without any external components. TR1863 require pullups on inputs.

UART DESCRIPTION

Figure 6 is a block diagram of the transmitter portion of the UART. Data can be loaded into the Transmitter Holding Register whenever the Transmitter Holding Register Empty (THRE) line is at a logic one, indicating that the Transmitter Holding Register is empty. The data is loaded in by strobing the Transmitter Holding Register Load (THRL) line to a logic zero. The data is automatically transferred to the Transmitter Register as soon as the Transmitter Register becomes empty. The desired start, stop and parity bits are then added to the data and serial transmission is started. The number of stop bits and the type of parity bit is under control of the Control Register. The state of the control lines is loaded into the Control Register when the Control Register Load (CRL) line is strobed to a logic one. The 5 control lines allow 24 different character formats as shown in Table 2. These 24 formats cover almost all of the transmission schemes presently in use.

A Master Reset (MR) input is provided which sets the transmitter to the idle state whenever this line is strobed to a logic one. In addition, a Status Flag Disconnect (SFD) line is provided. When this signal is at a logic one, the THRE output is disabled and goes to a high impedance. This allows the THRE outputs of a number of arrays to be tied to the same data bus.

Figure 7 illustrates the relative timing of the transmitter signals. After power turn-on, the master reset should be strobed to set the circuits to the idle state. The external device can then set the transmitter register data inputs to the desired value and after the data inputs are stable, the load pulse is applied. The data is then automatically transferred to the Transmitter Register where the start, stop and parity (if required) bits are added and transmission is started. This process is then repeated for each subsequent character as they become available. The only timing requirement for the external device is that the data inputs be stable during the load pulse (and 20 nsec after).

Table 2.
CONTROL DEFINITION

CONTROL WORD					CHARACTER FORMAT			
WLS2	WLS1	PI	EPE	SBS	START BIT	DATA BITS	PARITY BIT	STOP BITS
0	0	0	0	0	1	5	ODD	1
0	0	0	0	1	1	5	ODD	1.5
0	0	0	1	0	1	5	EVEN	1
0	0	0	1	1	1	5	EVEN	1.5
0	0	1	x	0	1	5	NONE	1
0	0	1	x	1	1	5	NONE	1.5
0	1	0	0	0	1	6	ODD	1
0	1	0	0	1	1	6	ODD	2
0	1	0	1	0	1	6	EVEN	1
0	1	0	1	1	1	6	EVEN	2
0	1	1	x	0	1	6	NONE	1
0	1	1	x	1	1	6	NONE	2
1	0	0	0	0	1	7	ODD	1
1	0	0	0	1	1	7	ODD	2
1	0	0	1	0	1	7	EVEN	1
1	0	0	1	1	1	7	EVEN	2
1	0	1	x	0	1	7	NONE	1
1	0	1	x	1	1	7	NONE	2
1	1	0	0	0	1	8	ODD	1
1	1	0	0	1	1	8	ODD	2
1	1	0	1	0	1	8	EVEN	1
1	1	0	1	1	1	8	EVEN	2
1	1	1	x	0	1	8	NONE	1
1	1	1	x	1	1	8	NONE	2

The UART Transmitter output will have less than 1% Distortion at baud rates of up to 312K baud (assuming the Transmitter Register Clock is perfect) and is, therefore, compatible with virtually all other asynchronous receivers.

Figure 8 is a block diagram of the Receiver portion of the UART. Serial asynchronous data is provided to the Receiver Input (RI). A start bit detect circuit continually searches for a logic one to logic zero transition while in the idle (logic one) state. When this transition is located, a counter is reset and allowed to count until the center of the start bit is located. If the input is still a logic zero at the center, the signal is assumed to be a valid start bit and the counter continues to count to find the center of all subsequent data and stop bits. (Verification of the start bit prevents the receiver from assembling an erroneous data character when a logic zero noise

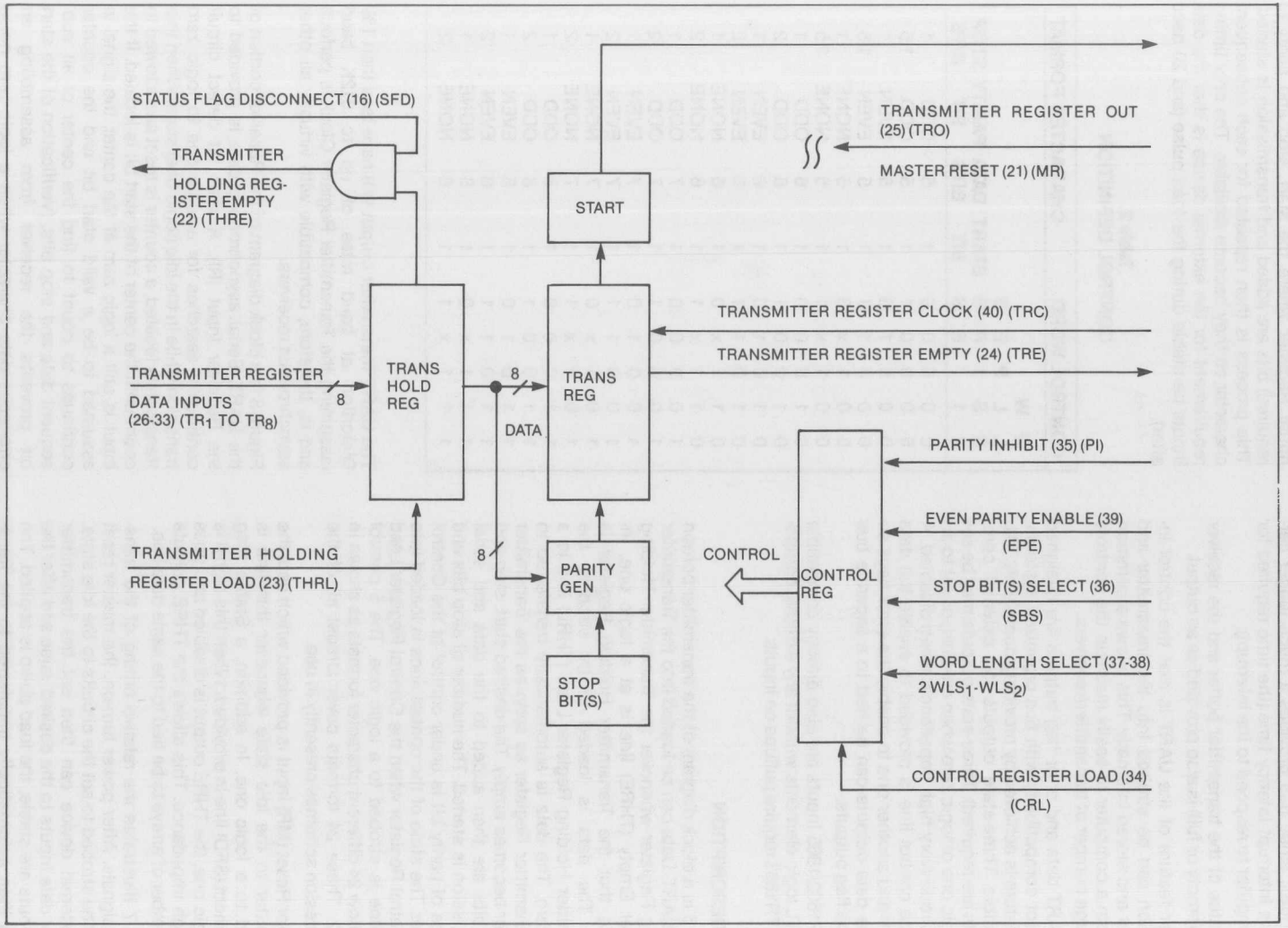


Figure 6. TRANSMITTER BLOCK DIAGRAM

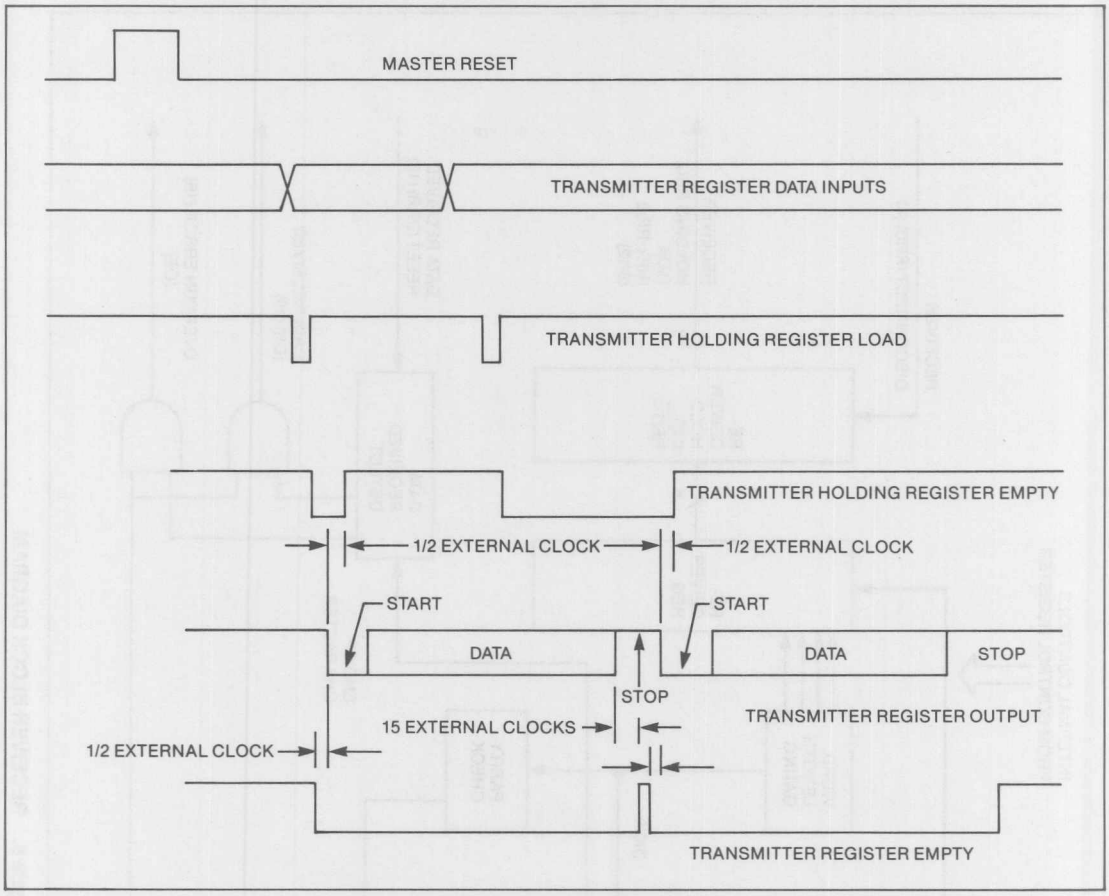


Figure 7. TRANSMITTER TIMING DIAGRAM

spike is presented to the Receiver Input). The Receiver is under control of the Control Register described in the previous paragraph. This register controls the number of data bits, number of stop bits, and the type of parity as described in Table 2. The word length gating circuit adjusts the length of the Receiver Register to match the length of the data characters. A parity check circuit checks for even or odd parity if parity was programmed. If parity does not check a Parity Error signal will be set to a logic one and this signal will be held until the next character is transferred to the Holding Register. A circuit is also provided that checks the first stop bit of each character. If the stop bit is not a logic one, the Framing Error line will be set to a logic one and held until the next character is transferred to the Holding Register. This feature permits easy detection of a break character (null character with no stop element). As each received character is transferred to the Holding Register, the Data Received (DR) line is set to a logic one indicating that the external device may sample the data output. When the external device samples the output, it should strobe the Data Received Reset (DRR) line to a logic zero to reset the DR line. If the DR line is not reset before a new character is transferred to the Holding Register (i.e., a character is lost) the Overrun Error line will be set to a logic one and held until the next character is loaded into the Holding Register. The timing for all of the Receiver functions is obtained from the external Receiver Register Clock which should be set at 16 times the baud rate of the transmitter.

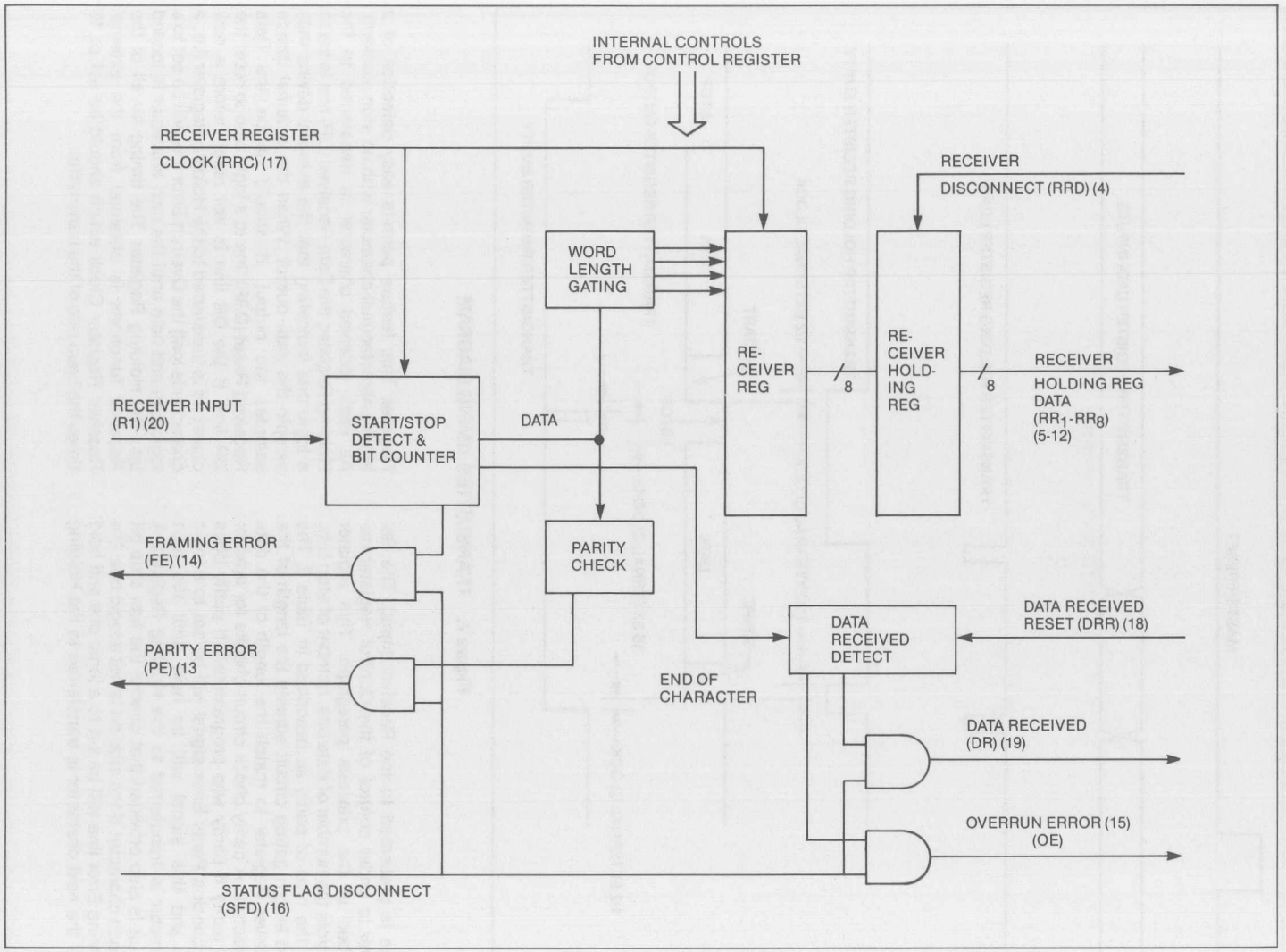


Figure 8. RECEIVER BLOCK DIAGRAM

Figure 9 illustrates the relative timing of the Receiver signals. A Master Reset strobe places the unit in the idle mode and the Receiver then begins searching for the first start bit. After a complete character has been decoded, the data output and error flags are set to the proper level and the Data Received (DR) line is set to a logic one. Although it is not apparent in Figure 9, the data outputs are set to the proper level one half clock period before the DR and error flags, which are set in the center of the first stop bit. The Data Received Reset pulse resets the DR line to a logic zero. Data can be strobed out at any time before the next character has been disassembled.

The UART Receiver uses a 16X clock for timing purposes. Furthermore, the center of the start bit is defined as clock count 7-1/2. Therefore, if the receiver clock is a symmetrical square wave as shown in Figure 10, the center of the bits will always be located within ±3.125% (assuming a perfect input clock) thus giving a receiver margin of 46.875%.

In Figure 10, the start bit could have started as much as one complete clock period before it was detected, as indicated by the shaded area of the negative going transition. Therefore, the exact center is also unknown by the shaded area around the sample point. This turns out to be ± 1/32 = ±3.125%.

If the receiver clock is not perfect, then the receiver distortion margin must be further reduced. For example, if the clock had 1.0% jitter, 0.1% offset and the positive clock pulse was only 40% of the clock cycle; then, for a 10 element character, the clock would add:

1.0% (Jitter)	+ (0.1% x 10) (Offset)	+ 0.1 (1/16) (Non-symmetrical Clock)	=	2.3% Distortion

(The frequency offset was multiplied by the number of elements per character since the offset is cumulative on each element.

Since a clock with these characteristics is very easy to obtain, it is apparent that a receiver operating margin of slightly over 45% is very easy to achieve when using the UART. Furthermore, this margin is sufficient for virtually all existing transmitters and modems presently in use.

The UART also begins searching for the next start bit exactly in the center of the first stop bit so that minimum character distortions of up to 50% can be accepted.

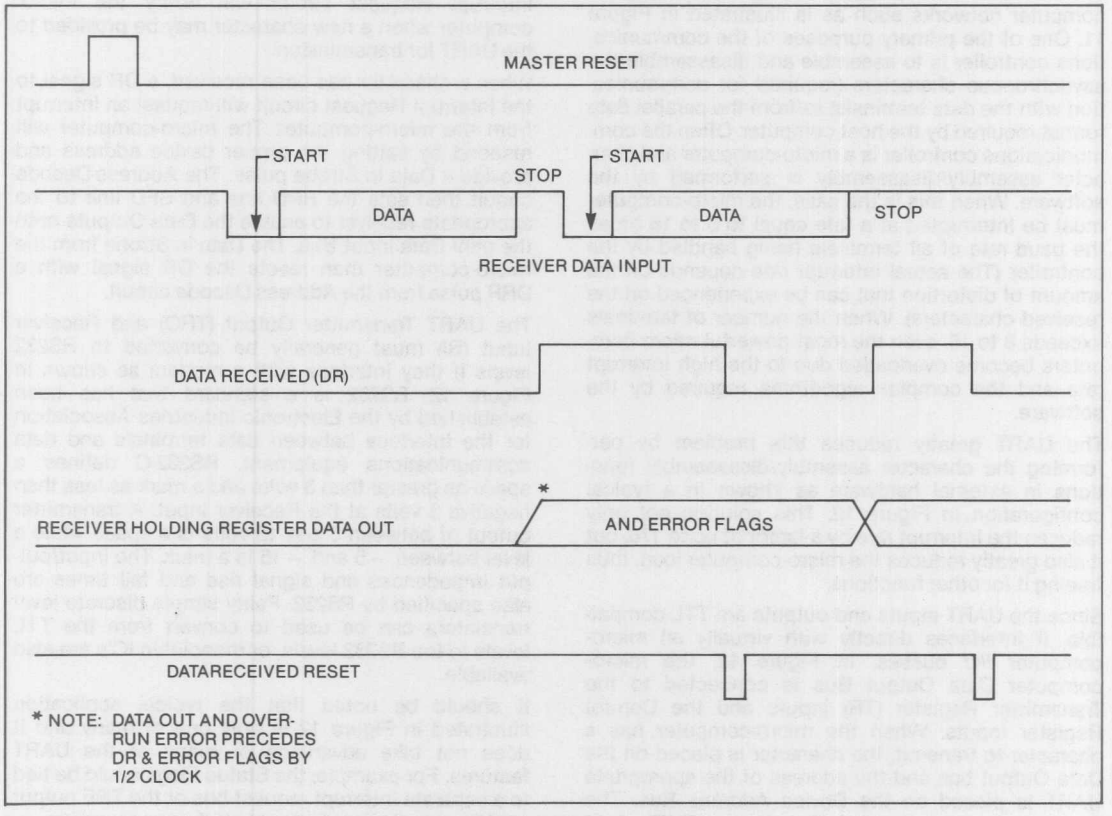


Figure 9. RECEIVER TIMING DIAGRAM

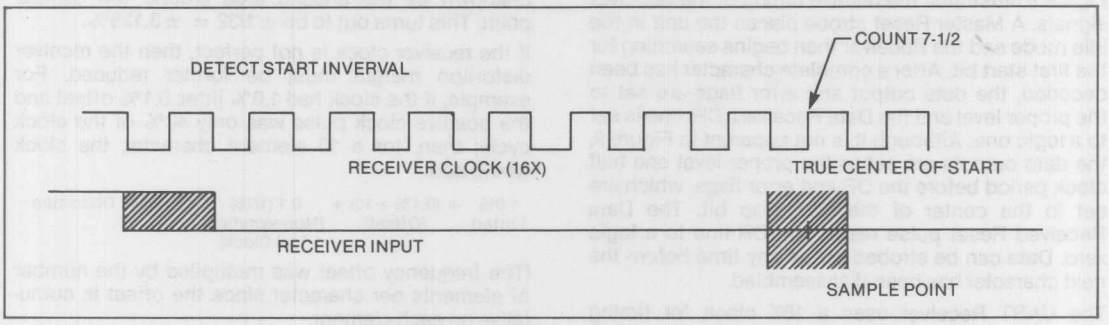


Figure 10.

A break character (null character without a stop bit) will lock the receiver up since it will not begin looking for the next start bit until a stop bit has been received.

TYPICAL UART APPLICATION

The UART is ideally suited for use in distributed computer networks such as is illustrated in Figure 11. One of the primary purposes of the communications controller is to assemble and disassemble the asynchronous characters (required for communication with the data terminals) to/from the parallel data format required by the host computer. Often the communications controller is a micro-computer and character assembly/disassembly is performed by the software. When this is the case, the micro-computer must be interrupted at a rate equal to 8 to 16 times the baud rate of all terminals being handled by the controller. (The actual interrupt rate depends on the amount of distortion that can be experienced on the received characters). When the number of terminals exceeds 8 to 16, even the most powerful micro-computers become overloaded due to the high interrupt rate and the complex algorithms required by the software.

The UART greatly reduces this problem by performing the character assembly/disassembly functions in external hardware as shown in a typical configuration in Figure 12. This solution not only reduces the interrupt rate by a factor of up to 176, but it also greatly reduces the micro-computer load, thus freeing it for other functions.

Since the UART inputs and outputs are TTL compatible, it interfaces directly with virtually all micro-computer I/O busses. In Figure 12, the micro-computer Data Output Bus is connected to the Transmitter Register (TR) inputs and the Control Register inputs. When the micro-computer has a character to transmit, the character is placed on the Data Output bus and the address of the appropriate UART is placed on the Device Address Bus. The Address Decode circuit will output a THRL load pulse under control of the Data Out Strobe from the micro-computer. When the control register should be changed, a new 5 bit control word is placed on the Data Output Bus and along with an appropriate device address which is converted to a CRL load pulse in the Address Decode circuits, again under control of the Data Out Strobe. A THRE Pulse to the Interrupt Request circuit will notify the micro-computer when a new character may be provided to the UART for transmission.

When a character has been received, a DR signal to the Interrupt Request circuit will request an interrupt from the micro-computer. The micro-computer will respond by setting the proper device address and provide a Data in Strobe pulse. The Address-Decode circuit then sets the RRD line and SFD line to the appropriate receiver to enable the Data Outputs onto the mini Data Input Bus. The Data in Strobe from the micro-computer then resets the DR signal with a DRR pulse from the Address Decode circuit.

The UART Transmitter Output (TRO) and Receiver Input (RI) must generally be converted to RS232 levels if they interface with a modem as shown in Figure 12. RS232 is a standard that has been established by the Electronic Industries Association for the interface between data terminals and data communications equipment. RS232-C defines a space as greater than 3 volts and a mark as less than negative 3 volts at the Receiver input. A transmitter output of between 5 and 15 volts is a space while a level between -5 and -15 is a mark. The input/output impedances and signal rise and fall times are also specified by RS232. Fairly simple discrete level translators can be used to convert from the TTL levels to the RS232 levels, or monolithic IC's are also available.

It should be noted that the typical application illustrated in Figure 12 is only one of many and it does not take advantage of many of the UART features. For example, the Status Flags could be tied to a separate interrupt request bus or the TRE output could be used to implement half-duplex operation.

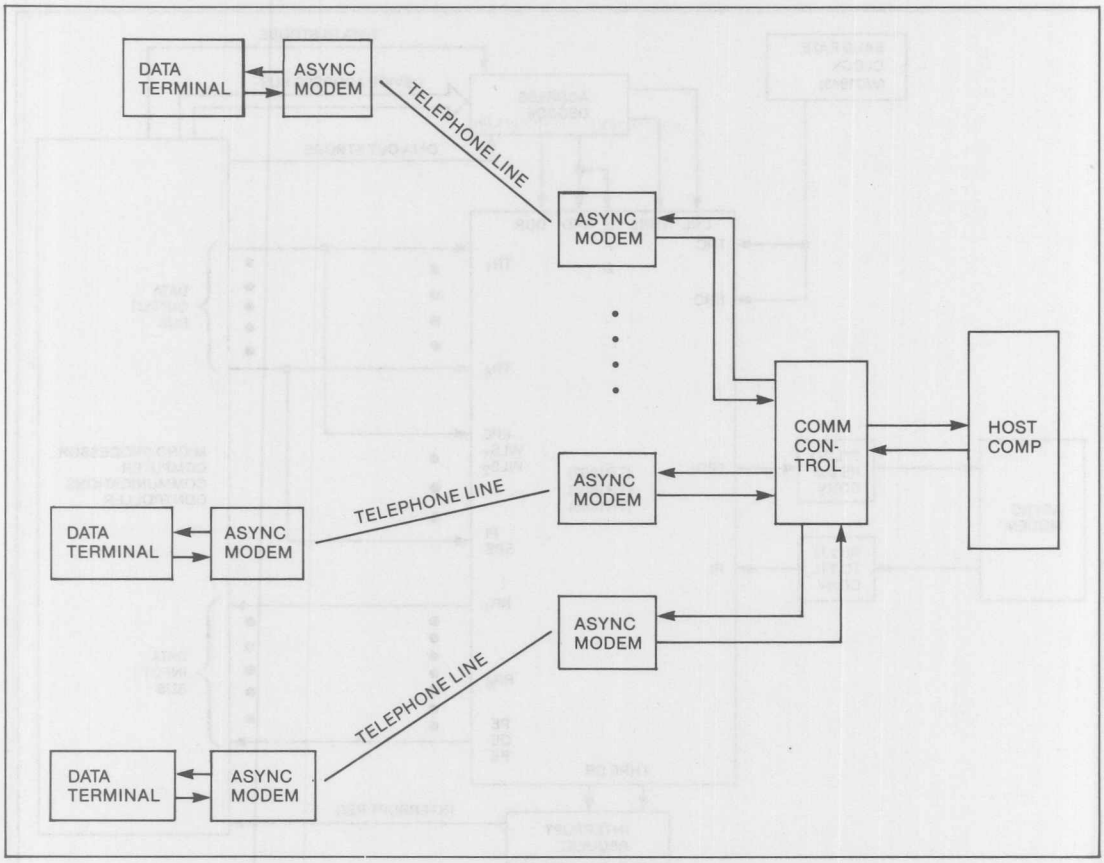

DATA TERMINAL
ASYNC MODEM
TELEPHONE LINE
ASYNC MODEM
COMM CON-TROL
HOST COMP
ASYNC MODEM
DATA TERMINAL
ASYNC MODEM
TELEPHONE LINE
ASYNC MODEM
TELEPHONE LINE
DATA TERMINAL
ASYNC MODEM

Figure 11.

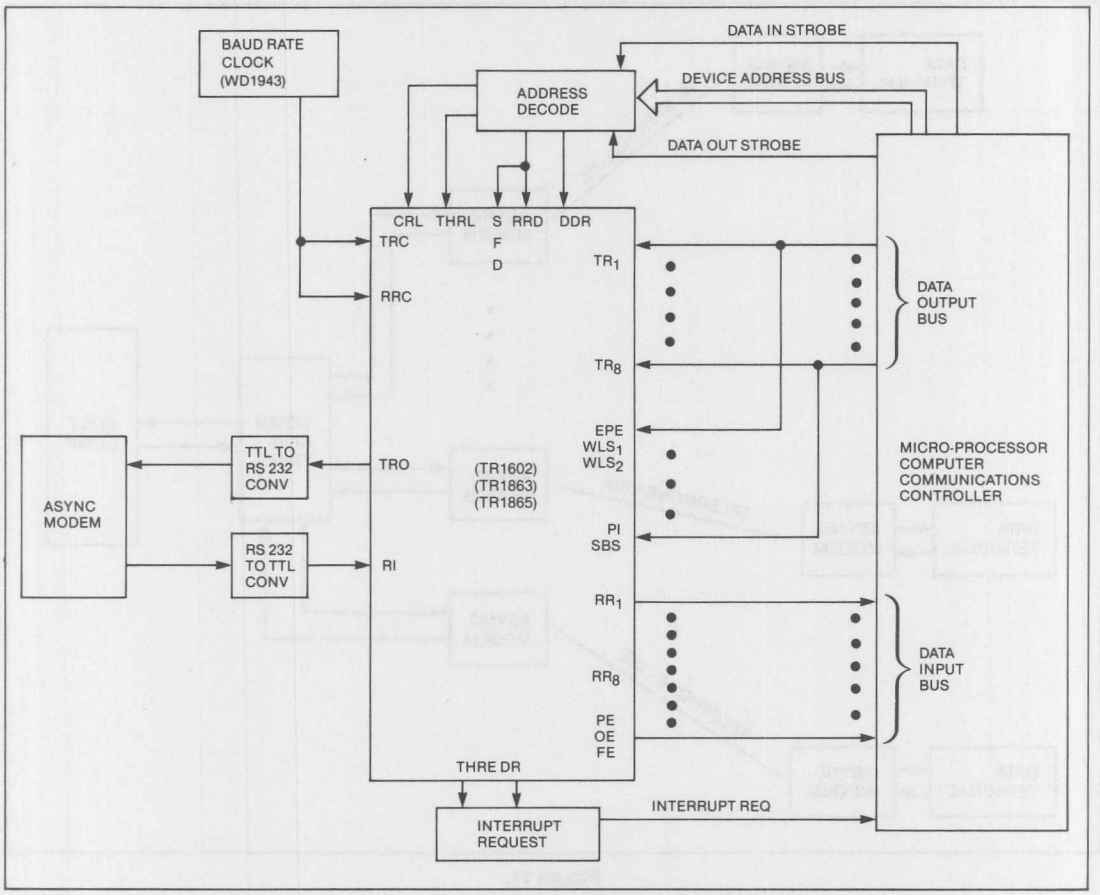


Figure 12. TYPICAL MICROCOMPUTER INTERFACE

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WESTERN DIGITAL
CORPORATION

WD1983 (BOART)
Bus Oriented Asynchronous Receiver/Transmitter

FEATURES

ASYNCHRONOUS MODE

- FULL DUPLEX OPERATION
- SELECTABLE 5,6,7, & 8 BIT CHARACTERS
- LINE BREAK DETECTION AND GENERATION
- 1, 1½, or 2 STOP BIT SELECTION
- FALSE START BIT DETECTION
- OVERRUN AND FRAMING ERROR DETECTION
- DC TO 36K BITS/SEC (16X)
- DC TO 600K BITS/SEC (1X)
- 8251/8251A ASYNCHRONOUS ONLY REPLACEMENT
- REQUIRES NO ASYNCHRONOUS SYSTEM CLOCK
- 28 PIN PLASTIC OR CERAMIC
- +5 VOLT ONLY

SYSTEM COMPATIBILITY

- DOUBLE BUFFERING OF DATA
- 8 BIT BI-DIRECTIONAL BUS FOR DATA, STATUS, AND CONTROL WORDS
- ALL INPUTS AND OUTPUTS TTL COMPATIBLE
- CHIP SELECT, $\overline{RE}$, $\overline{WE}$, C/$\overline{D}$ INTERFACE TO CPU
- ON-LINE DIAGNOSTIC CAPABILITY
- THREE STATE DATA BUS

BAUD RATE-DC TO 36K BITS/SEC (16X)
SELECTABLE CLOCK RATES

- 1X, 16X, 64X, BAUD RATE CLOCK INPUTS
- UP TO 47% DISTORTION ALLOWANCE WITH 64X CLOCK

APPLICATIONS

ASYNCHRONOUS COMMUNICATIONS
SERIAL/PARALLEL INTERFACE

GENERAL DESCRIPTION

The WD1983 is an N channel silicon gate MOS/LSI device that interfaces a digital asynchronous channel with a parallel channel. It is available in a ceramic or plastic standard 28 pin dual in line package.

The WD1983 is a fully programmable microprocessor I/O peripheral with two control registers and a status register. It is capable of full duplex operations.

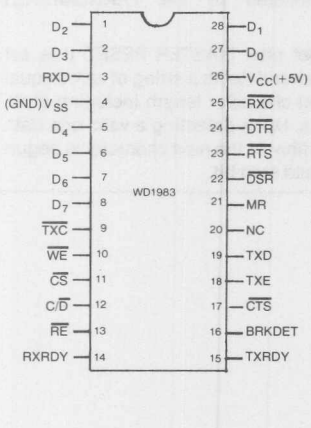


FIGURE 1 WD1983 PIN-OUT

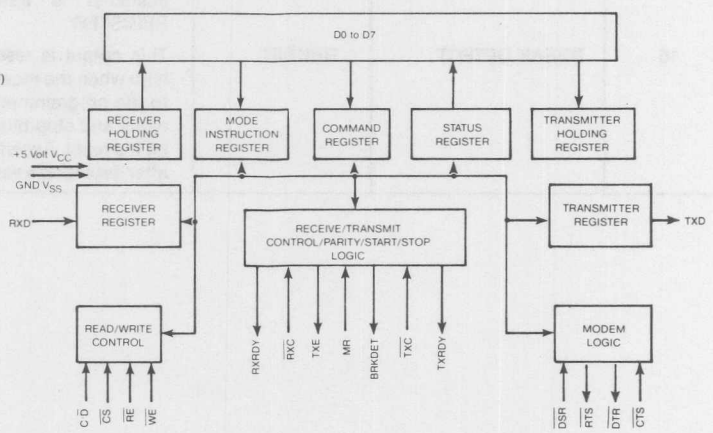


FIGURE 2 WD1983 BLOCK DIAGRAM

PIN NUMBER	PIN NAME	SYMBOL	FUNCTION
1, 2, 5, 6, 7, 8, 27, 28	DATA BUS	D0 THRU D7	These are input/output pins. Data on the DATA BUS is written into the selected register during a WRITE operation. During a READ operation, the DATA BUS is driven by data in the selected register. When not selected, ($\overline{CS}$ high), these pins are in a high impedance state.
3	RECEIVE DATA	RXD	This input is the received serial data.
4	POWER GND	V_{SS}	Ground
9	TRANSMIT CLOCK	$\overline{TXC}$	This input is the source clock for transmission. MODE INSTRUCTION word bits MR0 & MR1, control 1X, 16X, or 64X, times the transmitted bit rate.
10	WRITE ENABLE	$\overline{WE}$	This input, when low, writes the data on the DATA BUS into the addressed register.
11	CHIP SELECT	$\overline{CS}$	This input, when low, enables READ or WRITE operations.
12	CONTROL/DATA	C/$\overline{D}$	This input selects the CONTROL or DATA register. It is used in conjunction with a READ or WRITE enable.
13	READ ENABLE	$\overline{RE}$	This input, when low, accesses the contents of the addressed register.
14	RECEIVER READY	RXRDY	This output is set low after MASTER RESET. When set high it indicates that the receiver has assembled a character and transferred it to the RECEIVER HOLDING REGISTER. It is automatically reset when the RECEIVER HOLDING REGISTER is read.
15	TRANSMIT READY	TXRDY	This output is set high after MASTER RESET. It indicates that the transmitter is ready to accept a character. It will be set low whenever a character is written into the TRANSMITTER HOLDING REGISTER and will be set high again as soon as a character is transfered to the TRANSMITTER REGISTER.
16	BREAK DETECT	BRKDET	This output is reset after MASTER RESET. It is set high when the receiver detects a string of zeros equal to the programmed character length including start, parity and stop bits. Upon detecting a valid one data bit it's reset. Assembly of the next character is begun after detecting a valid start bit.

PIN NUMBER	PIN NAME	SYMBOL	FUNCTION
17	CLEAR TO SEND	$\overline{CTS}$	This input is set low to enable the transmitter. When set high it disables transmission. If the transmitter is transmitting a character, it will terminate transmission after the TRANSMITTER REGISTER is empty.
18	TRANSMIT EMPTY	TXE	This output is set high after MASTER RESET and is set low as soon as a character is transferred from the TRANSMITTER HOLDING REGISTER into the TRANSMITTER REGISTER. It returns to a high at the end of a transmitted character indicating the end of transmission if the TRANSMIT HOLDING REGISTER has not been loaded.
19	TRANSMIT DATA	TXD	This output is the transmit serial data. When no data is being transmitted or after MASTER RESET, this output is high (a marking condition). COMMAND CONTROL word bit 3 is used to program a break condition by forcing the TXD output to a low (spacing condition).
20		NC	No internal connection, pin not used.
21	MASTER RESET	MR	This input, when high, initializes the device and clears the COMMAND and MODE REGISTERS.
22	DATA SET READY	$\overline{DSR}$	This is a general purpose input which is sensed in STATUS REGISTER bit #7.
23	REQUEST TO SEND	$\overline{RTS}$	This is a general purpose output which is set and cleared by COMMAND word bit CR5. It is reset after MASTER RESET.
24	DATA TERMINAL READY	$\overline{DTR}$	This is a general purpose output which is set and cleared by COMMAND word bit CR1. It is reset after MASTER RESET.
25	RECEIVE CLOCK	$\overline{RXC}$	This input is the receiver clock. MODE INSTRUCTION word bits MR0 & MR1 control whether this input is 1X, 16X or 64X times the received bit rate.
26	POWER SUPPLY	V_{CC}	+5 Volts

REGISTERS, which buffer Transmit and Receive DATA. They are the TRANSMIT HOLDING REGISTER and the RECEIVE HOLDING REGISTER. There is a parallel-to-serial shift register (the TRANSMIT REGISTER) and a serial-to-parallel shift register (the RECEIVE REGISTER).

Operational control and monitoring of the BOART is performed by two CONTROL REGISTERS (the COMMAND INSTRUCTION REGISTER and the MODE INSTRUCTION REGISTER) and the STATUS REGISTER.

A READ/WRITE control circuit allows monitoring/programming or reading/loading in the CONTROL, STATUS or HOLDING REGISTERS by activating the appropriate control lines: Chip Select ($\overline{CS}$), Read Enable ($\overline{RE}$), Write Enable ($\overline{WE}$) and Control or Data Select (C/$\overline{D}$).

Internal control of the BOART is by means of two internal MICROCONTROLLERS; one for transmit and one for receive. The CONTROL REGISTERS, MODEM CONTROL LOGIC, READ/WRITE CONTROL LOGIC and various counters provide inputs to the MICROCONTROLLERS, which generate the necessary control signals to send and receive serial data according to the programmed asynchronous format.

READ/WRITE OPERATIONS

The WD1983 must be initialized after a MASTER RESET pulse by first writing the MODE INSTRUCTION word and then the COMMAND INSTRUCTION word. Thereafter, every control write to the device is interpreted as a COMMAND word. If it is desired to re-program the MODE REGISTER, a COMMAND REGISTER bit, INTERNAL RESET (CR6), allows the next control write data to be entered into the MODE REGISTER.

The WD1983 registers are accessed according to the following table:

$\overline{CS}$	C/$\overline{D}$	$\overline{RE}$	$\overline{WE}$	REGISTERS SELECTED
L	L	L	H	Read RECEIVE HOLDING REGISTER
L	L	H	L	Write TRANSMIT HOLDING REGISTER
L	H	L	H	Read STATUS REGISTER
L	H	H	L	Write CONTROL REGISTER
H	X	X	X	DATA BUS tri-stated

Note: "L" means V_{IL} at pins
"H" means V_{IH} at pins
"X" means don't care

nected to the microprocessor's data bus and system control bus. The appropriate $\overline{TXC}$ and $\overline{RXC}$ clock frequencies should be selected for the particular application using a programmable baud rate generator such as the BR1941.

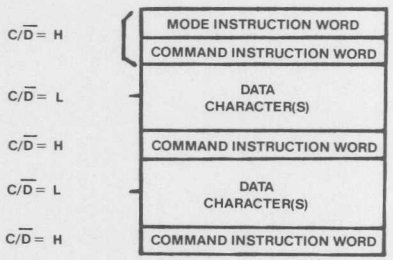
For typical data communication applications, the RXD and TXD input/outputs can be connected to RS-232C interface circuits or a modem.

The TXRDY, RXRDY, TXE and BRKDET Flags may be connected to the microprocessor system as interrupt inputs or the STATUS REGISTER can be periodically read in a polled environment to support BOART operations.

MODEM CONTROL SIGNALS can be configured several ways as the $\overline{DTR}$, $\overline{RTS}$ and $\overline{DSR}$ signals are controlled and sensed by the CPU through the COMMAND and STATUS REGISTERS. The $\overline{CTS}$ input is used to synchronize the transmitter to external events.

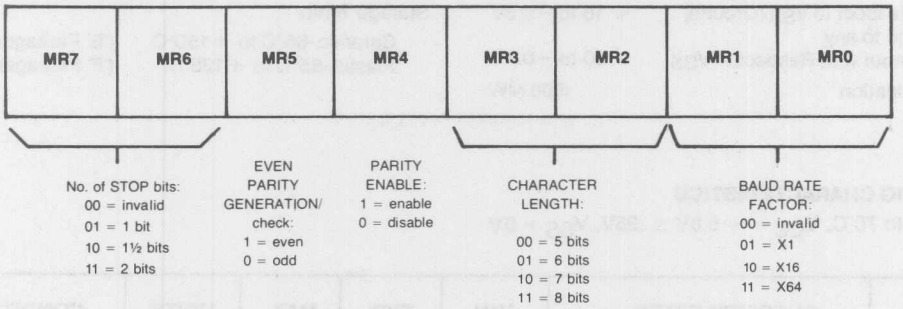
The SBRK bit of the COMMAND REGISTER (CR3) is used to send a Break Character. (A break character is defined as a start bit, and all zero data, parity and stop bits). When the CR3 bit is set to a "1", it causes the transmitter output, TXD, to be forced low after the last word is transmitted.

The receiver is equipped with logic to look for a break character. When a break character is received, the BREAK DETECT (BRKDET) FLAG and STATUS bit are set to logic "1". When the receiver input line goes high again for the least "one data bit time," the receiver resets the BREAK DETECT FLAG and resumes its search for a start bit.



TYPICAL DATA BLOCK TRANSFER

MODE INSTRUCTION CONTROL WORD FORMAT



COMMAND INSTRUCTION CONTROL WORD FORMAT

CR7	CR6	CR5	CR4	CR3	CR2	CR1	CR0
DON'T CARE	INTERNAL RESET (IR) 1 = returns WD1983 to mode instruction word format	REQUEST TO SEND ($\overline{RTS}$): 1 = forces $\overline{RTS}$ output low 0 = forces $\overline{RTS}$ output high	ERROR RESET (ER): 1 = resets PE, OE & FE error flags 0 = normal operation	SEND BREAK CHARACTER (SBRK): 1 = forces TXD output low 0 = normal operation	RECEIVE ENABLE (RXE): 1 = enable receiver 0 = disable receiver	DATA TERMINAL READY ($\overline{DTR}$): 1 = forces $\overline{DTR}$ output low 0 = forces $\overline{DTR}$ output	TRANSMIT ENABLE TXEN: 1 = enable transmitter 0 = disable transmitter

STATUS WORD FORMAT

SR7	SR6	SR5	SR4	SR3	SR2	SR1	SR0
$\overline{DSR}$ (SEE NOTE)	BRKDET (SEE NOTE)	FRAMING ERROR (FE): 1 = invalid stop bit detected at the end of the character 0 = No framing error detected (Reset by CR4)	OVERRUN ERROR (OE): 1 = CPU did not read the character before the next one became available 0 = No overrun error detected (Reset by CR4)	PARITY ERROR (PE): 1 = parity error detected 0 = No Parity error detected (Reset by CR4)	TXE (SEE NOTE)	RXRDY (SEE NOTE)	TXRDY (SEE NOTE)

FE, OE & PE FLAGS DO NOT INHIBIT OPERATION. THESE FLAGS ARE STATUS ONLY.

NOTE:
SR0, SR1, SR2, SR6, and SR7 HAVE IDENTICAL MEANINGS AS THE EXTERNAL OUTPUT PINS.

ABSOLUTE MAXIMUM RATINGS

V_{DD} with Respect to V_{SS} (Ground)	+ 15 to −0.3V	Storage Temp.	
Max. Voltage to any Input with Respect to V_{SS}	+ 20 to −0.3V	Ceramic -65°C to +150°C	('E' Package)
		Plastic -55°C to +125°C	('F' Package)
Power Dissipation	1000 MW		

OPERATING CHARACTERISTICS

T_A = 0°C to 70°C, V_{CC} = + 5.0V ± .25V, V_{SS} = 0V

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNITS	CONDITIONS
I_{LI}	Input Leakage			10	μA	$V_{IN} = V_{CC}$
I_{DL}	Data Bus Leakage			50	μA	Data Bus is in high impedence state
ICC_{AVE}	V_{CC} Supply Current		45	80	mA	5.25 VDC/f_{CLK} = 600 kHz No Loads.
V_{IH}	Input High Voltage	2.4		0.8	V	
V_{IL}	Input Low Voltage (All Inputs)	−0.3			V	
V_{OH}	Output High Voltage	2.4			V	I_O = − 100μA (source)
V_{OL}	Output Low Voltage			0.45	V	I_O = 1.6 mA (sink)

TABLE 1 WD1983 DC CHARACTERISTICS

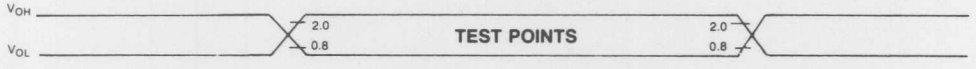


FIGURE 3 INPUT WAVEFORMS FOR AC TESTS

NOTE: ALL WAVEFORMS ARE MEASURED AT 2.0V IF RISING EDGE, AND 0.8V IF FALLING EDGE.

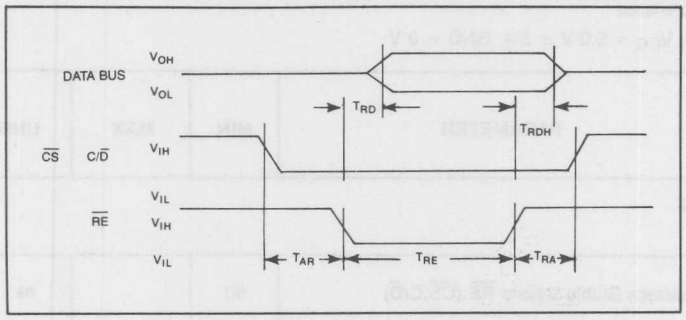


FIGURE 4 READ TIMING

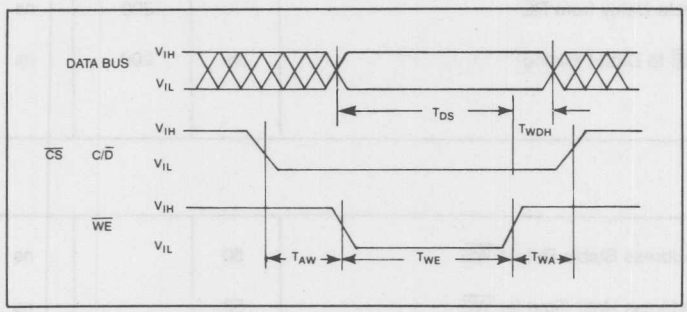


FIGURE 5 WRITE TIMING

NOTE:

8251A COMPATIBILITY

The WD1983 (BOART) is an asynchronous only device, which is compatible with the 8251A. However, in test evaluation and application, the following differences should be noted:

(1) The WD1983 utilizes the transmit and receive baud clocks in their respective internal logic sections instead of the system clock normally applied to Pin 20 on the 8251A. This Pin on the WD1983 is not used.

(2) As a result of the above condition, timings referenced to the system clock period in the 8251A specification are now specified in absolute time units or with respect to the transmit or receive baud clock.

SYMBOL	PARAMETER	MIN	MAX	UNIT	TEST CONDITIONS
BUS PARAMETERS READ CYCLE					
t_{AR}	Address Stable Before $\overline{RE}$ ($\overline{CS}$,C/$\overline{D}$)	50		ns	
t_{RA}	Address Hold Time for $\overline{RE}$ ($\overline{CS}$,C/$\overline{D}$)	50		ns	
t_{RE}	$\overline{RE}$ Pulse Width	230		ns	
t_{RD}	Data Delay from $\overline{RE}$		200	ns	C_L = 50pF
t_{RDH}	$\overline{RE}$ to Data Floating	25	200	ns	C_L (Max) = 50pF C_L (Min) = 15pF
WRITE CYCLE					
t_{AW}	Address Stable Before $\overline{WE}$	50		ns	
t_{WA}	Address Hold Time for $\overline{WE}$	50		ns	
t_{WE}	$\overline{WE}$ Pulse Width	230		ns	
t_{DS}	Data Set-Up Time for $\overline{WE}$	TWE		ns	
t_{WDH}	Data Hold Time for $\overline{WE}$	100		ns	
OTHER TIMINGS					
t_{DTX}	TXD Delay from Falling Edge of TXC		1000	ns	C_L = 100pF
t_{SRX}	RX Data Set-Up Time to Sampling Pulse	200		ns	C_L = 100pF
t_{HRX}	RX Data Hold Time to Sampling Pulse	200		ns	C_L = 100pF
f_{TX} [1]	Transmitter Input Clock Frequency 1X Baud Rate 16X and 64X Baud Rate	 DC DC	 500 600	 kHz kHz	
t_{TPW}	Transmitter Input Clock Pulse Width 1X Baud Rate 16X and 64X Baud Rate	 1.0 500		 μs ns	

TABLE 2 WD1983 AC CHARACTERISTICS (CONTINUED)

SYMBOL	PARAMETER	MIN	MAX	UNIT	TEST CONDITION
t_{TPD}	Transmitter Input Clock Pulse Delay				
	1X Baud Rate	1.0		μs	
	16X and 64X Baud Rate	800		ns	
f_{RX}	Receiver Input Clock Frequency				
	1X Baud Rate	DC	500	kHz	
	16X and 64X Baud Rate	DC	600	kHz	
t_{RPW}	Receiver Input Clock Pulse Width				
	1X Baud Rate	1.0		μs	
	16X and 64X Baud Rate	800		ns	
t_{RPD}	Receiver Input Clock Pulse Delay				
	1X Baud Rate	1.0		μs	
	16X and 64X Baud Rate	800		ns	
t_{TX}	TXRDY Delay from Center of Data Bit		8	t_{RXC}	C_L = 50pF (16X)
t_{RX}	RXRDY Delay from Center of Data Bit		1/2	t_{RXC}	
t_{IS}	Internal BRKDET Delay from Center of Data Bit		1	t_{RXC}	
t_{TRD}	TXRDY Delay from Falling Edge of $\overline{WE}$		1	t_{TXC}	
t_{TOD}	TXD Output from Falling Edge of $\overline{WE}$		2	t_{TXC}	
t_{WC}	Control Delay from Rising Edge of $\overline{WE}$ ($\overline{DTR}$, $\overline{RTS}$)		400	ns	
t_{CR}	Control to $\overline{RE}$ Set-Up Time ($\overline{DSR}$, $\overline{CTS}$)		1	TXC	
t_{MR}	Master Reset Pulse Width	500		ns	

TABLE 2 WD1983 AC CHARACTERISTICS

At f_{TX} (max), the duty cycle should be 50%. At less than f_{TX} (max), the minimum pulse width for the high or low half is $\frac{1}{2 \bullet f_{TX}(max)}$.
Hence, at frequencies less than f_{TX} (max), the required duty cycle will be less stringout than 50%.

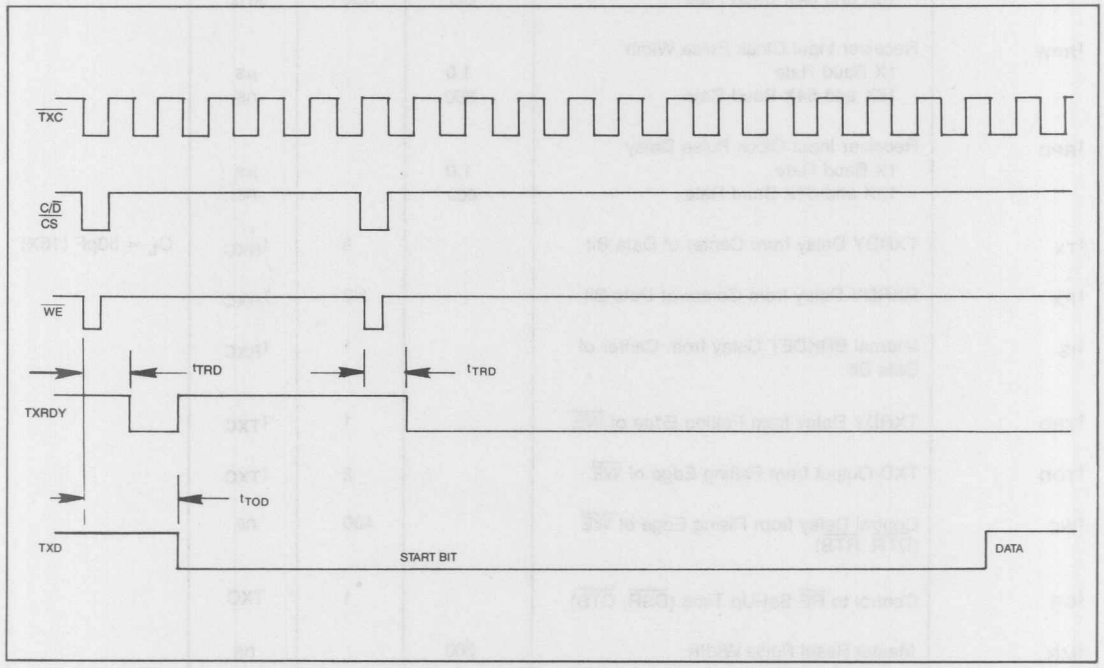


FIGURE 6

TRANSMITTER OUTPUT TIMINGS WITH RESPECT TO TRANSMIT CLOCK

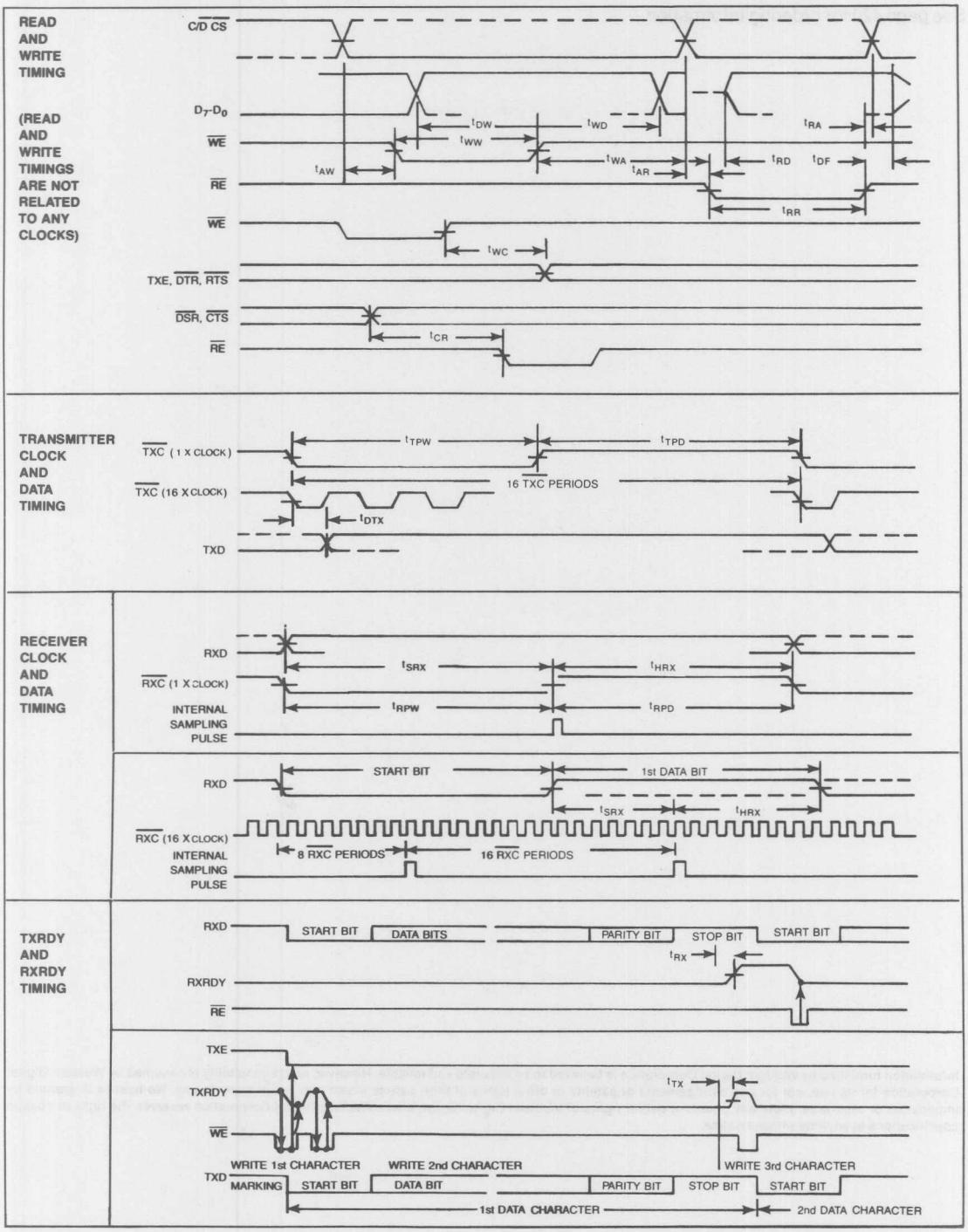


FIGURE 7 SYSTEM TIMING DIAGRAMS

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WD1993 Arinc 429 Receiver/Transmitter

FEATURES

- PRESENT UPON MASTER RESET FOR ARINC 429 PROTOCOL
- PROGRAMMABLE WORD LENGTH FROM 1 CHARACTER TO 8 CHARACTERS
- PROGRAMMABLE CHARACTER LENGTH, 5, 6, 7, OR 8 BITS
- RETURN TO ZERO (RZ) OUTPUT
- AUTO SPACE GENERATION
- DOUBLE BUFFERED RECEIVER AND TRANSMITTER
- UNDERRUN ERROR DETECTION FOR TRANSMISSION
- OVERRUN, FRAMING AND PARITY ERROR DETECTION ON RECEIVER
- WORD ERROR FLAG FOR COMPREHENSIVE ERROR REPORTING
- FIRST CHARACTER OF WORD FLAG FOR SINGLE INTERRUPT APPLICATIONS
- DIAGNOSTIC LOCAL LOOP-BACK TEST MODE
- DC TO 200 KILOBITS PER SECOND OPERATION
- TTL COMPATIBLE INPUTS AND OUTPUTS
- SINGLE +5 VOLT SUPPLY
- TEMPERATURE RANGES 0°C to 70°C, — 1993-03, −40°C to +85°C — 1993-02, −55°C to +125°C — 1993-01

INTRODUCTION

The Western Digital WD1993 Avionic Receiver/Transmitter is designed to handle digital data transmission, according to the Avionic Arinc 429 protocol. Also, the word length is programmable from one to eight characters of 5, 6, 7, or 8 bits. Parallel data is converted into a serial data stream during transmission and serial to parallel during reception. The WD1993 is packaged in a 28 pin plastic or ceramic package and is available in three temperature ranges: Commercial, Industrial and Military.

GENERAL DESCRIPTION

The WD1993 is a bus-orientated MOS/LSI device designed to provide the Avionics Arinc 429 Data Communication Protocol, along with programmable character length capabilities.

Also, the WD1993 contains a local loop-back test mode of operation, which is controlled by the Loop Test Enable (LTE) bit in the command register. In this diagnostic mode, the transmitter output is "looped-back" into the receiver input. The REN and TEN control bits must also be active ("1") and the CTS input must be low. The status and output flags operate normally.

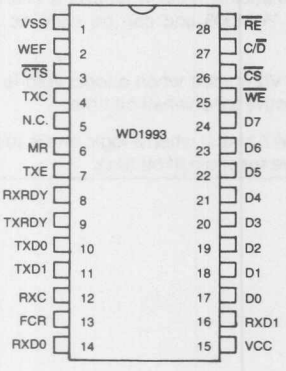


Figure 1 PIN DIAGRAM

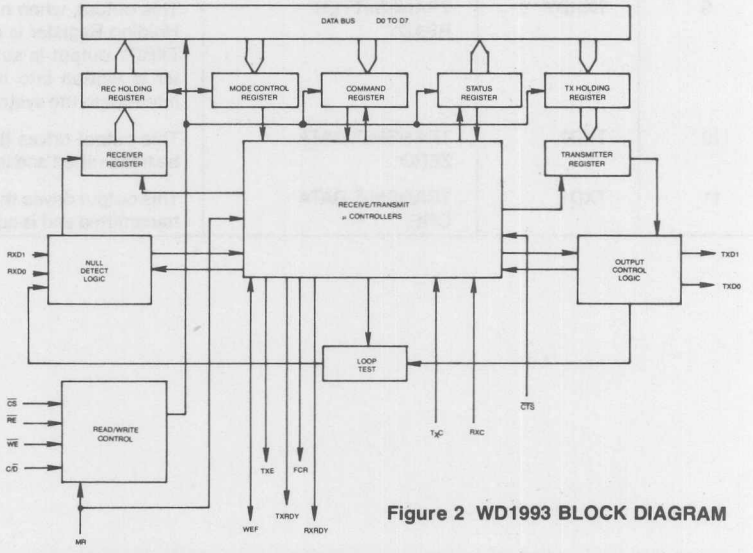


Figure 2 WD1993 BLOCK DIAGRAM

PIN NO.	SYMBOL	SIGNAL NAME	FUNCTION
1	VSS	GROUND	Ground
2	WEF	WORD ERROR FLAG	This pin is an output, which when active indicates an error in either the transmitter or receiver has been detected. It reflects an underrun, overrun, parity or framing (receive word) error and is intended as an error interrupt. The Status Register should be read to determine the specific error.
3	$\overline{CTS}$	CLEAR-TO-SEND	This input is activated (V_{IL}) to enable the transmitter logic.
4	TXC	TRANSMIT CLOCK	This input is the source clock for transmission. The data rate is a function of this clock frequency. ARINC MODE = 4 × bit rate
5	N.C.		No Internal Connection
6	MR	MASTER RESET	When active (V_{IH}), presets the WD1993 mode and command registers to the ARINC protocol. Master Reset also resets the data registers and places the WD1993 transmitter and receiver into idle states. After MR, the command register is set to 00100101 and the mode register is set to 00111100.
7	TXE	TRANSMITTER EMPTY	This output goes high to indicate the end of a transmit operation. TXE is automatically reset after the Transmit Holding Register is loaded.
8	RXRDY	RECEIVER READY	This output, when high, alerts the CPU that the Receiver Holding Register contains a data character that is ready to be input. This output is automatically reset whenever a character is read from the WD1993. RXRDY is enabled unless inhibited by setting command bit CR3 (RXRDYIN) to a logic "1." It is automatically enabled again after a receive sequence is completed.
9	TXRDY	TRANSMITTER READY	This output, when high, alerts the CPU that the Transmit Holding Register is ready to accept a data character. The TXRDY output is automatically reset whenever a character is written into the WD1993 and can be used as an interrupt to the system.
10	TXD0	TRANSMIT DATA ZERO	This output drives the V/Z circuit when a logic zero is to be transmitted and is active for one-half bit time.
11	TXD1	TRANSMIT DATA ONE	This output drives the V/Z circuit when a logic one is to be transmitted and is active for one-half bit time.

PIN NO.	SYMBOL	SIGNAL NAME	FUNCTION
12	RXC	RECEIVE CLOCK	This input is the source clock for reception. The data rate characteristics are the same as the transmit clock.
13	FCR	FIRST CHARACTER READY	This output goes high after the receiver has completed reception of the first character in a multi-character sequence.
14	RXD0	RECEIVE DATA ZERO	RXD0 is driven by the line V/Z receiver circuit. When the V/Z circuit detects a logic zero, a TTL logic one (active for one-half bit time) is provided to the WD1993.
15	VCC	POWER SUPPLY	+5V DC
16	RXD1	RECEIVE DATA ONE	The RXD1 input is driven by the V/Z line receiver. Each time the V/Z circuit detects a logic one, a TTL level logic one (active for one-half bit time) is provided to this input.
17 18 19 20 21 22 23 24	D0 D1 D2 D3 D4 D5 D6 D7	DATA BUS	This is the bi-directional data bus. It is the means of communication between the WD1993 and the CPU. Control, Mode, Data and Status Registers are accessed via this bus.
25	$\overline{WE}$	WRITE ENABLE	When active (V_{IL}), allows the CPU to write into the selected register.
26	$\overline{CS}$	CHIP SELECT	When active (V_{IL}), the device is selected. This enables communication between the WD1993 and a microprocessor.
27	C/$\overline{D}$	CONTROL/DATA	This input is used in conjunction with an active read or write operation to determine register access via the DATA BUS.
28	$\overline{RE}$	READ ENABLE	When active (V_{IL}), allows the CPU to read data or status information from the WD1993.

ORGANIZATION

A block diagram of the WD1993 is shown in figure 2.

As mentioned, the WD1993 is an eight bit bus-oriented device. Communication between the WD1993 and the controlling CPU occurs via the 8 bit data bus through the bus transceivers. There are 2 accessible data registers, which buffer transmit and receive data. They are the Transmit Holding Register and the Receive Holding Register. There is a parallel-to-serial shift register (parallel in-serial out), the transmit register and a serial-to-parallel shift register (serial in-parallel out), the receive register.

Operational control and monitoring of the WD1993 is performed by two control registers (the command instruction register and the mode instruction register) and the status register.

A read/write control circuit allows programming/monitoring or loading/reading of data in the control, status or holding registers by activating the appropriate control lines: Chip Select ($\overline{CS}$), Read Enable ($\overline{RE}$), Write Enable ($\overline{WE}$), and Control or Data Select (C/$\overline{D}$).

Internal control of the WD1993 is by means of two internal microcontrollers; one for transmit and one for receive. The control registers, null detect logic and various counters, provide inputs to the microcontrollers which generate the necessary control signals to send and receive serial data according to the Arinc 429-1 protocol, along with the programmable multicharacter capabilities.

OPERATION

Upon master reset (MR), the device is programmed to transmit and receive four 8-bit contiguous characters with the 32nd bit odd parity. (ARINC protocol.)

A minimum four bit time space is automatically inserted after the character transmission. Two receiver inputs, RXD1/RXD0 and two transmitter outputs, TXD1/TXD0, are provided to interface with voltage—impedance (V/Z) circuits to translate ± 10 volt ARINC line levels to 5 volt TTL logic levels. The transmit clock (TXC) and receive clock (RXC), in ARINC mode, are four times (4X) the bit rate desired.

The receiver monitors the received data input to detect a four bit time null, which delimits the word. If the communications link is broken during a word reception, the receiver will generate a word error flag to (WEF) to notify the CPU to request retransmission. When a null is detected, the receiver logic is reset and returned to an idle state awaiting the next word.

The WD1993 may also be programmed to support a multiple character word consisting of from one to eight characters. Also, the character length is programmable from 5 to 8 bits, and the parity bit if parity is used, may be either inside or outside the word.

The Command Register is used to select features such as parity options, loop test capability, RXRDY flag enabling, transmitter and receiver enabling, and may also cause the WD1993 to return to the Mode instruction.

The Mode Register is used to select features such as bits/character and characters/word.

The Status Register contains information such as Transmitter Ready, Transmitter Empty, Receiver Ready, error conditions, and First Character Ready.

OPERATING DESCRIPTION

The WD1993 is primarily designed to operate in an 8 bit micro-processor environment, although other control logic schemes are easily implemented. The DATA BUS and the Interface Control Signals ($\overline{CS}$, $\overline{RE}$, $\overline{WE}$ and C/$\overline{D}$) should be connected to the microprocessor's data bus and system control bus.

The appropriate TXC and RXC clock frequencies should be selected for the particular application, using a programmable baud rate generator such as a BR1941. A master reset pulse initializes the WD1993 and presets the control registers to the ARINC protocol.

The RXD1/RXD0 inputs are interfaced to the DITS data line via external level translators that provide TTL (5V) logic levels to the WD1993. The TXD1/TXD0 outputs are connected to high voltage (± 10V) driver circuits. Figures 16 and 17 show some typical ± 10V translator and driver circuits.

The TXRDY, RXRDY, FCR and WEF Flags may be connected to the microprocessor system as interrupt inputs. The status register can be periodically read in a polled environment to support WD1993 operations.

The $\overline{CTS}$ input can be used to synchronize the transmitter to external events.

The WD1993 is designed such that a control register write operation accesses the command instruction register.

The RXRDYIN bit of the command register is used to inhibit the RXRDY output pin for ARINC operations.

MULTI-CHARACTER OPERATIONS

As discussed above, the WD1993 is equipped with a multicharacter option which provides the user with the means of transmitting and receiving multiple contiguous characters of data within one set of delimiters—4 bit nulls for ARINC 429. Since the WD1993 is an 8 bit bus-oriented device, the controlling processor must read the WD1993 data from its holding register before the subsequent characters are assembled. This situation also exists on the transmit side, i.e., the Transmit Holding Register must be loaded before the previous 8 bits are completely shifted out of the transmit register.

Several "flags" are provided for interrupt purposes so that continuity is maintained and data integrity is preserved. These flags are First Character Ready (FCR), Receiver Ready (RXRDY), Transmitter Ready (TXRDY) and Transmitter Empty (TXE).

The Transmitter operates as follows:

a) With the mode and command registers programmed as desired, the transmitter is enabled, TEN (CR0) = "1".

b) The TXE and TXRDY flags are "1" (active).

c) The external $\overline{CTS}$ signal = "0".

d) The CPU loads data into the Transmitter Holding Register, TXE and TXRDY go Low.

e) The data is loaded into the transmit register and TXRDY goes high. This indicates the first data word is being sent and a character can be loaded into the holding register. If the WD1993 is programmed for more than one character (multi-character) then an underrun error will be generated if the next character is not loaded before the previous word is completely shifted out, unless the current character is the last character in a sequence.

f) If the last character is transmitted and no more new data is to be sent, the transmitter will indicate its status by raising the TXE flag. (No error is generated as a result of this condition.)

The Receiver operates similarly:

a) With the control registers suitably programmed, the receiver is enabled, REN (CR2) = "1".

b) The RXRDY and FCR flags are "0". (Inactive).

c) The incoming data word activates the receive logic and the data begins to be assembled in the receive register.

d) When the first character is completely assembled, the data is loaded into the Receive Holding Register, the FCR (First Character Ready) and RXRDY (Receiver Ready) flags become active, "1". The CPU should read the data prior to the reception of the next character or an overrun error will be generated as the receiver will overwrite the old data with the new data character just received.

The exception to this is in the ARINC mode, where the first character in the ARINC protocol contains a label. The FCR and RXRDY Flags become active to indicate the reception of the first character of data. The CPU reads the first character and decides whether or not it wants to acquire the subsequent characters. If not, then the CPU performs a "control write" to the COMMAND REGISTER, setting the RXRDYIN (CR3) bit to a "1". This bit in ARINC mode, inhibits the RXRDY flag from interrupting the CPU during the reception of the 3 remaining characters. The RXRDYIN bit is then automatically reset upon completion of the receive sequence and RXRDY is enabled again.

LOOP TEST MODE

As mentioned, the WD1993 is equipped with a diagnostic test mode, local loop-back. This mode is activated by setting the LTE command bit to a "1". The TEN and REN bits should be "1" and $\overline{CTS}$ should be "V_{IL}". The receiver inputs are ignored and the transmitter outputs are sending nulls. The transmitter is internally "looped-back" to the receiver and the error and status flags operate normally.

For basic testing, failing to reload the Transmit Holding Register in the middle of a data send sequence will cause an underrun error in the transmitter and a word error in the receiver. Failure to read the Receive Holding Register after a FCR or RXRDY flag will cause an overrun error to be generated.

For Loop-Back test operations, the user should be sure that the TXC and RXC clock frequencies are the same. This is normally implemented by placing the same clock signal on both pins (TXC and RXC).

ARINC BACKGROUND

Aeronautical Radio Inc. (ARINC) publishes the ARINC 429 specification. This document defines the air transport industries standards for the transfer of digital data between avionics systems elements. This specification was adopted by The Airlines Electronic Engineering Committee April 11, 1978. By the adoption of this specification the foundation is set for a standard protocol governing all intersystems equipment (Line Replaceable Units).

MARK 33 DIGITAL INFORMATION TRANSFER SYSTEM (DITS)

Basic Philosophy

Transmit from a designated output port over a single twisted and shielded pair of wires to designated receiver.

Bidirectional data flow not permitted on a given pair.

Data Transfer

Numeric
Iso Alphabet #5
Graphic

Data Format

32 bits or less (unused bit positions should be filled with binary zeros or valid data pad bits).

Bit #32 is assigned to parity.

Modulation
Return to Zero (RZ)

Transmit Voltage Levels

high	+10	±0.5V
null	0	±0.5V
low	−10	±0.5V

Receiver Voltage Levels:

	(in absence of noise)	(noisy environment)
high	+6.0V to +10V	+5.0V to +13V
low	−6.0V to +10V	−5.0V to −13V

No damage to receiver up to 20 vac rms between A & B; +28, A to Gnd; −28, B to Gnd.

Data Rate
100 kilo bit per second ± 1%
Low speed 12 to 14.5 kilo bit per second ± 1%

Word Synchronization
All zero gap of a minimum of 4 bit times

REGISTER DEFINITIONS

The format and definition of the Command Register is shown below:

CR7	CR6	CR5	CR4	CR3	CR2	CR1	CR0
EPS	IR	PEN	LTE	RXRDYIN	REN	PIA	TEN

TEN — Transmit ENable
1 — Enabled
0 — Disabled

PIA — Parity Inside or After
1 — After the data word
0 — Inside (the last data bit) of word

REN — Receive ENable
1 — Enabled
0 — Disabled

RXRDYIN — RXRDY Inhibit
1 — Inhibit RXRDY output flag
0 — Normal transmitter operation enable RXRDY output flag

LTE — Loop Test ENable
1 — Local loop-back mode
0 — Normal Operation

PEN — Parity ENable
1 — Enabled
0 — Disabled

IR — Internal Reset
1 — Returns WD1993 to mode instruction
0 — format

EPS — Even Parity Select
1 — Even parity
0 — Odd parity

The format and definition of the Mode Register is shown below:

MR7	MR6	MR5	MR4	MR3	MR2	MR1	MR0
X	N3	N2	N1	CLS2	CLS1	X	X

CLS2	CLS1	Character Length Select
0	0	5 bits
0	1	6 bits
1	0	7 bits
1	1	8 bits

N3	N2	N1	Characters Per Word Select
0	0	0	1 character
0	0	1	2 characters
0	1	0	3 characters
0	1	1	4 characters
1	0	0	5 characters
1	0	1	6 characters
1	1	0	7 characters
1	1	1	8 characters

The WD1993 registers are addressed according to the following table:

$\overline{CS}$	C/$\overline{D}$	$\overline{RE}$	$\overline{WE}$	Registers Selected
L	L	L	H	Read Receive Holding Register
L	L	H	L	Write Transmit Holding Register
L	H	L	H	Read Status Register
L	H	H	L	Write Control Registers
H	X	X	X	Data Bus Tri-Stated

L = V_{IL} at pins
H = V_{IH} at pins
X = don't care

The format of the Status Register is shown below:

SR7	SR6	SR5	SR4	SR3	SR2	SR1	SR0
UE	FCR	WEF	OE	PE	TXE	RXRDY	TXRDY

TXRDY — Transmitter Ready

1 — Active (THR can be reloaded)
0 — Inactive (transmitter is busy)

RXRDY — Receiver Ready

1 — Active (RHR should be read)
0 — Inactive

TXE — Transmitter Empty

1 — Transmitter idle
0 — Transmitter active

PE — Parity Error

1 — Error reported
0 — No error

OE — Overrun Error

1 — RHR has been overwritten
0 — No error

WEF — Word Error Flag

1 — Indicates improper receive sequence (word error), overrun error, parity error, framing error or underrun error.
0 — No error

FCR — First Character Ready

1 — This bit indicates the receiver has just completed assembly of the 1st character in a multi-character sequence and that the data is contained in the RHR.
0 — First character not ready.

UE — Underrun Error

1 — Indicates that the THR has not been loaded with a new character in time for a contiguous data transmission sequence.
0 — No error

ABSOLUTE MAXIMUM RATINGS

Storage Temperature −55°C to +125°C (Plastic Package)
−65°C to +150°C (Ceramic Package)

Voltage on any Pin with Respect to Ground . . −0.3V to +7V
Power Dissipation . . . . . 400 MW

Note: Absolute maximum ratings indicate limits beyond which permanent damage may occur. Continuous operation at these limits is not intended and should be limited to those conditions specified under DC Electrical Characteristics.

DC ELECTRICAL CHARACTERISTICS

T_A = 0°C to +70°C; V_{CC} = 5.0V ± 5%; GND = 0V

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT	TEST CONDITIONS
V_{IL}	Input Low Voltage	−0.3		0.8	V	
V_{IH}	Input High Voltage	2.0		V_{CC}	V	
V_{OL}	Output Low Voltage			0.45	V	I_{OL} = 1.6mA
V_{OH}	Output High Voltage	2.4			V	I_{OH} = −100μA
I_{DL}	Data Bus Leakage			50	uA	Data Bus is in High Impedence State
				10	uA	
I_{IL}	Input Leakage			10	uA	V_{IN} = V_{CC}
I_{CC}	Power Supply Current		45	80	mA	V_{CC} = 5.25V No Load

CAPACITANCE

T_A = 25°C; V_{CC} = GND = ØV

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT	TEST CONDITIONS
C_{IN}	Input Capacitance			10	pF	f_C = 1MHz
$C_{I/O}$	I/O Capacitance			20	pF	Unmeasured pins returned to GND

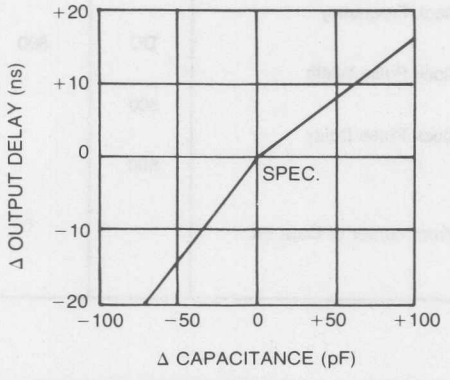


Figure 3 OUTPUT DELAY vs CAPACITANCE

A.C. TIMING PARAMETERS

SYMBOL	PARAMETER	MIN	MAX	UNIT	TEST CONDITIONS
BUS PARAMETERS					
Read Cycle (Reference Figure 6)					
t_{AR}	Address Stable before $\overline{RE}$, ($\overline{CS}$, C/$\overline{D}$)	50		ns	
t_{RA}	Address Hold Time for $\overline{RE}$, ($\overline{CS}$, C/$\overline{D}$)	5		ns	
t_{RE}	$\overline{RE}$ Pulse Width	350		ns	
t_{RD}	Data Delay from $\overline{RE}$		200	ns	C_L = 50 pF
t_{RDH}	$\overline{RE}$ to Data Floating		200	ns	C_L = 50 pF
		25		ns	C_L = 15 pF
WRITE CYCLE (Reference Figure 7)					
t_{AW}	Address Stable before $\overline{WE}$	20		ns	
t_{WA}	Address Hold Time for $\overline{WE}$	20		ns	
t_{WE}	$\overline{WE}$ Pulse Width	350		ns	
t_{DS}	Data Set-Up Time for $\overline{WE}$	200		ns	
t_{WDH}	Data Hold Time for $\overline{WE}$	40		ns	
OTHER TIMINGS (Reference Figures 8, 9)					
t_{DTX}	TXD Delay from Falling Edge of TXC		500	ns	C_L = 100 pF
t_{SRX}	Rx Data Set-up Time to Sampling Pulse	200		ns	C_L = 100 pF
t_{NRX}	Rx Data Hold Time to Sampling Pulse	100		ns	C_L = 100 pF
t_{TX}	Transmitter Input Clock Frequency				
	4×	DC	800	kHz	
t_{TPW}	Transmitter Input Clock Pulse Width				
	4×	500		ns	
t_{TPD}	Transmitter Input Clock Pulse Delay				
	4×	500		ns	
t_{RX}	Receiver Input Clock Frequency				
	4×	DC	800	kHz	
t_{RPW}	Receiver Input Clock Pulse Width				
	4×	500		ns	
t_{RPD}	Receiver Input Clock Pulse Delay				
	4×	500		ns	
				ns	
t_{TX}	TXRDY Delay from center of Data Bit		½	t_{TXC}	

A.C. TIMING PARAMETERS

SYMBOL	PARAMETER	MIN	MAX	UNIT	TEST CONDITION
t_{TX}	TXRDY Delay from Center of Data Bit	200 ns	2	t_{TXC}	(4x)
t_{RX}	RXRDY Delay from Center of Data Bit (FCR Delay from Center of Data Bit)		½	R_{RXC}	
	TXE Delay from Center of Data Bit		½	t_{TXC}	C_L = 50 pF 4 × Rate

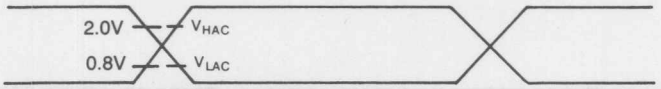


Figure 4 TEST POINTS FOR A.C. TIMING

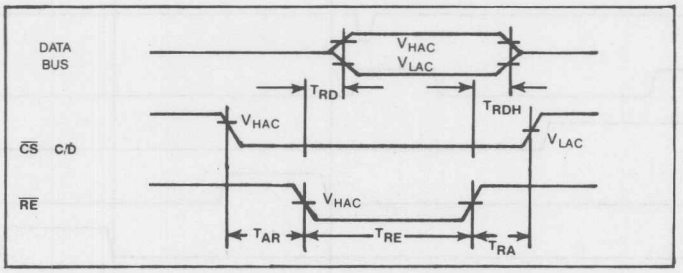


Figure 5 READ CYCLE TIMING

Note: AC timings measured at V_{OH} = 2.0V, V_{OL} = 0.8V and with test load circuit.

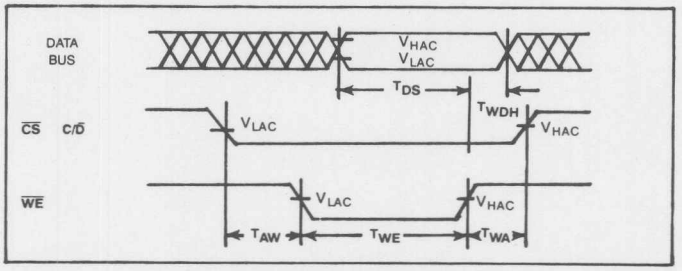


Figure 6 WRITE CYCLE TIMING

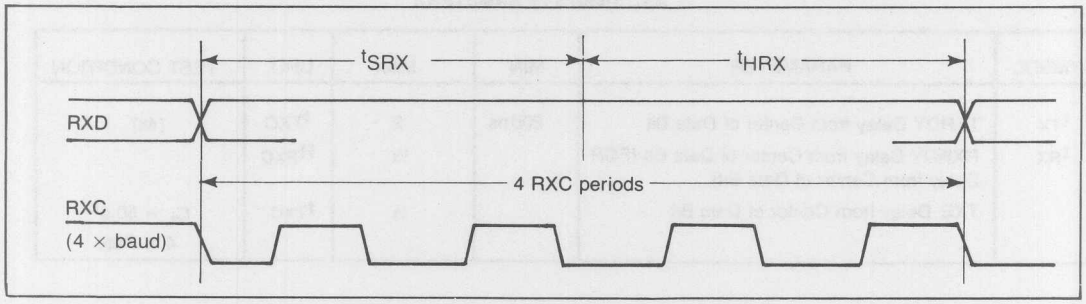


Figure 7 RECEIVER CLOCK AND DATA TIMINGS

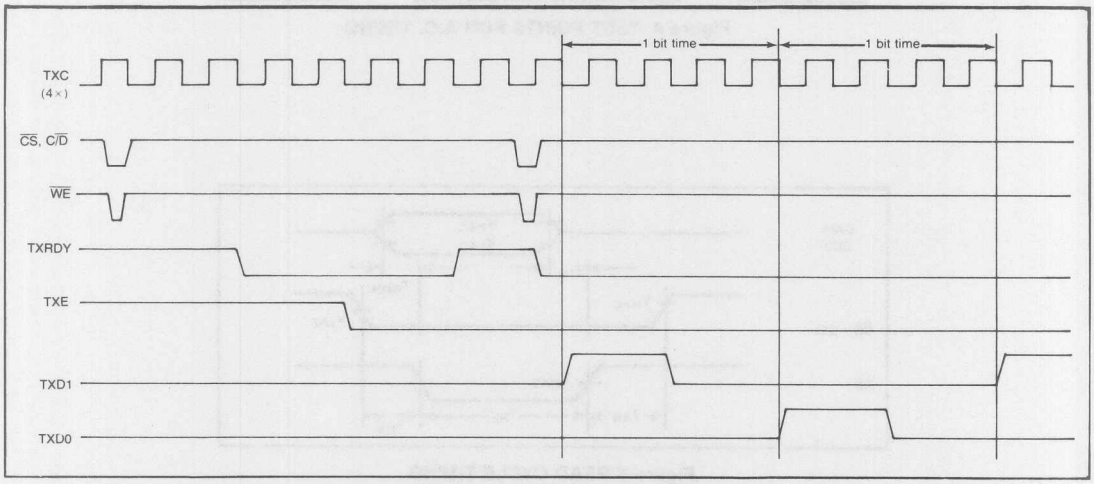


Figure 8 TRANSMITTER TIMINGS (ARINC MODE)

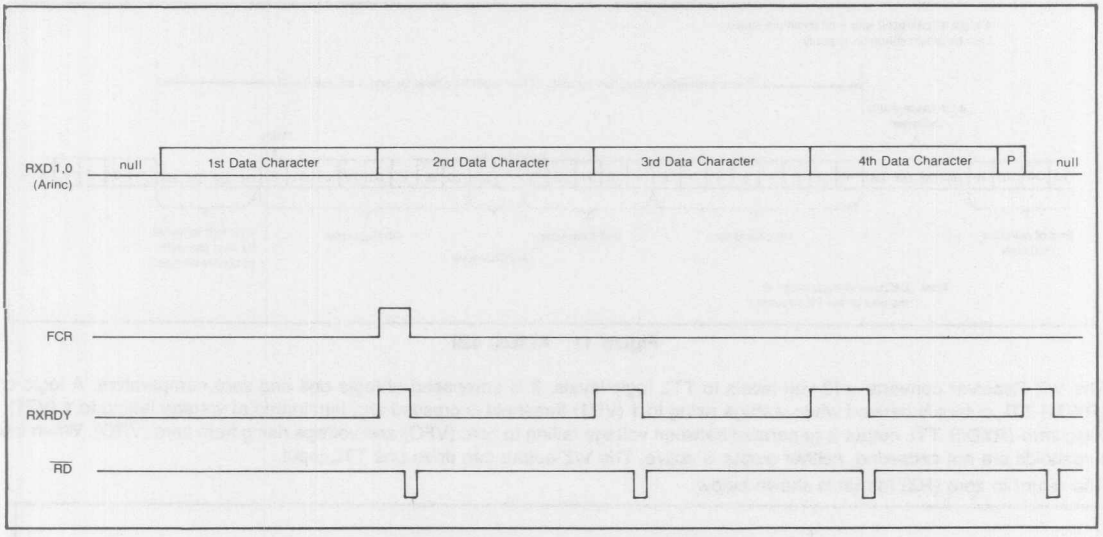


Figure 9 RXRDY AND FCR TIMING

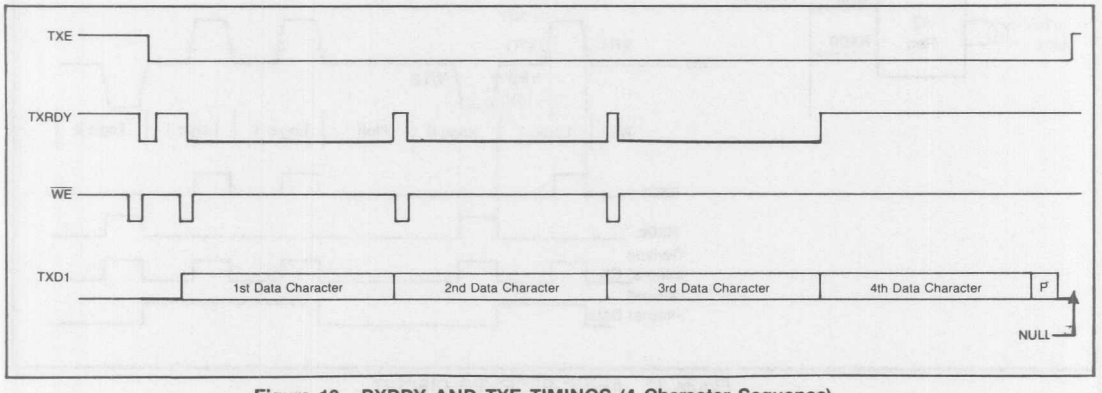


Figure 10 RXRDY AND TXE TIMINGS (4 Character Sequence)

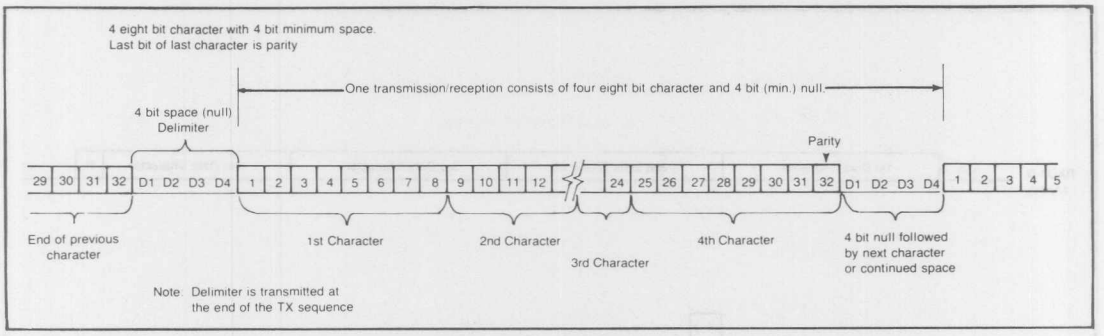


Figure 11 ARINC 429

The V/Z Receiver converts ±10 volt levels to TTL logic levels. It is composed of logic one and zero comparators. A logic one (RXD1) TTL output is derived when voltage rising to 1 (VR1) threshold is crossed and terminated at voltage falling to 1 (VF1). A logic zero (RXD0) TTL output is generated between voltage falling to zero (VFO) and voltage rising from zero (VRO). When input thresholds are not exceeded, neither output is active. The V/Z output can drive one TTL input.

The return to zero (RZ) format is shown below

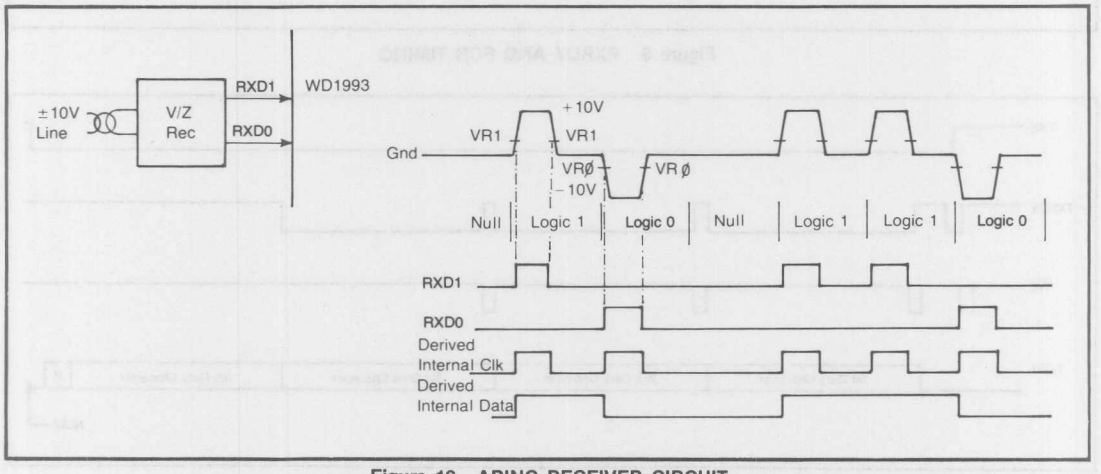


Figure 12 ARINC RECEIVER CIRCUIT

The V/Z Driver convert TTL logic levels into ± 10 volt levels. The TXD1 and TXD0 outputs of the WD1993 are used to drive the line drivers. Each output can drive one TTL load. When the outputs are not active, the line Driver should return to zero.

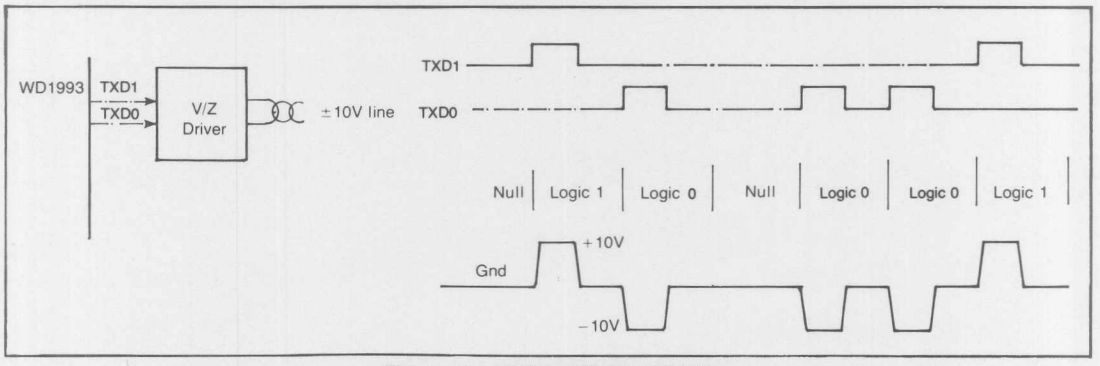


Figure 13 ARINC DRIVER CIRCUIT

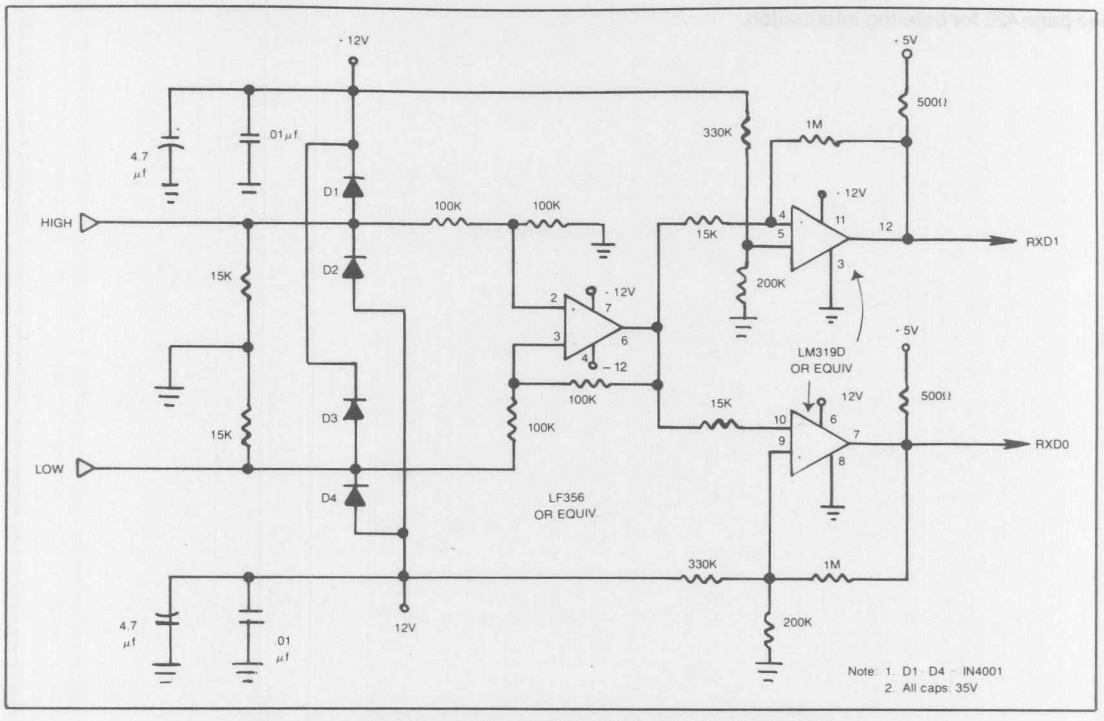


Figure 14 ARINC 429 LINE LEVEL TRANSLATOR (RECEIVER)

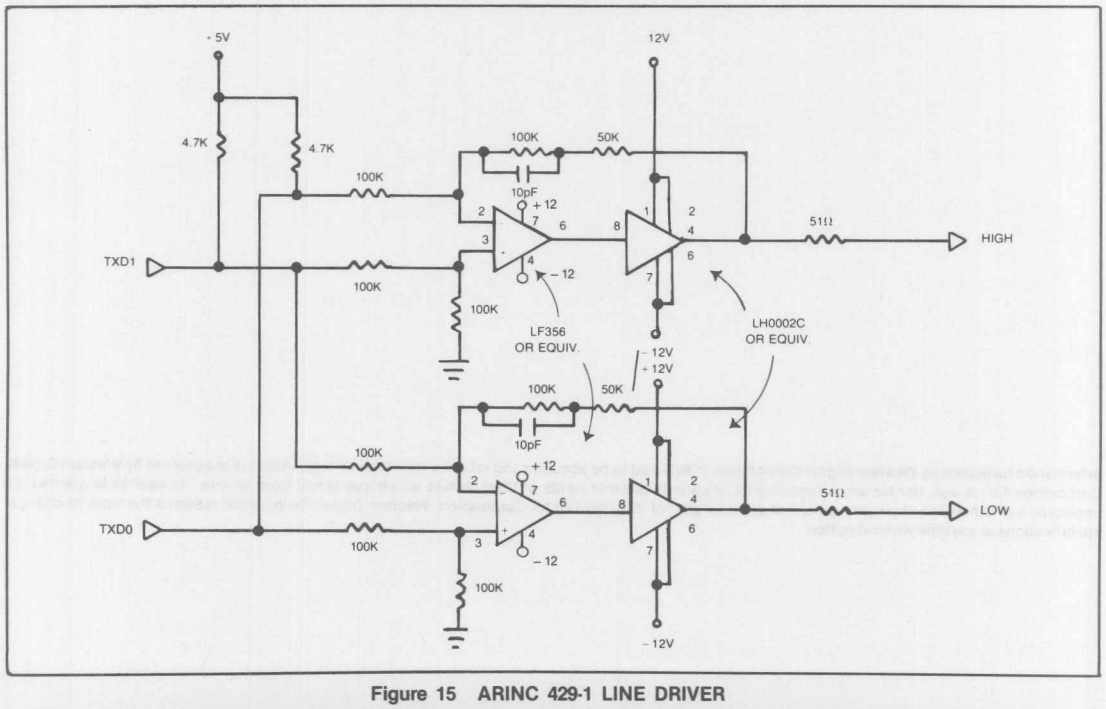
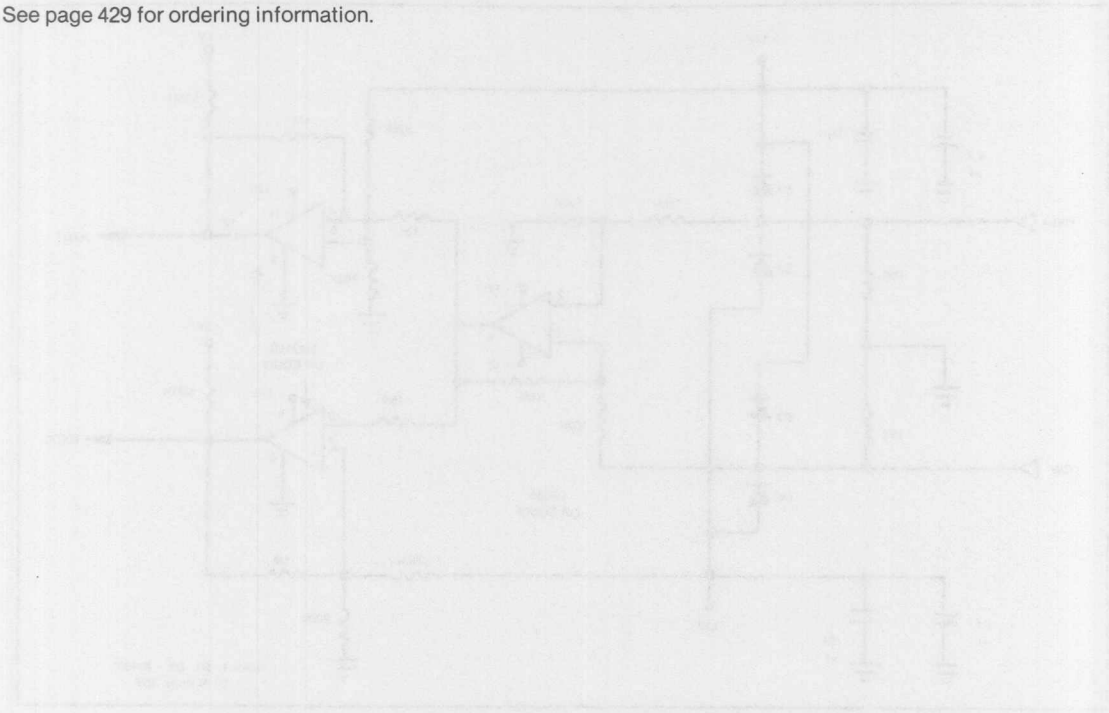
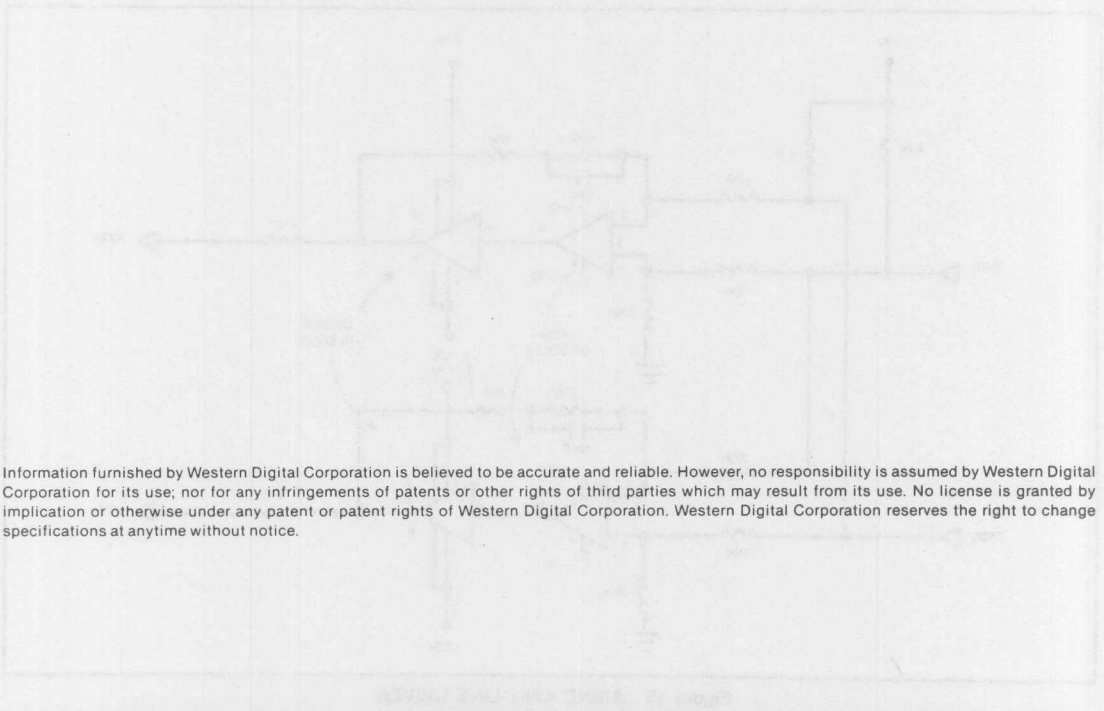


Figure 15 ARINC 429-1 LINE DRIVER

See page 429 for ordering information.





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FEATURES

- TWO INDEPENDENT ASYNCHRONOUS FULL DUPLEX DATA COMMUNICATION CHANNELS (2 BOARTS)
- TWO INDEPENDENT BAUD RATE GENERATORS (ONE PER CHANNEL)
- EACH CHANNEL WITH FOLLOWING FEATURES:
- SELECTABLE 5 TO 8 BIT CHARACTERS
- 1X, 16X, 64X CLOCK RATES
- 16 SELECTABLE BAUD RATE CLOCK FREQUENCIES (INTERNAL)
- LINE BREAK DETECTION AND GENERATION
- 1, 1½, OR 2 STOP BIT SELECTION
- FALSE START BIT DETECTION
- ODD OR EVEN PARITY GENERATE AND DETECTION
- OVERRUN AND FRAMING DETECTION
- DOUBLE BUFFERING OF DATA
- TTL COMPATIBLE INPUTS AND OUTPUTS
- COMPATIBLE WITH 8251A (ASYNC ONLY) AND WD1983 DEVICES
- DIAGNOSTIC LOCAL LOOP-BACK MODE
- RXD INITIALIZATION UPON MASTER RESET
- ON-BOARD OSCILLATOR FOR EASE OF USE WITH A CRYSTAL
- VERSATILE CLOCK SELECT OPTIONS FOR INDEPENDENT TRANSMIT AND RECEIVE RATES

INTRODUCTION

The Western Digital WD2123 Dual Enhanced Universal Communications Element (DEUCE) is a single chip MOS/LSI Data Communications Controller Circuit that contains two independent full-duplex asynchronous RECEIVER/TRANSMITTER CHANNELS and two independent BAUD RATE GENERATORS. The WD2123 is fabricated in N-Channel silicon gate technology and is packaged in a 40 pin plastic or ceramic package. All inputs and outputs are TTL compatible.

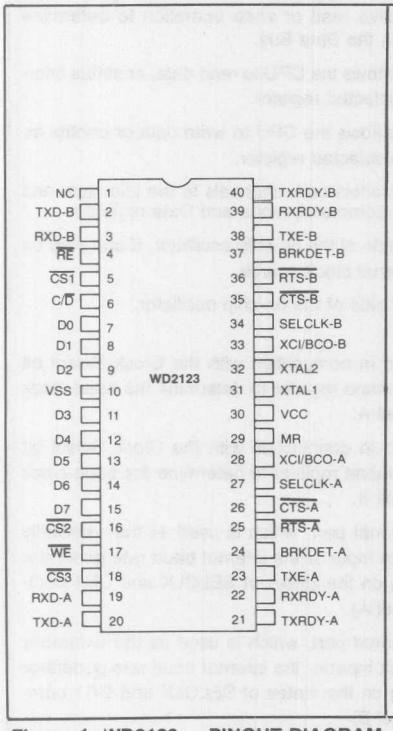


Figure 1. WD2123 PINOUT DIAGRAM

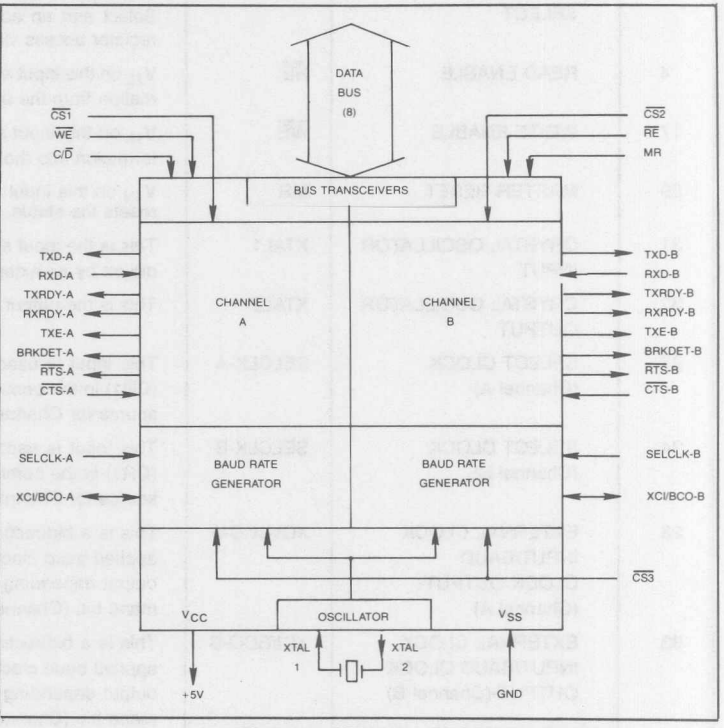


Figure 2. WD2123 BLOCK DIAGRAM

PIN NUMBER	PIN NAME	SYMBOL	FUNCTION
10	GROUND	VSS	Ground
30	POWER SUPPLY	VCC	+5VDC power supply input.
7	DATA BUS	D0	This is the 8 bit Bidirectional Data Bus. It is the means of communication between the WD2123 and the CPU. Data, control, mode and status registers are accessed via this bus.
8		D1	
9		D2	
11		D3	
12		D4	
13		D5	
14		D6	
15		D7	
5	CHIP SELECT ONE	$\overline{CS1}$	V_{IL} on this input selects Channel A and enables computer communications with Channel A Data, control and status registers.
16	CHIP SELECT TWO	$\overline{CS2}$	V_{IL} on this input selects Channel B and enables computer communications with Channel B Data, control and status registers.
18	CHIP SELECT THREE	$\overline{CS3}$	V_{IL} on this input select the Baud Rate registers for programming.
6	CONTROL or DATA SELECT	C/$\overline{D}$	This input is used in conjunction with the appropriate Chip Select and an active read or write operation to determine register access via the Data Bus.
4	READ ENABLE	$\overline{RE}$	V_{IL} on this input allows the CPU to read data, or status information from the selected register.
17	WRITE ENABLE	$\overline{WE}$	V_{IL} on this input allows the CPU to write data or control information into the selected register.
29	MASTER RESET	MR	V_{IH} on this input resets both channels to the idle state and resets the status, command, mode and Data registers.
31	CRYSTAL OSCILLATOR INPUT	XTAL1	This is the input side of the on-chip oscillator. It can also be driven by an external clock source.
32	CRYSTAL OSCILLATOR OUTPUT	XTAL2	This is the output side of the on-chip oscillator.
27	SELECT CLOCK (Channel A)	SELCLK-A	This input is used in conjunction with the Clock Select bit (CR1) in the command register to determine the baud clock source for Channel A.
34	SELECT CLOCK (Channel B)	SELCLK-B	This input is used in conjunction with the Clock Select bit (CR1) in the command register to determine the baud clock source for Channel B.
28	EXTERNAL CLOCK INPUT/BAUD CLOCK OUTPUT-(Channel A)	XCI/BCO-A	This is a bidirectional port, which is used as the externally applied baud clock input or the internal baud rate generator output depending on the states of SELCLK and CR1 command bit. (Channel A)
33	EXTERNAL CLOCK INPUT/BAUD CLOCK OUTPUT-(Channel B)	XCI/BCO-B	This is a bidirectional port, which is used as the externally applied baud clock input or the internal baud rate generator output depending on the states of SELCLK and CR1 command bit. (Channel B)
26	CLEAR-TO-SEND (Channel A)	$\overline{CTS-A}$	V_{IL} on this input enables Channel A to transmit serial data if the Transmitter is enabled.

PIN NUMBER	PIN NAME	SYMBOL	FUNCTION
35	CLEAR-TO-SEND (Channel B)	$\overline{\text{CTS-B}}$	V_{IL} on this input enables Channel B to transmit serial data if the Transmitter is enabled.
20	TRANSMIT DATA (Channel A)	TXD-A	This is the Serial Data Output from Channel A.
2	TRANSMIT DATA (Channel B)	TXD-B	This is the Serial Data Output from Channel B.
19	RECEIVE DATA (Channel A)	RXD-A	This is the Serial Data Input for Channel A.
3	RECEIVE DATA (Channel B)	RXD-B	This is the Serial Data Input for Channel B.
21	TRANSMITTER READY (Channel A)	TXRDY-A	This output, when high (V_{OH}), alerts the CPU that Channel A is ready to accept a new data character. The TXRDY output is automatically reset whenever a character is written into the Transmit Holding Register and can be used as an interrupt to the system.
40	TRANSMITTER READY (Channel B)	TXRDY-B	This output, when high (V_{OH}), alerts the CPU that Channel B is ready to accept a new data character. The TXRDY output is automatically reset whenever a character is written into the Transmit Holding Register and can be used as an interrupt to the system.
22	RECEIVER READY (Channel A)	RXRDY-A	This output, when high (V_{OH}), alerts the CPU that Channel B contains a data character that is ready to be input. This output is automatically reset whenever the new character is read from the Receive Holding Register and can be used as an interrupt to the system.
39	RECEIVER READY (Channel B)	RXRDY-B	This output, when high (V_{OH}), alerts the CPU that Channel B contains a data character that is ready to be input. This output is automatically reset whenever the new character is read from the Receive Holding Register and can be used as an interrupt to the system.
23	TRANSMITTER EMPTY (Channel A)	TXE-A	This output, when high (V_{OH}), indicates that Channel A Transmitter has no new characters to send and is waiting in an idle state.
38	TRANSMITTER EMPTY (Channel B)	TXE-B	This output, when high (V_{OH}), indicates that Channel B Transmitter has no new characters to send and is waiting in an idle state.
24	BREAK DETECT (Channel A)	BRKDET-A	This output, when high (V_{OH}), indicates that the Receiver for Channel A has detected a break condition.
37	BREAK DETECT (Channel B)	BRKDET-B	This output, when high (V_{OH}), indicates that the Receiver for Channel B has detected a break condition.
25	REQUEST-TO-SEND (Channel A)	$\overline{\text{RTS-A}}$	A general purpose output that is controlled by the command register bit CR5 for Channel A.
36	REQUEST-TO-SEND (Channel B)	$\overline{\text{RTS-B}}$	A general purpose output that is controlled by the command register bit CR5 for Channel B.
1		NC	No Internal Connection.

Table 1 WD2123 PIN DESCRIPTIONS

GENERAL DESCRIPTION

The WD2123 Block Diagram is shown in Figure 2. The WD2123 is a merger of two WD1983s and one WD1941 from WDC's line of communications devices on one piece of silicon. The 1983 is an asynchronous only version of the 8251A and the 1941 is a baud rate generator. In this manner, 8251A compatibility is maintained with the WD2123 with the added features of 2 channels and 2 baud rate generators on a single chip.

As depicted from the block diagram, the channels are referred to as CHANNELS A and B. CHANNEL A, which is an asynchronous 8251A, is addressed or controlled by the input signal $\overline{CS1}$. CHANNEL B is similarly controlled by $\overline{CS2}$. Finally, the BAUD RATE GENERATORS are controlled by $\overline{CS3}$.

Each channel of the WD2123 can be programmed to receive and transmit asynchronous serial data. The WD2123 performs serial-to-parallel conversion on data characters received from an input/output device or a MODEM, and parallel-to-serial conversion on data characters received from the CPU. The CPU can read the status of either channel at any time. Status information on a per channel basis reported includes the type and the condition of the transfer operations being performed by the WD2123 as well as any transmission error conditions (parity, overrun, or framing). Programming the WD2123 is identical to the 8251A in the asynchronous mode, remembering that $\overline{CS1}$, when low, selects CHANNEL A and when $\overline{CS2}$ is low, selects CHANNEL B.

The WD2123 BAUD RATE GENERATORS may be selected either internally or externally. The clock select logic includes a clock select control bit CR1 (CS) in each COMMAND INSTRUCTION REGISTER. This control bit allows selection of the internal baud clock or an externally applied clock and works in conjunction with the select clock pin, "SELCLK" and the external clock input/baud clock output pin, "XCI/BCO". When CS is logic 1, the external clock select mode is selected. This means that the transmit and receive clocks (TXC and RXC) are internally tied together and the select clock pin, SELCLK, will determine whether those clocks are driven from the internal baud rate generator (SELCLK is high) or from the external clock input pin, "XCI/BCO", (SELCLK is low).

If the internal BRG clock is selected, (SELCLK is high) then the external clock input pin becomes a BRG clock output. Hence, the mnemonic, "XCI/BCO".

When CR1 (CS) is logic 0, then internal clock select mode is selected. The transmit clock (TXC) is driven by the internal BRG clock and the receive clock is driven by the select clock pin, (SELCLK). The XCI/BCO pin becomes the baud clock output (the same signal that is being applied to TXC).

The WD2123 also provides a local loop-back test mode of operation for each channel. This diagnostic mode is independently controlled via the LB(CR7) bit of the COMMAND REGISTER. When LB is logic 1, the channel is programmed for Local Loop-Back. In this diagnostic mode, the TXD output is set to the marking (logic "1") state; the output of the TRANSMIT REGISTER is "looped-back" into the RECEIVER REGISTER input; $\overline{RTS}$ output is held high; the $\overline{CTS}$ and RXD inputs are ignored. An additional requirement is that the TEN(CR0) command bit and the REN(CR2) be logic 1. The status and output flags operate normally.

Each channel is also provided with break character generation and detection. (A break character is defined as all zero data bits, parity bit and stop bits after a valid start bit.) For break character generation, SBRK (CR3) command bit is set to a logic 1. This causes the TXD output to be forced low (spacing) for as long as SBRK is programmed high. The break detect output and status bit (SR6) is set to logic 1, indicating that the receiver has detected a break character. The framing error flag is also set to 1 for this condition.

ORGANIZATION

The WD2123 is an eight bit bus-oriented device. Communication between the controlling CPU and the two RECEIVER/TRANSMITTER CHANNELS or the two BAUD RATE GENERATORS occurs via the 8 bit data bus through a common set of bus transceivers.

A diagram of one of the two communication controllers is shown in Figure 3. There are two accessible data registers, which buffers transmit and receive data. They are the TRANSMIT HOLDING REGISTER and the RECEIVE HOLDING REGISTER. There is a parallel-to-serial shift register, the TRANSMIT REGISTER and a serial-to-parallel shift register, the RECEIVE REGISTER.

Operational Control and monitoring of the CHANNEL is performed by two CONTROL REGISTERS (the COMMAND INSTRUCTION REGISTER and the MODE INSTRUCTION REGISTER) and the STATUS REGISTER.

A read/write control circuit allows programming/monitoring or loading/reading of data in the CONTROL, STATUS and HOLDING REGISTERS by activating the appropriate control lines: Chip Select ($\overline{CS1}$, $\overline{CS2}$, $\overline{CS3}$), READ ENABLE ($\overline{RE}$), WRITE ENABLE ($\overline{WE}$) and CONTROL or DATA SELECT (C/$\overline{D}$).

Internal control of each channel is by means of two internal microcontrollers: one for transmit and one for receive. The control registers, various counters and external signals provide inputs to the microcontrollers, which generate the necessary control signals to send and receive serial data according to the programmed protocol.

A diagram of one of the two BAUD RATE GENERATORS is shown in Figure 4. The 4 low order DATA BUS bits, DO-D3, are used to program the desired rate by loading the RATE REGISTER. Control signals $\overline{CS3}$, $\overline{WE}$ and C/$\overline{D}$ are used to select and load the appropriate register.

The contents of the RATE REGISTER is decoded and addresses a FREQUENCY SELECT ROM for the proper frequency, which is generated by the DIVIDER circuitry and the control logic.

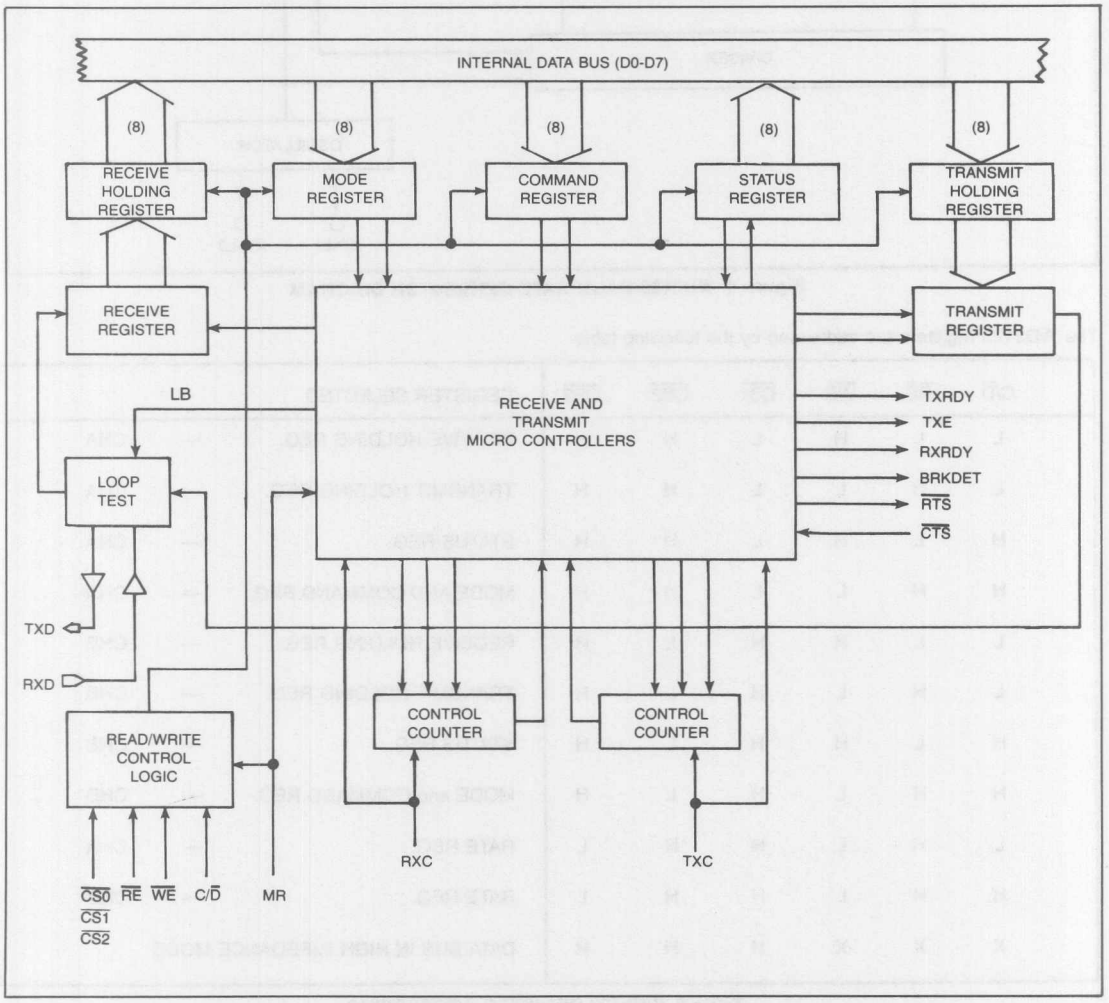


Figure 3. RECEIVE/TRANSMIT COMMUNICATIONS CONTROLLER DIAGRAM

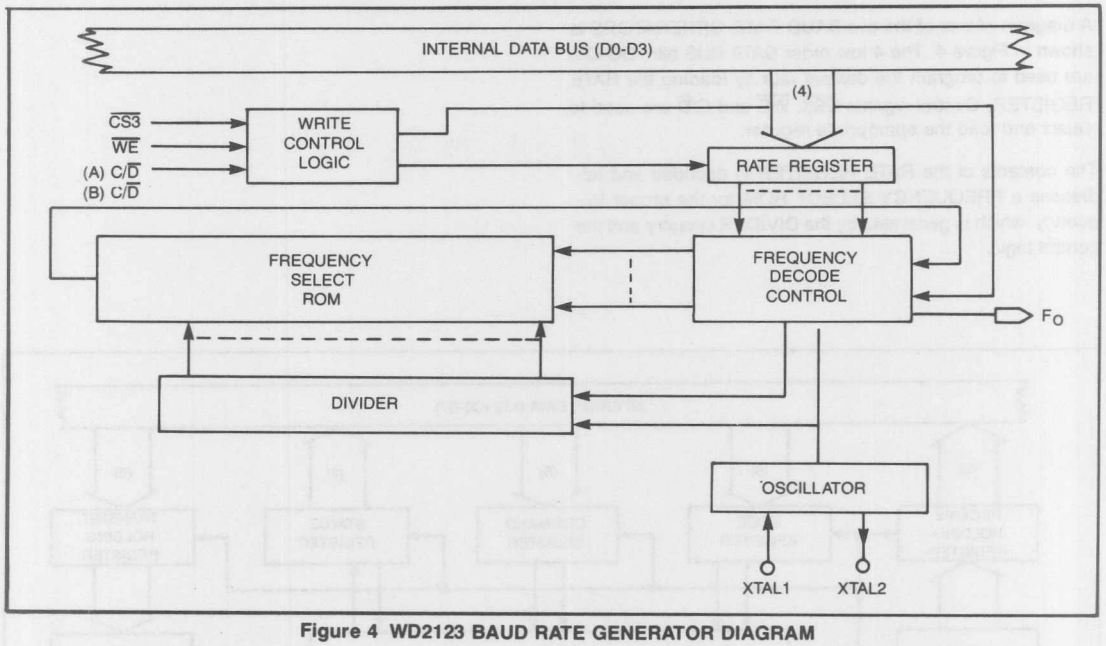


Figure 4 WD2123 BAUD RATE GENERATOR DIAGRAM

The WD2123 registers are addressed by the following table:

C/$\overline{D}$	$\overline{RE}$	$\overline{WE}$	$\overline{CS1}$	$\overline{CS2}$	$\overline{CS3}$	REGISTER SELECTED		
L	L	H	L	H	H	RECEIVE HOLDING REG.	—	CHA
L	H	L	L	H	H	TRANSMIT HOLDING REG.	—	CHA
H	L	H	L	H	H	STATUS REG.	—	CHA
H	H	L	L	H	H	MODE AND COMMAND REG.	—	CHA
L	L	H	H	L	H	RECEIVE HOLDING REG.	—	CHB
L	H	L	H	L	H	TRANSMIT HOLDING REG.	—	CHB
H	L	H	H	L	H	STATUS REG.	—	CHB
H	H	L	H	L	H	MODE and COMMAND REG.	—	CHB
L	H	L	H	H	L	RATE REG.	—	CHA
H	H	L	H	H	L	RATE REG.	—	CHB
X	X	X	H	H	H	DATA BUS IN HIGH IMPEDANCE MODE		

Table 2 WD2123 REGISTER ADDRESSING

Note:
"L" means V_{IL} at pins.
"H" means V_{IH} at pins.
"X" means don't care.

The WD2123 contains two MODE REGISTERS—one for each channel. The format and definition of the MODE REGISTERS are shown below:

MR7	MR6	MR5	MR4	MR3	MR2	MR1	MR0
S2	S1	EP	PEN	L2	L1	B2	B1

B2	B1	BAUD RATE FACTOR
0	0	Undefined
0	1	1X
1	0	16X
1	1	64X
L2	**L1**	**CHARACTER LENGTH**
0	0	5 Bits
0	1	6 Bits
1	0	7 Bits
1	1	8 Bits
PEN		**PARITY ENABLE**
0		Disable Parity
1		Enable Parity
EP		**PARITY SELECT**
0		Odd Parity
1		Even Parity
S2	**S1**	**NUMBER OF STOP BITS**
0	0	Invalid
0	1	1 Bit
1	0	1½ Bits
1	1	2 Bits

Table 3 WD2123 MODE REGISTERS

The WD2123 contains two COMMAND REGISTERS—one per channel. The format and definition of the COMMAND REGISTERS are shown below:

CR7	CR6	CR5	CR4	CR3	CR2	CR1	CR0
LB	IR	RTS	ER	SBK	REN	CS	TEN

TEN	TRANSMIT ENABLE
1	Enable
0	Disable
CS	**CLOCK SELECT**
1	External Clock Select Mode
0	Internal Clock Select Mode
REN	**RECEIVE ENABLE**
1	Enable
0	Disable
SBK	**SEND BREAK CHARACTER**
1	Force TXD Low
0	Normal Operation
ER	**ERROR RESET**
1	Reset Error Flags
0	No Reset
RTS	**REQUEST TO SEND**
1	Force $\overline{RTS}$ pin = 0 (V_{OL})
0	Force $\overline{RTS}$ pin = 1 (V_{OH})
IR	**INTERNAL RESET**
1	Next Write to Mode Register
0	Next Write to Command Register
LB	**LOOP BACK ENABLE**
0	Normal Operation Mode
1	Local Loop-Back Mode

Table 4 WD2123 CONTROL REGISTERS

The WD2123 contains two STATUS REGISTERS—one per channel. The STATUS REGISTER is a read-only register. The format and definition of the STATUS REGISTERS are shown below:

SR7	SR6	SR5	SR4	SR3	SR2	SR1	SR0
CTS	BRK DET	FE	OE	PE	TXE	RX RDY	TX RDY

TXRDY	**TRANSMITTER READY**
1	Denotes THR is empty and ready for a new character
0	THR not empty. (Reset when THR is loaded by CPU)
RXRDY	**RECEIVER READY**
1	Denotes that the RHR contains a valid character
0	RHR does not contain a valid character. (Reset when the CPU reads the RHR)
TXE	**TRANSMITTER EMPTY**
1	Denotes that the TR is empty
0	Denotes that the TR is not empty
PE	**PARITY ERROR**
1	Denotes Parity Error
0	No Parity Error. (Reset by ER bit of command register)
OE	**OVERRUN ERROR**
1	Denotes Overrun Error
0	No Overrun Error. (Reset by ER bit of command register)
FE	**FRAMING ERROR**
1	Denotes Framing Error
0	No Framing Error. (Reset by ER bit of command register)
BRKDET	**BREAK DETECT**
1	Indicates that the receiver has detected a line break condition. (FE will also be set)
0	No Break Condition detected for at least one bit time
CTS	**CLEAR-TO-SEND**
1	Indicates that the $\overline{CTS}$ pin is active (V_{IL})
0	Indicates that the $\overline{CTS}$ pin is not active (V_{IH})

Table 5 WD2123 STATUS REGISTERS

The WD2123 contains two RATE REGISTERS that are used to select 16 BAUD rates when CR1 = 1 and SELCLK = 1. The Format of the RATE REGISTERS is shown below. Note that the Receiver and the Transmitter of any channel run off the same Baud clock except when CR1 = 0, then the Transmitter runs off the Baud Clock and the Receiver runs off an externally applied signal input on the SELCLK pin.

D7							D0
X	X	X	X	RA3 RB3	RA2 RB2	RA1 RB1	RA0 RB0

When C/$\overline{D}$ = 0, RA3 to RA0 are loaded.
When C/$\overline{D}$ = 1, RB3 to RB0 are loaded.

The C/$\overline{D}$ line is used in conjunction with $\overline{CS3}$ and $\overline{WE}$ to program the desired BAUD rate. When C/$\overline{D}$ is low, Channel A is selected, and when C/$\overline{D}$ is high, Channel B is selected. The low order 4 bits of the DATA BUS are loaded into the selected rate register, and the high order 4 bits are ignored.

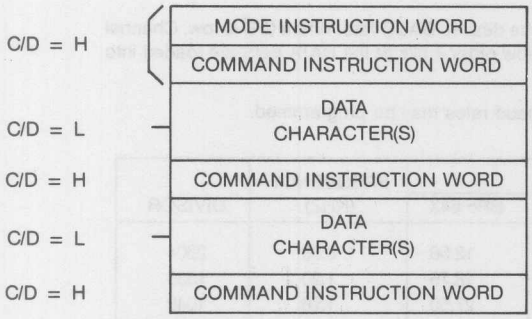
When the crystal frequency equals 1.8432 MH_z the following baud rates may be programmed.

				BAUD RATE			FREQUENCY	
R3	R2	R1	R0	BRF 1X	BRF 16X	BRF 64X	(KHZ)	DIVISOR
0	0	0	0	800	50.0	12.50	0.80	2304
0	0	0	1	1,200	75.0	18.75	1.20	1536
0	0	1	0	1,760	110.0	27.50	1.76	1049
0	0	1	1	2,150	134.5	33.59	2.15	855
0	1	0	0	2,400	150.0	37.50	2.40	768
0	1	0	1	3,200	200.0	50.00	3.20	576
0	1	1	0	4,800	300.0	75.00	4.80	384
0	1	1	1	9,600	600.0	150.00	9.60	192
1	0	0	0	19,200	1,200.0	300.00	19.20	96
1	0	0	1	28,800	1,800.0	450.00	28.80	64
1	0	1	0	38,400	2,400.0	600.00	38.40	48
1	0	1	1	57,600	3,600.0	900.00	57.60	32
1	1	0	0	76,800	4,800.0	1,200.00	76.80	24
1	1	0	1	115,200	7,200.0	1,800.00	115.20	16
1	1	1	0	153,600	9,600.0	2,400.00	153.60	12
1	1	1	1	307,200	19,200.0	4,800.00	307.20	6

Table 6. WD2123 BAUD RATE SELECTION

READ/WRITE OPERATIONS

The WD2123 must be initialized after a MASTER RESET pulse by first writing the MODE INSTRUCTION word and then the COMMAND INSTRUCTION word. Thereafter, every control write to the device is interpreted as a COMMAND word. If it is desired to re-program the MODE REGISTER, a COMMAND REGISTER bit, INTERNAL RESET (CR6), allows the next control write data to be entered into the MODE REGISTER.



TYPICAL DATA BLOCK TRANSFER

OPERATING DESCRIPTION

The WD2123 is primarily designed to operate in an 8 bit microprocessor environment, although other control logic schemes are easily implemented. The DATA BUS and the interface control signals ($\overline{CS1}$, $\overline{CS2}$, $\overline{CS3}$, C/$\overline{D}$, $\overline{RE}$, $\overline{WE}$) should be connected to the microprocessor's data bus and system control bus. A 1.8432 MHz crystal should be connected to the WD2123 as shown in figure 5. The appropriate TXC (RXC) clock frequencies should be programmed via system software. Different Baud clock configurations are possible, such as separate transmit and receive frequencies, and are outlined in the general description.

For typical data communication applications, the RXD and TXD input/outputs can be connected to RS-232C interface circuits. Interface control signals, $\overline{CTS}$ and $\overline{RTS}$, are controlled and sensed by the CPU through the COMMAND and STATUS REGISTERS and can be configured in several ways. The $\overline{CTS}$ input can be used to synchronize the transmitter to external events.

The TXRDY, RXRDY, TXE and BRKDET FLAGS may be connected to the microprocessor system as interrupt inputs or the STATUS REGISTER can be periodically read in a polled environment to support data communication control operations.

The SBRK bit of the COMMAND REGISTER (CR3) is used to send a Break Character. (A Break Character is defined as a start bit, and all zero data, parity and stop bits.) When the CR3 bit is set to a "1", it causes the transmitter output, TXD, to be forced low after the last bit of the last character is transmitted.

The Receiver is equipped with logic to look for a break character. When a break is received, the BREAK DETECT (BRKDET) FLAG and STATUS bit are set to "1". When the receiver input line goes high (V_{IH}) for at least one clock period, the receiver resets the BRKDET FLAG and resumes its search for a start bit.

PROGRAMMING PROCEDURE

The programming sequence of the two channels will be different, depending on whether it is an initialization sequence (that is, one performed right after a hardware master reset occurs) or a re-programming sequence (that is, one performed to change the protocol characteristics (Parity, rate, character length, etc.) after the device has been previously operating in the system). The programming sequence differs, in that, after a master reset, the chip is set to expect the first *control write* operation (C/$\overline{D}$ = 1) to contain a *mode instruction.* Any *subsequent control write* operations will be transferred to the *command instruction* register.

Now when it is desired to *change* the *mode instruction* register contents, the following re-programming sequence should be performed. A Command Control word of "40" Hex is written to the Chip. This turns off the Receiver and Transmitter and sets the IR (Internal Reset) bit. This bit causes the read/write control logic to expect the *next control write* operation to be a *new mode instruction.* After the new mode instruction is written to the chip, all subsequent control write operations will again be interpreted as *command instructions.* Therefore, after the *new mode instruction* is performed, the next command would turn the receiver and transmitter back on and resume normal Data operations.

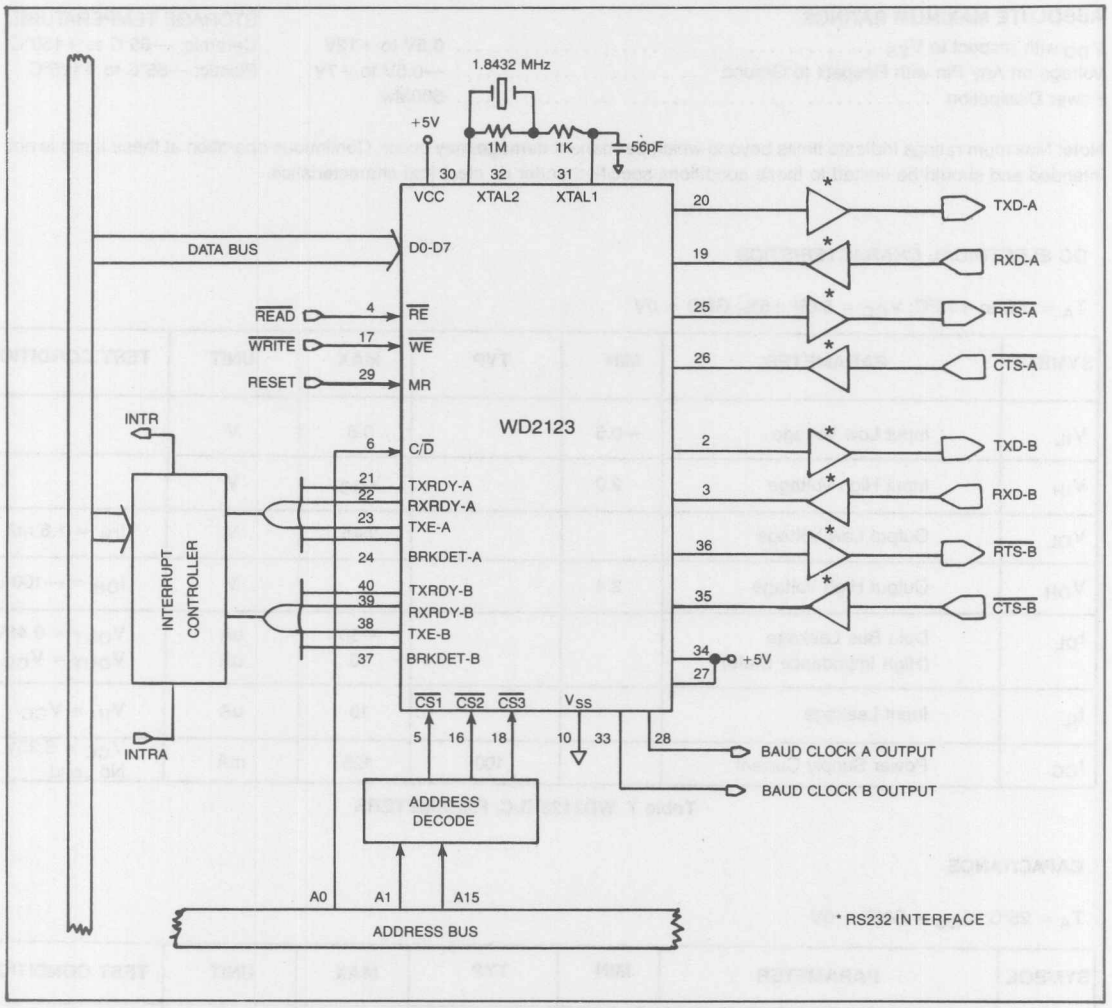


Figure 5 WD2123 MICROPROCESSOR APPLICATION

ABSOLUTE MAXIMUM RATINGS

V_{DD} with respect to V_{SS} ..... 0.5V to +12V
Voltage on Any Pin with Respect to Ground ..... —0.5V to +7V
Power Dissipation ..... 500Mw.

STORAGE TEMPERATURE:
Ceramic: —65°C to +150°C
Plastic: —55°C to +125°C

Note: Maximum ratings indicate limits beyond which permanent damage may occur. Continuous operation at these limits is not intended and should be limited to those conditions specified under dc electrical characteristics.

DC ELECTRICAL CHARACTERISTICS

T_A = 0°C to +70°C; V_{CC} = 5.0V ±5%; GND = 0V

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT	TEST CONDITIONS
V_{IL}	Input Low Voltage	—0.5		0.8	V	
V_{IH}	Input High Voltage	2.0		V_{CC}	V	
V_{OL}	Output Low Voltage			0.45	V	I_{OL} = 1.6 mA
V_{OH}	Output High Voltage	2.4			V	I_{OH} = —100 uA
I_{DL}	Data Bus Leakage (High Impedance State)			—50 10	uA uA	V_{OUT} = 0.45V V_{OUT} = V_{CC}
I_{IL}	Input Leakage			10	uA	V_{IN} = V_{CC}
I_{CC}	Power Supply Current		100	125	mA	V_{CC} = 5.25V No Load

Table 7 WD2123 D.C. PARAMETERS

CAPACITANCE

T_A = 25°C; V_{CC} = GND = 0V

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT	TEST CONDITIONS
C_{IN}	Input Capacitance			10	pF	f_C = 1MHz
$C_{I/O}$	I/O Capacitance			20	pF	Unmeasured pins returned to GND.

Table 8 WD2123 CAPACITANCE LEVELS

AC ELECTRICAL CHARACTERISTICS

Table 9 WD2123 A.C. PARAMETERS

T_A = 0°C to + 70C; V_{CC} = 5.0V ±5%; GND = 0V

SYMBOL	PARAMETER	MIN	MAX	UNITS	CONDITIONS
BUS PARAMETERS Read Cycle					
t_{AR}	Address Stable Before READ (CS,C/D)	50		ns	
t_{RA}	Address Hold Time for READ (CS,C/D)	50		ns	
t_{RE}	READ Pulse Width	230		ns	
t_{RD}	Data Delay from READ		200	ns	C_L = 50 pF
t_{RDH}	READ to Data Floating	25	200	ns	C_L (Max) = 50 pF C_L (Min) = 15 pF
Write Cycle					
t_{AW}	Address Stable Before WRITE	50		ns	
t_{WA}	Address Hold Time for WRITE	50		ns	
t_{WE}	WRITE Pulse Width	230		ns	
t_{DS}	Data Set-Up Time for WRITE	TWE		ns	
t_{WDH}	Data Hold Time for WRITE	100		ns	
OTHER TIMINGS					
t_{TXC}	Transmit Clock Period	1.6		us	
t_{DTX}	TxD Delay from Falling Edge of TxC		1000	ns	C_L = 100 pF
t_{SRX}	Rx Data Set-Up Time to Sampling Pulse	200		ns	C_L = 100 pF
t_{HRX}	Rx Data Hold Time to Sampling Pulse	200		ns	C_L = 100 pF
f_{TX}	Transmitter Input Clock Frequency 1x Baud Rate 16x and 64x Baud Rate	 DC DC	 500 600	 kHz kHz	 Clock 50% Duty Cycle
t_{TPW}	Transmitter Input Clock Pulse Width 1x Baud Rate 16x and 64x Baud Rate	 1.0 800		 us ns	
t_{TPD}	Transmitter Input Clock Pulse Delay 1x Baud Rate 16x and 64x Baud Rate	 1.0 800		 us ns	
t_{MR}	Master Reset	500		ns	

Table 9 WD2123 A.C. PARAMETERS

SYMBOL	PARAMETER	MIN	MAX	UNIT	TEST CONDITION
f_{RX}	Receiver Input Clock Frequency 1x Baud Rate 16x and 64x Baud Rate	 DC DC	 500 600	 kHz kHz	Clock 50% Duty Cycle
t_{RPW}	Receiver Input Clock Pulse Width 1x Baud Rate 16x and 64x Baud Rate	 1.0 800		 us ns	
t_{RPD}	Receiver Input Clock Pulse Delay 1x Baud Rate 16x and 64x Baud Rate	 1.0 800		 us ns	
t_{TX}	TxRDY Delay from Center of Stop Bit		8	t_{RXC}	C_L = 50pF (16X)
t_{RX}	RxRDY Delay from Center of Stop Bit		½	t_{RXC}	
t_{IS}	Internal BRKDET Delay from Center of Data Bit		1	RXC	
t_{TRD}	TxRDY Delay from Falling Edge of WRITE		450	ns	
t_{TOD}	TXD Output from Falling Edge of WRITE		1½	t_{TXC}	
t_{WC}	Control Delay from Rising Edge of WRITE (RTS)		200	ns	
t_{CR}	Control to READ Set-Up Time (CTS)		1	t_{TXC}	
t_{MR}	Master Reset	500		ns	

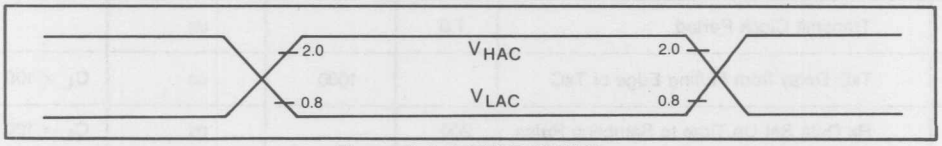


Figure 6 A.C. TEST POINTS

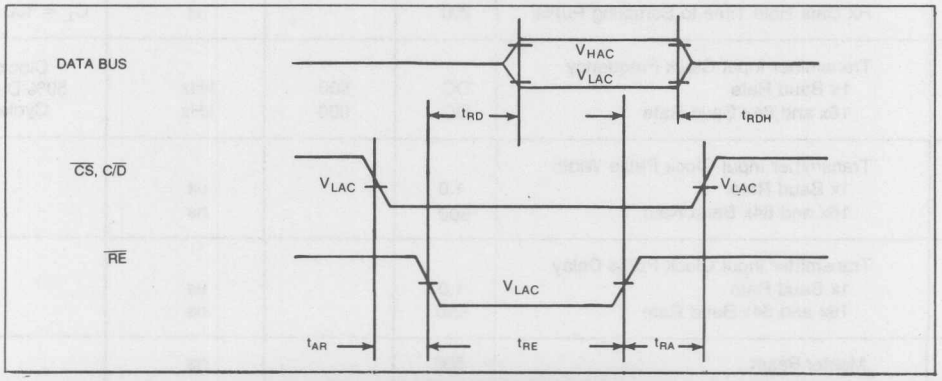


Figure 7 WD2123 READ TIMING

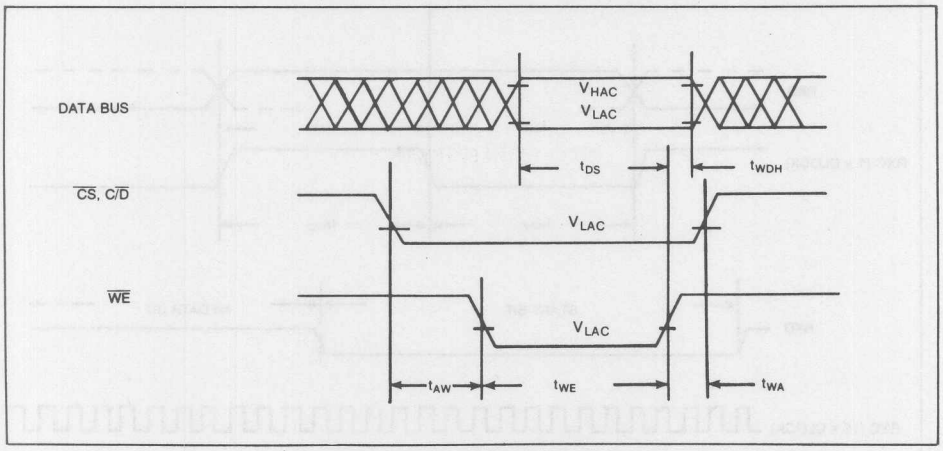


Figure 8 WD2123 WRITE TIMING

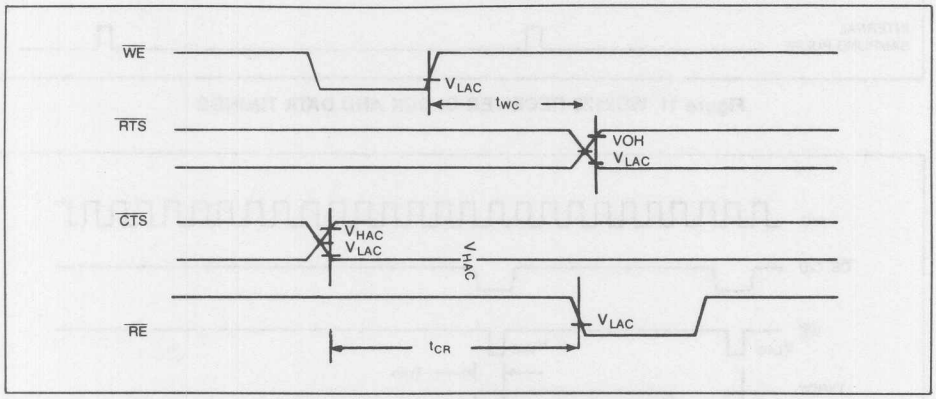


Figure 9 WD2123 INTERFACE CONTROL TIMING

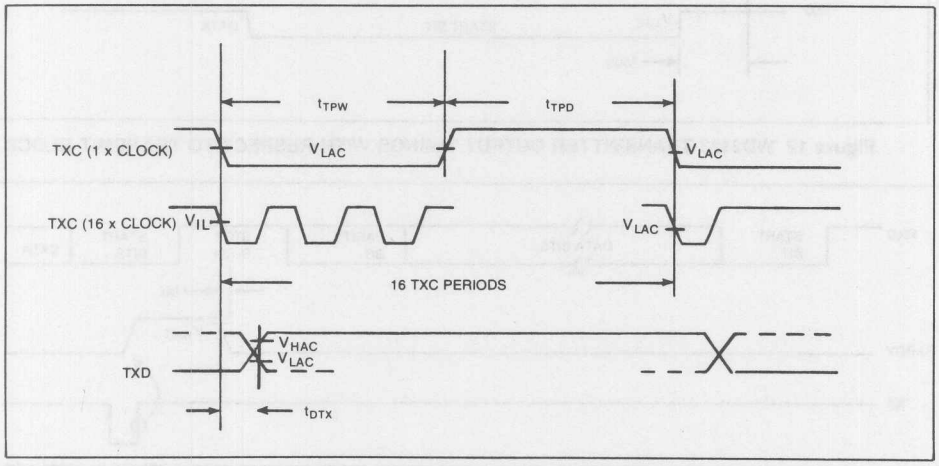


Figure 10 WD2123 TRANSMITTER CLOCK AND DATA TIMING

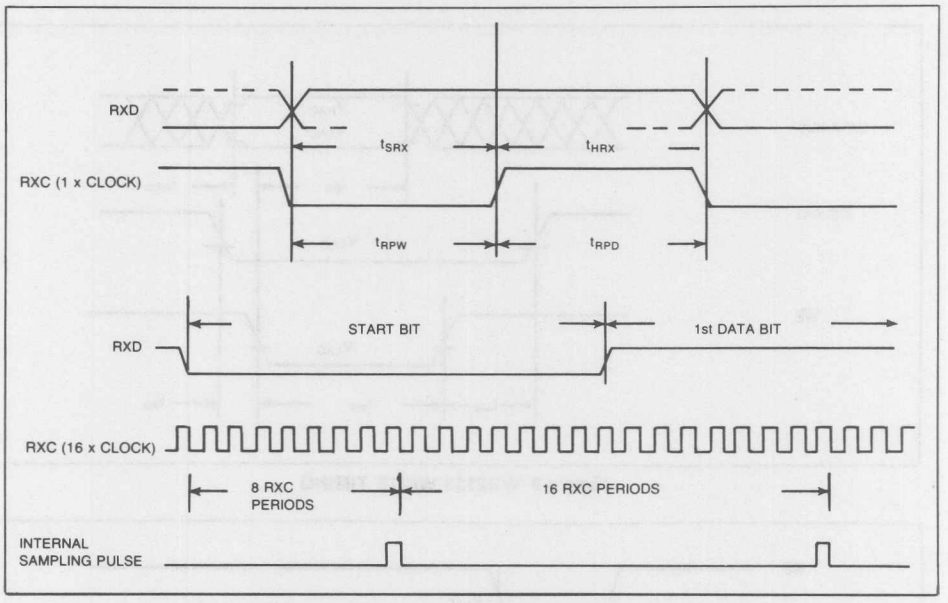


Figure 11 WD2123 RECEIVER CLOCK AND DATA TIMINGS

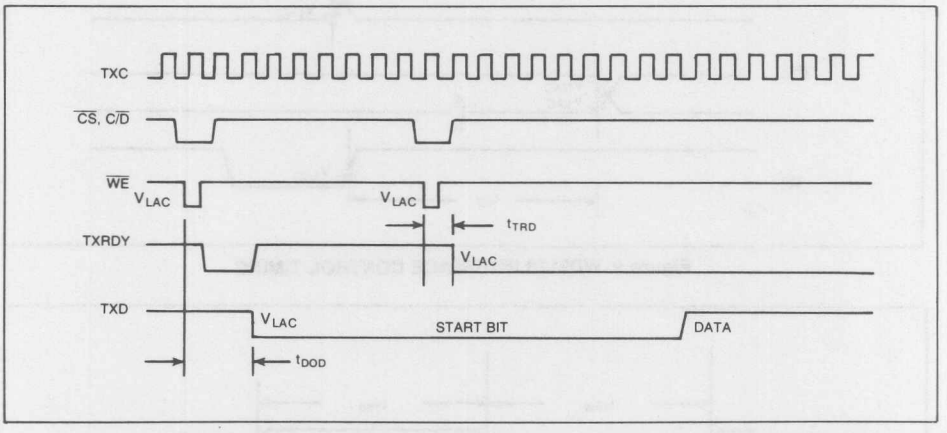


Figure 12 WD2123 TRANSMITTER OUTPUT TIMINGS WITH RESPECT TO TRANSMIT CLOCK

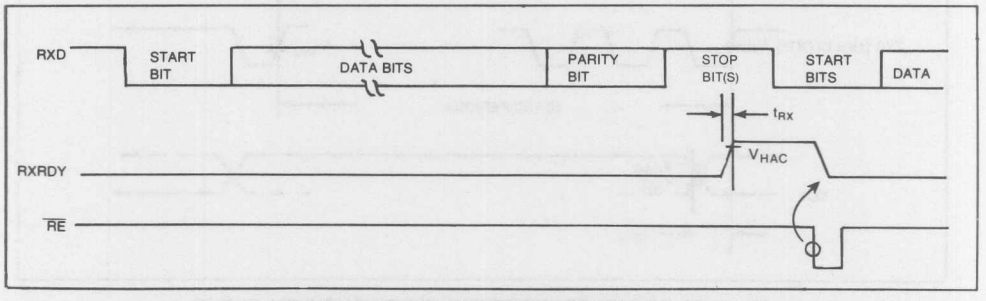


Figure 13 WD2123 RXRDY TIMING

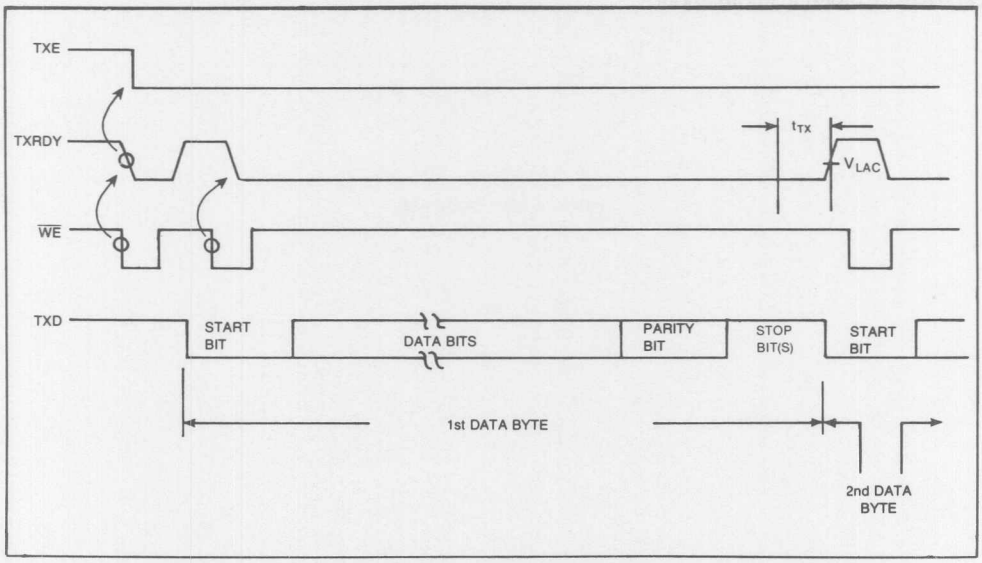
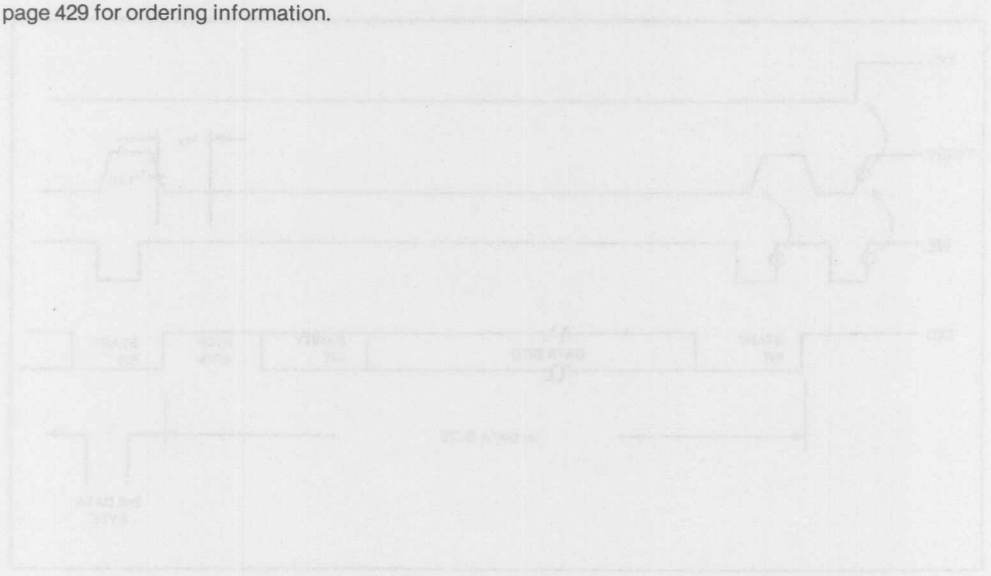


Figure 14 WD2123 TXRDY TIMING

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See page 429 for ordering information.



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WD8250 Asynchronous Communications Element

FEATURES

- Designed to be Easily Interfaced to Most Popular Microprocessors (Z-80, 8080A, 6800, etc.)
- Full Double Buffering
- Independently Controlled Transmit, Receive, Line Status, and Data Set Interrupts
- Programmable Baud Rate Generator Allows Division of Any Input Clock by 1 to (2^{16} - 1) and Generates the Internal 16x Clock
- Independent Receiver Clock Input
- Fully Programmable Serial-Interface Characteristics
  - —5-, 6-, 7-, or 8-Bit Characters
  - —Even, Odd, or No-Parity Bit Generation and Detection
  - —1-, 1½-, or 2-Stop Bit Generation
  - —Baud Rate Generation (DC to 56K Baud)
- False Start Bit Detector
- Complete Status Reporting Capabilities
- THREE-STATE TTL Drive Capabilities for Bi-directional Data Bus and Control Bus
- Line Break Generation and Detection
- Internal Diagnostic Capabilities
  - —Loopback Controls for Communications Link Fault Isolation
  - —Break, Parity, Overrun, Framing Error Simulation
- Full Prioritized Interrupt System Controls
- Single +5-Volt Power Supply

GENERAL DESCRIPTION

The WD8250 is a programmable Asynchronous Communication Element (ACE) in a 40-pin package. The device is fabricated in N/MOS silicon gate technology.

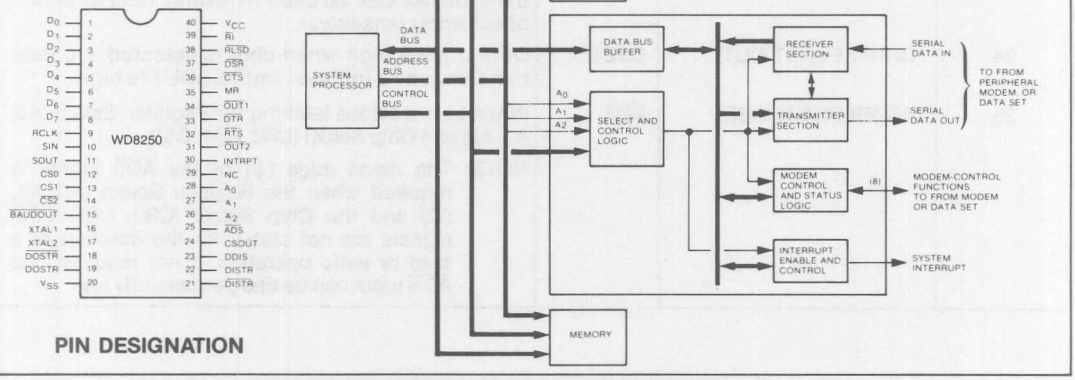
The ACE is a software-oriented device using a three-state 8-bit bi-directional data bus.

The ACE is used to convert parallel data to a serial format on the transmit side, and convert serial data to parallel on the receiver side. The serial format, in order of transmission and reception, is a start bit, followed by five to eight data bits, a parity bit (if programmed) and one, one and one half (five bit format only) or two stop bits. The maximum recommended data rate is 56K baud.

Internal registers enable the user to program various types of interrupts, modem controls, and character formats. The user can read the status of the ACE at any time monitoring word conditions, interrupts and modem status.

An additional feature of the ACE is a programmable baud rate generator that is capable of dividing an internal XTAL or TTL signal clock by a division of 1 to 2^{16} – 1.

The ACE is designed to work in either a polling or interrupt driven system, which is programmable by users software controlling an internal register.



PIN DESIGNATION

WD8250 GENERAL SYSTEM CONFIGURATION

PIN DEFINITIONS

PIN NUMBER	PIN NAME	SYMBOL	FUNCTION
1-8	DATA BUS	D0-D7	3-state input/output lines. Bi-directional communication lines between WD8250 and Data Bus. All assembled data TX and RX, control words, and status information are transferred via the D0-D7 data bus.
9	RECEIVE CLK.	RCLK	This input is the 16X baud rate clock for the receiver section of the chip (may be tied to BAUDOUT pin 15).
10	SERIAL INPUT	SIN	Received Serial Data In from the communications link (Peripheral device, modem or data set).
11	SERIAL OUTPUT	SOUT	Transmitted Serial Data Out to the communication link. The SOUT signal is set to a (logic 1) marking condition upon a MASTER RESET.
12 13 14	CHIP SELECT CHIP SELECT CHIP SELECT	CS0 CS1 $\overline{CS2}$	When CS0 and CS1 are high, and $\overline{CS2}$ is low, chip is selected. Selection is complete when the address strobe $\overline{ADS}$ latches the chip select signals.
15	BAUDOUT	$\overline{BAUDOUT}$	16X clock signal for the transmitter section of the WD8250. The clock rate is equal to the oscillator frequency divided by the divisor loaded into the divisor latches. The BAUDOUT signal may be used to clock the receiver by tying to (pin 9) RCLK.
16 17	EXTERNAL CLOCK IN EXTERNAL CLOCK OUT	XTAL 1 XTAL 2	These pins connect the crystal or signal clock to the WD8250 baud rate divisor circuit. See Fig. 3 and Fig. 4 for circuit connection diagrams.
18 19	DATA OUT STROBE DATA OUT STROBE	$\overline{DOSTR}$ DOSTR	When the chip has been selected, a low $\overline{DOSTR}$ or high DOSTR will latch data into the selected WD8250 register (a CPU write). Only one of these lines need be used. Tie unused line to its inactive state. $\overline{DOSTR}$ — high or DOSTR — low.
20	GROUND	V_{SS}	System signal ground.
21 22	DATA IN STROBE DATA IN STROBE	$\overline{DISTR}$ DISTR	When chip has been selected, a low $\overline{DISTR}$ or high DISTR will allow a read of the selected WD8250 register (a CPU read). Only one of these lines need be used. Tie unused line to its inactive state. $\overline{DISTR}$ — high or DISTR — low.
23	DRIVER DISABLE	DDIS	Output goes low whenever data is being read from the WD8250. Can be used to reverse data direction of external transceiver.
24	CHIP SELECT OUT	CSOUT	Output goes high when chip is selected. No data transfer can be initiated until CSOUT is high.
25	ADDRESS STROBE	$\overline{ADS}$	When low, provides latching for Register Select (A0, A1, A2) and Chip Select (CS0, CS1, $\overline{CS2}$) NOTE: The rising edge (↓) of the $\overline{ADS}$ signal is required when the Register Select (A0, A1, A2) and the Chip Select (CS0, CS1, $\overline{CS2}$) signals are not stable for the duration of a read or write operation. If not required, the $\overline{ADS}$ input can be tied permanently low.

PIN NUMBER	PIN NAME	SYMBOL	FUNCTION
26 27 28	REGISTER SELECT A2 REGISTER SELECT A1 REGISTER SELECT A0	A2 A1 A0	These three inputs are used to select a WD8250 internal register during a data read or write. See Table below.
29	NO CONNECT	NC	No Connect
30	INTERRUPT	INTRPT	Output goes high whenever an enabled interrupt is pending.
31	OUTPUT 2	$\overline{OUT2}$	User-designated output that can be programmed by Bit 3 of the modem control register = 1, causes $\overline{OUT2}$ to go low.
32	REQUEST TO SEND	$\overline{RTS}$	Output when low informs the modem or data set that the WD8250 is ready to transmit data. See Modem Control Register.
33	DATA TERMINAL READY	$\overline{DTR}$	Output when low informs the modem or data set that the WD8250 is ready to communicate.
34	OUTPUT 1	$\overline{OUT1}$	User designated output can be programmed by Bit 2 of Modem Control Register = 1 causes $\overline{OUT1}$ to go low.
35	MASTER RESET	MR	When high clears the registers to states as indicated in Table 1.
36	CLEAR TO SEND	$\overline{CTS}$	Input from DCE indicating remote device is ready to transmit. See Modem Control Register.
37	DATA SET READY	$\overline{DSR}$	Input from DCE used to indicate the status of the local data set. See Modem Control Register.
38	RECEIVED LINE SIGNAL DETECT	$\overline{RSLD}$	Input from DCE indicating that it is receiving a signal which meets its signal quality conditions. See Modem Control Register.
39	RING INDICATOR	$\overline{RI}$	Input, when low, indicates that a ringing signal is being received by the modem or data set. See Modem Control Register.
40	+5V	V_{CC}	+5 Volt Supply.

CHIP SELECTION AND REGISTER ADDRESSING

Address Strobe (ADS pin 25): When low provides latching for register select (A0, A1, A2) and chip select (CS0, CS1, $\overline{CS2}$).

NOTE: The rising edge (↓) of the $\overline{ADS}$ input is required when Register Select (A0, A1, A2) and Chip Select (CS0, CS1, $\overline{CS2}$) signals are not stable for the duration of a read or write operation. If $\overline{ADS}$ is not required for latching, this input can be tied permanently low.

Chip Select (CS0, CS1, $\overline{CS2}$) pins 12-14: The definition of chip selected is CS0, CS1 both high and $\overline{CS2}$ is low. Chip selection is complete when latched by $\overline{ADS}$ or $\overline{ADS}$ is tied low.

Register Select (A0, A1, A2) pins 26-28: To select a register for read or write operation, see Register Table.

NOTE: (DLAB) Divisor Latch access bit is the MSB of the Line Control Register. DLAB must be programmed high logic 1 by the system software to access the Baud Rate Generator Divisor Latches.

DLAB	A2	A1	A0	Register
0	0	0	0	Receiver Buffer (read), Transmitter Holding Register (write)
0	0	0	1	Interrupt Enable
X	0	1	0	Interrupt Identification (read only)
X	0	1	1	Line Control
X	1	0	0	MODEM Control
X	1	0	1	Line Status
X	1	1	0	MODEM Status
X	1	1	1	None
1	0	0	0	Divisor Latch (least significant byte)
1	0	0	1	Divisor Latch (most significant byte)

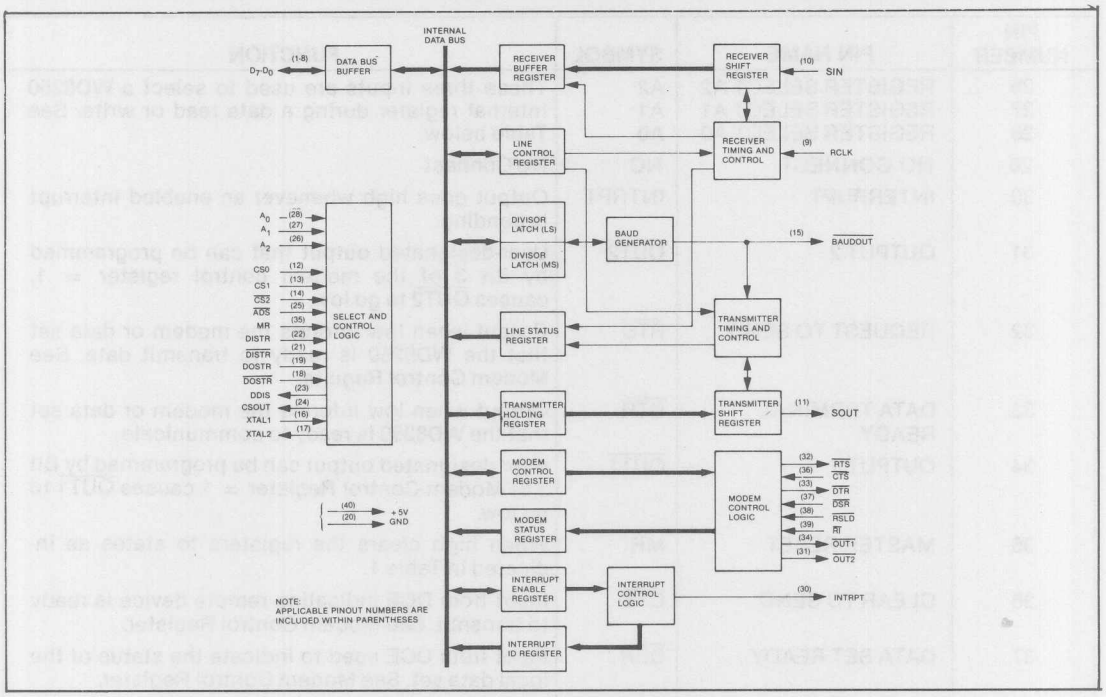
WD8250 OPERATIONAL DESCRIPTION

Master Reset

A high-level input on pin 35 causes the WD8250 to reset to the condition listed in Table 1.

WD8250 Accessible Registers

The system programmer has access to any of the registers summarized in Table 2. For individual register descriptions, refer to the following pages under register heading.



WD8250 BLOCK DIAGRAM

Table 1. Reset Control of Registers and Pinout Signals

Register/Signal	Reset Control	Reset State
Receiver Buffer Register	First Word Received	Data
Transmitter Holding Register	Writing into the Transmitter Holding Register	Data
Interrupt Enable Register	Master Reset	All Bits Low (0-3 forced and 4-7 permanent)
Interrupt Identification Register	Master Reset	Bit 0 is High and Bits 1-7 Are Permanently Low
Line Control Register	Master Reset	All Bits Low
MODEM Control Register	Master Reset	All Bits Low
Line Status Register	Master Reset	All Bits Low, Except Bits 5 and 6 Are High
Modem Status Register	Master Reset MODEM Signal Inputs	Bits 0-3 Low Bits 4-7 — Input Signal
Divisor Latch (low order bits)	Writing into the Latch	Data
Divisor Latch (high order bits)	Writing into the Latch	Data
SOUT	Master Reset	High
$\overline{\text{BAUDOUT}}$	Writing into either Divisor Latch	Low
CSOUT	$\overline{\text{ADS}}$ Strobe Signal and State of Chip Select Lines	High/Low
DDIS	DDIS = $\overline{\text{CSOUT}} \cdot \text{RCLK} \cdot \overline{\text{DISTR}}$ (At Master Reset, the CPU sets RCLK and DISTR low.)	High
INTRPT	Master Reset	Low

$\overline{OUT\ 2}$	Master Reset	High
$\overline{RTS}$	Master Reset	High
$\overline{DTR}$	Master Reset	High
$\overline{OUT\ 1}$	Master Reset	High
D7-D0 Data Bus Lines	In THREE-STATE Mode, Unless CSOUT • DISTR = High or CSOUT • DOSTR = High	THREE-STATE Data (ACE to CPU) Data (CPU to ACE)

Table 2. Summary of WD8250 Accessible Registers

	Register Address									
	0 DLAB=0	0 DLAB=0	1DLAB=0	2	3	4	5	6	0DLAB=1	1DLAB=1
Bit No.	Receiver Buffer Register (Read Only)	Transmitter Holding Register (Write Only)	Interrupt Enable Register	Interrupt Identification Register	Line Control Register	MODEM Control Register	Line Status Register	MODEM Status Register	Divisor Latch (LS)	Divisor Latch (MS)
0	Data Bit 0*	**Data Bit 0***	Enable Received Data Available Interrupt (ERBFI)	"0" if Interrupt Pending	Word Length Select Bit 0 (WLS0)	Data Terminal Ready (DTR)	Data Ready (DR)	Delta Clear to Send (DCTS)	Bit 0	Bit 8
1	Data Bit 1	Data Bit 1	Enable Transmitter Holding Register Empty Interrupt (ETBEI)	Interrupt ID Bit (0)	Word Length Select Bit 1 WLS1)	Request to Send (RTS)	Overrun Error (OR)	Delta Data Set Ready (DDSR)	Bit 1	Bit 9
2	Data Bit 2	Data Bit 2	Enable Receiver Line Status Interrupt (ELSI)	Interrupt ID Bit (1)	Number of Stop Bits (STB)	Out 1	Parity Error (PE)	Trailing Edge Ring Indicator (TERI)	Bit 2	Bit 10
3	Data Bit 3	Data Bit 3	Enable MODEM Status Interrupt (EDSSI)	0	Parity Enable (PEN)	Out 2	Framing Error (FE)	Delta Receive Line Signal Detect (DSLSD)	Bit 3	Bit 11
4	Data Bit 4	Data Bit 4	0	0	Even Parity Select (EPS)	Loop	Break Interrupt (BI)	Clear to Send (CTS)	Bit 4	Bit 12
5	Data Bit 5	Data Bit 5	0	0	Stick Parity	0	Transmitter Holding Register Empty (THRE)	Data Set Ready (DSR)	Bit 5	Bit 13
6	Data Bit 6	Data Bit 6	0	0	Set Break	0	Transmitter Shift Register Empty (TSRE)	Ring Indicator (RI)	Bit 6	Bit 14
7	Data Bit 7	Data Bit 7	0	0	Divisor Latch Access Bit (DLAB)	0	0	Received Line Signal Detect (RLSD)	Bit 7	Bit 15

*Bit 0 is the least significant bit. It is the first bit serially transmitted or received.

Line Control Register

Bits 0 and 1: These two bits specify the number of bits in each transmitted or received serial character. The encoding of bits 0 and 1 is as follows:

Bit 1	Bit 0	Word Length
0	0	5 Bits
0	1	6 Bits
1	0	7 Bits
1	1	8 Bits

Bit 2: This bit specifies the number of stop bits in each transmitted or received serial character. If bit 2 is a logic 0, 1 Stop bit is generated or checked in the transmit or receive data, respectively. If bit 2 is a logic 1 when a 5-bit word length is selected via bits 0 and 1, 1½ Stop bits are generated or checked. If bit 2 is a logic 1 when either a 6-, 7-, or 8-bit word length is selected, 2 Stop bits are generated or checked.

Bit 3: This bit is the Parity Enable bit. When bit 3 is a logic 1, a Parity bit is generated (transmit data) or checked (receive data) between the last data word bit and Stop bit of the serial data. (The Parity bit is used to produce an even or odd number of 1s when the data word bits and the Parity bit are summed.)

Bit 4: This bit is the Even Parity Select bit. When bit 3 is a logic 1 and bit 4 is a logic 0, an odd number of logic 1s is transmitted or checked in the data word bits and Parity bit. When bit 3 is a logic 1 and bit 4 is a logic 1, an even number of bits is transmitted or checked.

Bit 5: This bit is the Stick Parity bit. When bit 3 is a logic 1 and bit 5 is a logic 1, the Parity bit is transmitted and then detected by the receiver in the opposite state indicated by bit 4.

Bit 6: This bit is the Set Break Control bit. When bit 6 is a logic 1, the serial output (SOUT) is forced to the Spacing (logic 0) state and remains there (until reset by a low-level bit 6) regardless of other transmitter activity. The feature enables the CPU to alert a terminal in a computer communications system.

Bit 7: This bit is the Divisor Latch Access Bit (DLAB). It must be set high (logic 1) to access the Divisor Latches of the Baud Rate Generator during a Read or Write operation. It must be set low (logic 0) to access the Receiver Buffer, the Transmitter Holding Register, or the Interrupt Enable Register.

WD8250 Programmable Baud Rate Generator

The WD8250 contains a programmable Baud Rate Generator that is capable of taking any clock input (DC to 3.1 MHz) and dividing it by any divisor from 1 to $(2^{16} - 1)$. The output frequency of the Baud Generator is 16x the Baud rate. Two 8-bit latches store the divisor in a 16-bit binary format. These Divisor Latches must be loaded during initialization in order to insure desired operation of the Baud Rate Generator. Upon loading either of the Divisor Latches, a 16-bit Baud counter is immediately loaded. This prevents long counts on initial load.

Tables 3 and 4 illustrate the use of the Baud Generator with two different driving frequencies. One is referenced to a 1.8432 MHz crystal. The other is a 3.072 MHz crystal.

NOTE

The maximum operating frequency of the Baud Generator is 3.1 MHz. However, when using divisors of 6 and below, the maximum frequency is equal to 1/2 the divisor in MHz. For example, if the divisor is 1, then the maximum frequency is 1/2 MHz. In no case should the data rate be greater than 56K Baud.

Line Status Register

This 8-bit register provides status information to the CPU concerning the data transfer. The contents of

Table 3. Baud Rates Using 1.8432 MHz Crystal.

Desired Baud Rate	Divisor Used to Generate 16x Clock	Percent Error Difference Between Desired and Actual
50	2304	—
75	1536	—
110	1047	0.026
134.5	857	0.058
150	768	—
300	384	—
600	192	—
1200	96	—
1800	64	—
2000	58	0.69
2400	48	—
3600	32	—
4800	24	—
7200	16	—
9600	12	—
19200	6	—
38400	3	—
56000	2	2.86

NOTE: 1.8432 MHz is the standard 8080 frequency divided by 10.

Table 4. Baud Rates Using 3.072 MHz Crystal.

Desired Baud Rate	Divisor Used to Generate 16x Clock	Percent Error Difference Between Desired and Actual
50	3840	—
75	2560	—
110	1745	0.026
134.5	1428	0.034
150	1280	—
300	640	—
600	320	—
1200	160	—
1800	107	—
2000	96	—
2400	80	—
3600	53	0.628
4800	40	—
7200	27	1.23
9600	20	—
19200	10	—
38400	5	—
56000	3	14.285

the Line Status Register are indicated in table 2 and are described below.

Bit 0: This bit is the receiver Data Ready (DR) indicator. Bit 0 is set to a logic 1 whenever a complete incoming character has been received and transferred into the Receiver Buffer Register. Bit 0 will be reset to a logic 0 either by the CPU reading the data in the Receiver Buffer Register or by writing a logic 0 into it from the CPU.

Bit 1: This bit is the Overrun Error (OE) indicator. Bit 1 indicates that data in the Receiver Buffer Register was not read by the CPU before the next character was transferred into the Receiver Buffer Register, thereby destroying the previous character. The OE indicator is reset whenever the CPU reads the contents of the Line Status Register.

Bit 2: This bit is the Parity Error (PE) indicator. Bit 2 indicates that the received data character does not have the correct even or odd parity, as selected by the even-parity-select bit. The PE bit is set to a logic 1 upon detection of a parity error and is reset to a logic 0 whenever the CPU reads the contents of the Line Status Register.

Bit 3: This bit is the Framing Error (FE) indicator. Bit 3 indicates that the received character did not have a valid Stop bit. Bit 3 is set to a logic 1 whenever the Stop bit following the last data bit or parity bit is detected as a zero bit (Spacing level).

Bit 4: This bit is the Break Interrupt (BI) indicator. Bit 4 is set to a logic 1 whenever the received data input is held in the Spacing (Logic 0) state for longer than a full word transmission time (that is, the total time of Start bit + data bits + Parity + Stop bits).

NOTE

Bits 1 through 4 are the error conditions that produce a Receiver Line Status interrupt whenever any of the corresponding conditions are detected.

Bit 5: This bit is the Transmitter Holding Register Empty (THRE) indicator. Bit 5 indicates that the WD8250 is ready to accept a new character for transmission. In addition, this bit causes the WD8250 to issue an interrupt to the CPU when the Transmit Holding Register Empty Interrupt enable is set high. The THRE bit is set to a logic 1 when a character is transferred from the Transmitter Holding Register into the Transmitter Shift Register. The bit is reset to logic 0 concurrently with the loading of the Transmitter Holding Register by the CPU.

Bit 6: This bit is the Transmitter Shift Register Empty (TSRE) indicator. Bit 6 is set to a logic 1 whenever the Transmitter Shift Register is idle. It is reset to logic 0 upon a data transfer from the Transmitter Holding Register to the Transmitter Shift Register. Bit 6 is a read-only bit.

Bit 7: This bit is permanently set to logic 0.

Interrupt Identification Register

The WD8250 has an on chip interrupt capability that allows for complete flexibility in interfacing to all popular microprocessors presently available. In order to provide minimum software overhead during data character transfers, the WD8250 prioritizes interrupts into four levels. The four levels of interrupt conditions are as follows: Receiver Line Status (priority 1); Received Data Ready (priority 2); Transmitter Holding Register Empty (priority 3); and MODEM Status (priority 4).

Information indicating that a prioritized interrupt is pending and source of that interrupt are stored in the Interrupt Identification Register (refer to table 5). The Interrupt Identification Register (IIR), when addressed during chip-select time, freezes the highest priority interrupt pending and no other interrupts are acknowledged until the particular interrupt is serviced by the CPU. The contents of the IIR are indicated in table 2 and are described below.

Bit 0: This bit can be used in either a hardwired prioritized or polled environment to indicate whether an interrupt is pending. When bit 0 is a logic 0, an interrupt is pending and the IIR contents may be used as a pointer to the appropriate interrupt service routine. When bit 0 is a logic 1, no interrupt is pending and polling (if used) continues.

Bits 1 and 2: These two bits of the IIR are used to identify the highest priority interrupt pending as indicated in table 5.

Bits 3 through 7: These five bits of the IIR are always logic 0.

Interrupt Enable Register

This 8-bit register enables the four interrupt sources of the WD8250 to separately activate the chip Interrupt (INTRPT) output signal. It is possible to totally disable the interrupt system by resetting bits 0 through 3 of the Interrupt Enable Register. Similarly, by setting the appropriate bits of this register to a logic 1, selected interrupts can be enabled. Disabling the interrupt system inhibits the Interrupt Identification Register and the active (high) INTRPT output from the chip. All other system functions operate in their normal manner, including the setting of the Line Status and MODEM Status Registers. The contents of the Interrupt Enable Register are indicated in table 2 and are described below.

Bit 0: This bit enables the Received Data Available Interrupt when set to logic 1.

Bit 1: This bit enables the Transmitter Holding Register Empty Interrupt when set to a logic 1.

Bit 2: This bit enables the Receiver Line Status Interrupt when set to logic 1.

Table 5. Interrupt Control Functions.

Interrupt Identification Register			Interrupt Set and Reset Functions			
Bit 2	Bit 1	Bit 0	Priority Level	Interrupt Flag	Interrupt Source	Interrupt Reset Control
0	0	1	—	None	None	—
1	1	0	Highest	Receiver Line Status	Overrun Error or Parity Error or Framing Error or Break Interrupt	Reading the Line Status Register
1	0	0	Second	Received Data Available	Receiver Data Available	Reading the Receiver Buffer Register
0	1	0	Third	Transmitter Holding Register Empty	Transmitter Holding Register Empty	Reading the IIR Register (if source of interrupt) or Writing into the Transmitter Holding Register
0	0	0	Fourth	MODEM Status	Clear to Send or Data Set Ready or Ring Indicator or Received Line Signal Detect	Reading the MODEM Status Register

Bit 3: This bit enables the MODEM Status Interrupt when set to logic 1.

Bits 4 through 7: These four bits are always logic 0.

MODEM Control Register

This 8-bit register controls the interface with the MODEM or data set (or a peripheral device emulating a MODEM). The contents of the MODEM Control Register are indicated in table 2 and are described below.

Bit 0: This bit controls the Data Terminal Ready ($\overline{DTR}$) output. When bit 0 is set to a logic 1, the $\overline{DTR}$ output is forced to a logic 0. When bit 0 is reset to a logic 0, the $\overline{DTR}$ output is forced to a logic 1.

NOTE

The $\overline{DTR}$ output of the WD8250 may be applied to an EIA inverting line driver (such as the DS1488) to obtain the proper polarity input at the succeeding MODEM or data set.

Bit 1: This bit controls the Request to Send ($\overline{RTS}$) output. Bit 1 affects the $\overline{RTS}$ output in a manner identical to that described above for bit 0.

Bit 2: This bit controls the Output 1 ($\overline{OUT\ 1}$) signal, which is an auxiliary user-designated output. Bit 2 affects the $\overline{OUT\ 1}$ output in a manner identical to that described above for bit 0.

Bit 3: This bit controls the Output 2 ($\overline{OUT\ 2}$) signal, which is an auxiliary user-designated output. Bit 3 affects the $\overline{OUT\ 2}$ output in a manner identical to that described above for bit 0.

Bit 4: This bit provides a loopback feature for diagnostic testing of the WD8250. When bit 4 is set to logic 1, the following occur: the transmitter Serial Output (SOUT) is set to a logic one (high) state; the receiver Serial Input (SIN) is disconnected; the output of the Transmitter Shift Register is "looped back" into the Receiver Shift Register input; the four MODEM Control Inputs ($\overline{CTS}$, $\overline{DSR}$, $\overline{RLSD}$, and $\overline{RI}$) are disconnected; and the four MODEM Control outputs ($\overline{DTR}$, $\overline{RTS}$, $\overline{OUT\ 1}$, and $\overline{OUT\ 2}$) are internally connected to the four MODEM Control inputs. In the diagnostic mode, data that is transmitted is immediately received. This feature allows the processor to verify the transmit- and receive-data paths of the WD8250.

In the diagnostic mode, the receiver and transmitter interrupts are fully operational. The MODEM Control Interrupts are also operational but the interrupts' sources are now the lower four bits of the MODEM Control Register instead of the four MODEM Control inputs. The interrupts are still controlled by the Interrupt Enable Register.

The WD8250 interrupt system can be tested by writing into the lower six bits of the Line Status Register

and the lower four bits of the MODEM Status Register. Setting any of these bits to a logic 1 generates the appropriate interrupt (if enabled). The resetting of these interrupts is the same as in normal WD8250 operation. To return to this operation, the registers must be reprogrammed for normal operation and then bit 4 must be reset to logic 0.

Bits 5 through 7: These bits are permanently set to logic 0.

MODEM Status Register

This 8-bit register provides the current state of the control lines from the MODEM (or peripheral device) to the CPU. In addition to this current-state information, four bits of the MODEM Status Register provide change information. These bits are set to a logic 1 whenever a control input from the MODEM changes state. They are reset to logic 0 whenever the CPU reads the MODEM Status Register.

The contents of the MODEM Status Register are indicated in table 2 and are described below.

Bit 0: This bit is the Delta Clear to Send (DCTS) indicator. Bit 0 indicates that the $\overline{CTS}$ input to the chip has changed state since the last time it was read by the CPU.

Bit 1: This bit is the Delta Data Set Ready (DDSR) indicator. Bit 1 indicates that the $\overline{DSR}$ input to the chip has changed state since the last time it was read by the CPU.

Bit 2: This bit is the Trailing Edge of Ring Indicator (TERI) detector. Bit 2 indicates that the $\overline{RI}$ input to the chip has changed from an On (logic 1) to an Off (logic 0) condition.

Bit 3: This bit is the Delta Received Line Signal Detector (DRLSD) indicator. Bit 3 indicates that the $\overline{RLSD}$ input to the chip has changed state.

NOTE

Whenever bit 0, 1, 2, or 3 is set to logic 1, a MODEM Status Interrupt is generated.

Bit 4: This bit is the complement of the Clear to Send ($\overline{CTS}$) input.

Bit 5: This bit is the complement of the Data Set Ready ($\overline{DSR}$) input.

Bit 6: This bit is the complement of the Ring Indicator ($\overline{RI}$) input.

Bit 7: This bit is the complement of the Received Line Signal Detect ($\overline{RLSD}$) input.

Typical Applications

Figures 1 and 2 show how to use the WD8250 chip in an 8080A system and in a microcomputer system with a high-capacity data bus.

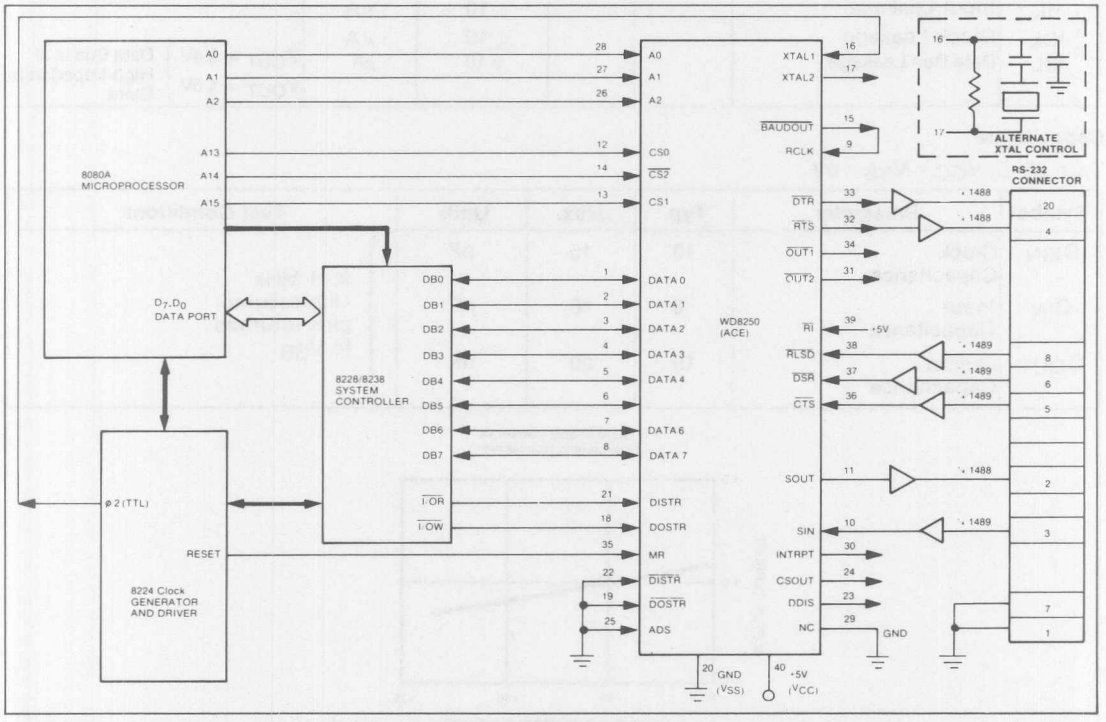


FIGURE 1. TYPICAL 8-BIT MICROPROCESSOR/RS-232 TERMINAL INTERFACE USING THE ACE.

Typical Applications (continued)

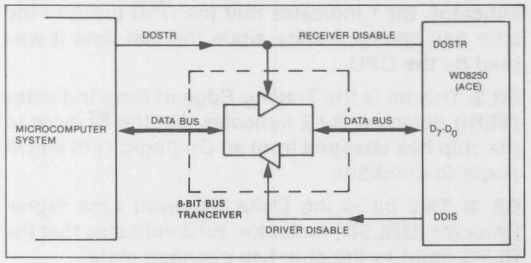


FIGURE 2. TYPICAL INTERFACE FOR A HIGH-CAPACITY DATA BUS.

ABSOLUTE MAXIMUM RATINGS

Temperature Under Bias ..... 0°C to +70°C
Storage Temperature -65°C to +150°C (Ceramic)
-50°C to +125°C (Plastic)
All Input or Output Voltages with
Respect to V_{SS} ..... -0.5 V to +7.0 V
Power Dissipation ..... 750 mW

Absolute maximum ratings indicate limits beyond which permanent damage may occur. Continuous operation at these limits is not intended; operation should be limited to those conditions specified under DC Electrical Characteristics.

DC Electrical Characteristics

T_A = 0°C to +70°C, V_{CC} = +5V ± 5%, V_{SS} = 0V, unless otherwise specified.

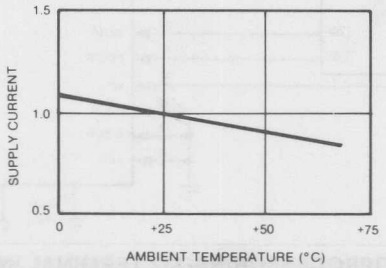
Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
V_{ILX}	Clock Input Low Voltage	-0.5		0.8	V	
V_{IHX}	Clock Input High Voltage	2.4		V_{CC}	V	
V_{IL}	Input Low Voltage	-0.5		0.8	V	
V_{IH}	Input High Voltage	2.4		V_{CC}	V	
V_{OL}	Output Low Voltage			.45	V	I_{OL}=1.6mA on all outputs
V_{OH}	Output High Voltage	2.4			V	I_{OH}=-100 μA
$I_{CC(AV)}$	Avg Power Supply Current (V_{CC})			150	ma	
I_{IL}	Input Leakage			± 10	μA	
I_{CL}	Clock Leakage			± 10	μA	
I_{DL}	Data Bus Leakage			± 10	μA	V_{OUT} = 0.4V, V_{OUT} = 4.6V: Data Bus is at High-Impedance State

Capacitance

T_A = 25°C, V_{CC} = V_{SS} = 0V

Symbol	Parameter	Typ.	Max.	Units	Test Conditions
C_{XIN}	Clock Capacitance	10	15	pF	fc=1 MHz, Unmeasured pins returned to V_{SS}
C_{IN}	Input Capacitance	6	10	pF	
C_{OUT}	Output Capacitance	10	20	pF	

Typical Supply Current vs. Temperature, Normalized

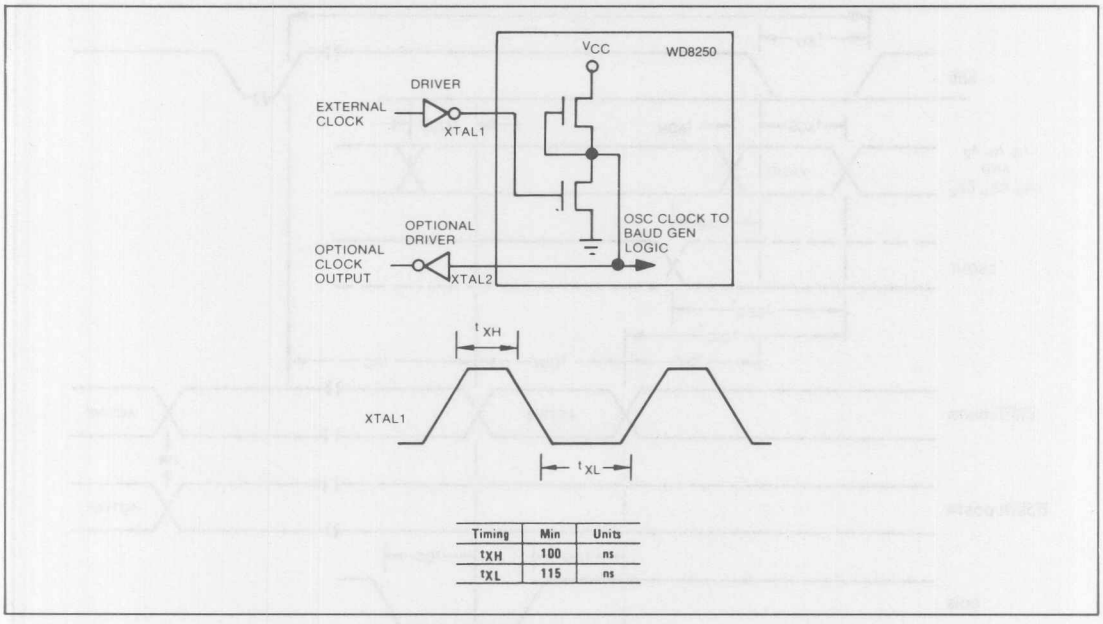


AC Electrical Characteristic T_A = 0°C to +70°C, V_{CC} = +5V ± 5%

Symbol	Parameter	Units	Min	Max	Test Conditions
t_{AW}	Address Strobe Width	ns	120		1TTL Load
t_{ACS}	Address and Chip Select Setup Time	ns	100		1TTL Load
t_{ACH}	Address and Chip Select Hold Time	ns	10		1TTL Load
t_{CSS}	CSOUT Delay from Latch	ns		160	1TTL Load
t_{DID}	$\overline{DISTR}$/DISTR Delay from Latch	ns	50		1TTL Load
t_{DIW}	$\overline{DISTR}$/DISTR Strobe Width	ns	300		1TTL Load
t_{RC}	Read Cycle Delay	ns	655		1TTL Load
RC	Read Cycle = $t_{ACS} + t_{DID} + t_{DIW} + t_{RC}$ + 20 ns	ns	1125		1TTL Load
t_{DD}	$\overline{DISTR}$/DISTR to Driver Disable Delay	ns		200	1TTL Load
t_{DDD}	Delay from $\overline{DISTR}$/DISTR to Data	ns		300	1TTL Load
t_{HZ}	$\overline{DISTR}$/DISTR to Floating Data Delay	ns	60		1TTL Load
t_{DOD}	$\overline{DOSTR}$/DOSTR Delay From Latch	ns	20		1TTL Load
t_{DOW}	$\overline{DOSTR}$/DOSTR Strobe Width	ns	175		1TTL Load
t_{WC}	Write Cycle Delay	ns	685		1TTL Load
WC	Write Cycle = $t_{ACS} + t_{DOD} + t_{DOW} + t_{WC}$ + 20 ns	ns	1000		1TTL Load
t_{DS}	Data Setup Time	ns	175		1TTL Load
t_{DH}	Data Hold Time	ns	60		1TTL Load
t_{CSC}*	CSOUT Delay from Select	ns		260	1TTL Load
t_{DIC}*	$\overline{DISTR}$/DISTR Delay from Select	ns	150		1TTL Load
t_{DOC}*	$\overline{DOSTR}$/DOSTR Delay from Select	ns	150		1TTL Load
t_{ACR}*	Address and Chip Select Hold Time from $\overline{DISTR}$/DISTR	ns	10		1TTL Load
t_{ACW}*	Address and Chip Select Hold Time fom $\overline{DOSTR}$/DOSTR	ns	10		1TTL Load
t_{MR}	Master Reset Pulse Width	ns	500		1TTL Load

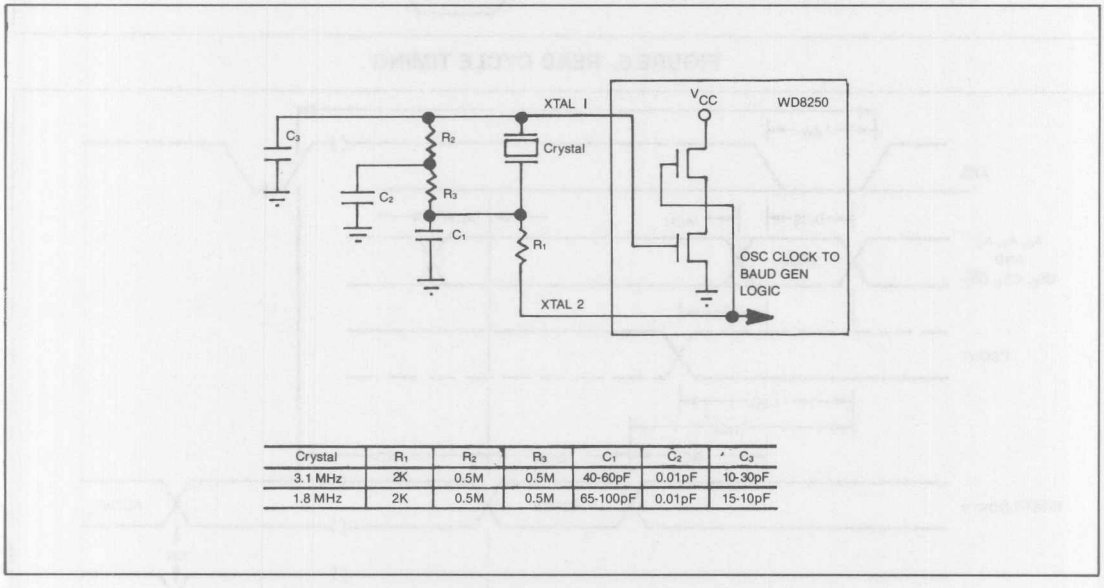
*Only applicable when ADS is permanently low.

Symbol	Parameter	Min.	Max.	Units	Test Conditions
Baud Generator					
N	Baud Rate Divisor	1	$2^{16}-1$		
t_{BLD}	Baud Output Negative Edge Delay		250	ns	100pF Load
t_{BHD}	Baud Output Positive Edge Delay		250	ns	100pF Load
t_{LW}	Baud Output Down Time	425		ns	100pF Load
t_{HW}	Baud Output Up Time	330		ns	100pF Load
Receiver					
t_{SCD}	Delay from RCLK to Sample Time		2	μs	
t_{SINT}	Delay from Stop to Set Interrupt		2	μs	100pF Load
t_{RINT}	Delay from $\overline{\text{DISTR}}$/DISTR (RD RBR) to Reset Interrupt	.250	1	μs	100pF Load
Transmitter					
t_{HR}	Delay from $\overline{\text{DOSTR}}$/DOSTR (WR THR) to Reset Interrupt	.250	1	μs	100pF Load
t_{IRS}	Delay from Initial INTR Reset to Transmit Start		16	$\overline{\text{BAUDOUT}}$ Cycles	
t_{SI}	Delay from Initial Write to Interrupt		24	$\overline{\text{BAUDOUT}}$ Cycles	
t_{SS}	Delay from Stop to Next Start	.250	1	μs	
t_{STI}	Delay from Stop to Interrupt (THRE)		8	$\overline{\text{BAUDOUT}}$ Cycles	
T_{IR}	Delay from $\overline{\text{DISTR}}$/DISTR (RD IIR) to Reset Interrupt (THRE)	.250	1	μs	100pF Load
Modem Control					
t_{MDO}	Delay from DOSTR/$\overline{\text{DOSTR}}$ (WR MCR) to Output	.250	1	μs	100pF Load
t_{SIM}	Delay to Set Interrupt from MODEM Input	.250	1	μs	100pF Load
t_{RIM}	Delay to Reset Interrupt from $\overline{\text{DISTR}}$/DISTR (RD MSR)	.250	1	μs	100pF Load



Timing	Min	Units
t_{XH}	100	ns
t_{XL}	115	ns

FIGURE 3. EXTERNAL CLOCK INPUT (3.1 MHz MAX.)



Crystal	R_1	R_2	R_3	C_1	C_2	C_3
3.1 MHz	2K	0.5M	0.5M	40-60pF	0.01pF	10-30pF
1.8 MHz	2K	0.5M	0.5M	65-100pF	0.01pF	15-10pF

FIGURE 4. TYPICAL CRYSTAL OSCILLATOR NETWORK

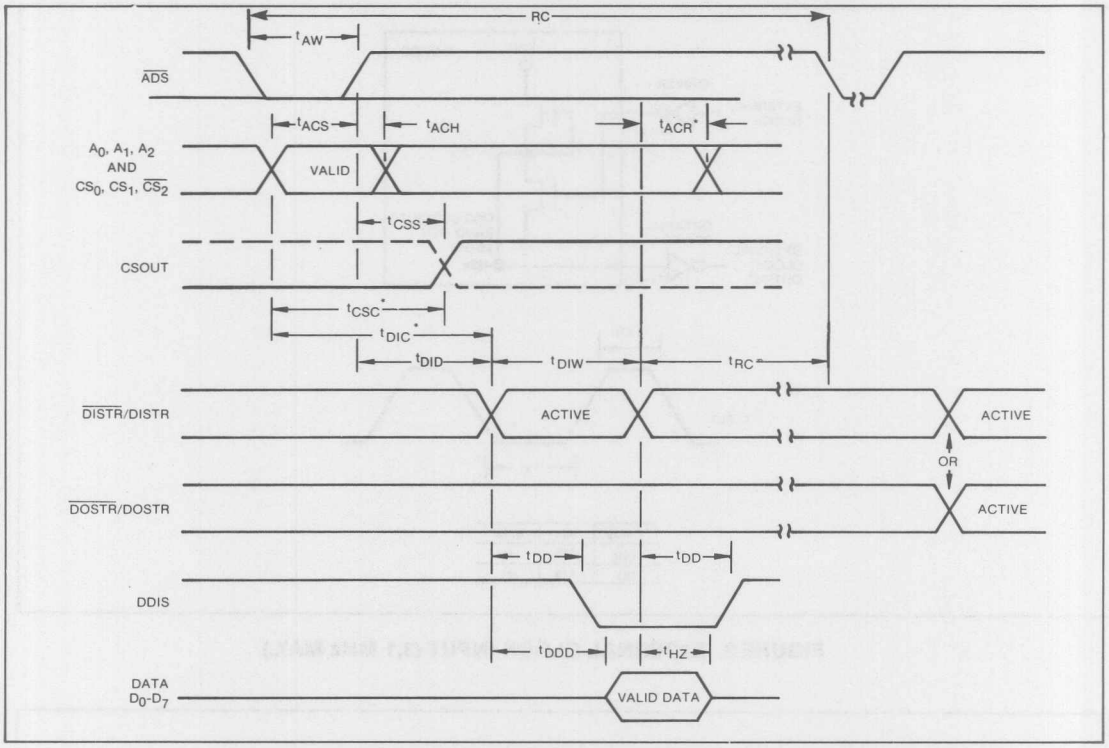


FIGURE 5. READ CYCLE TIMING

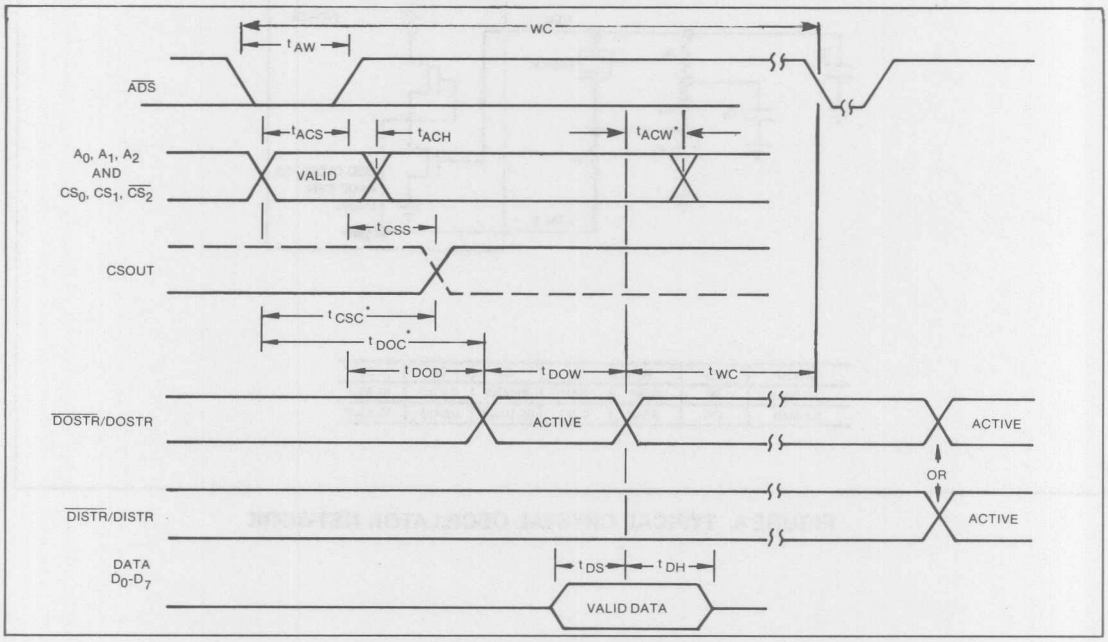


FIGURE 6. WRITE CYCLE TIMING

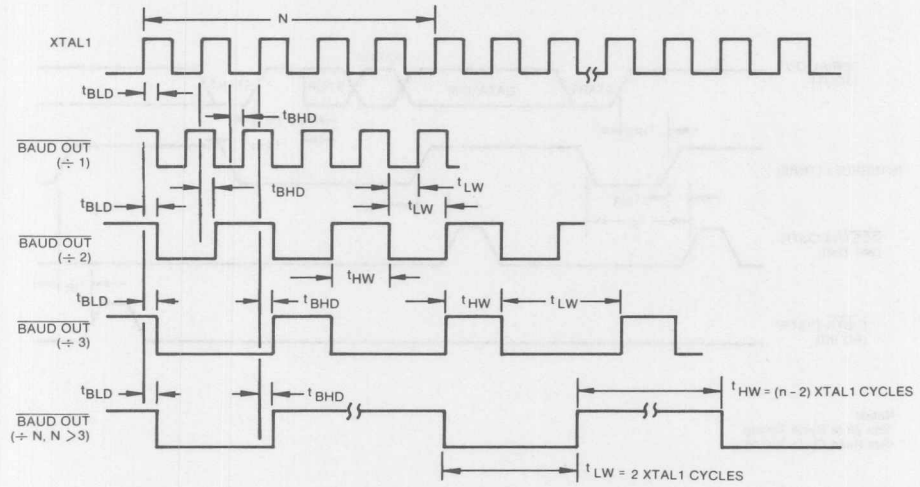
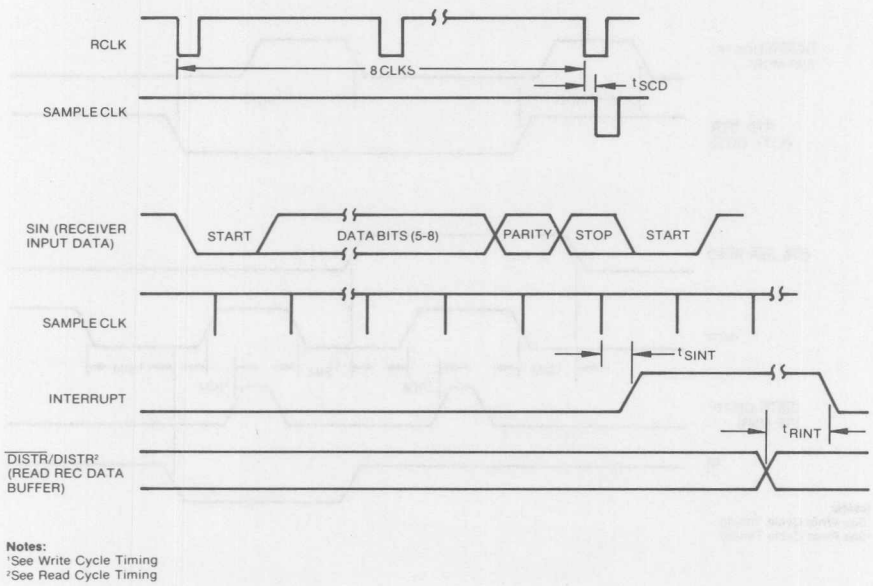
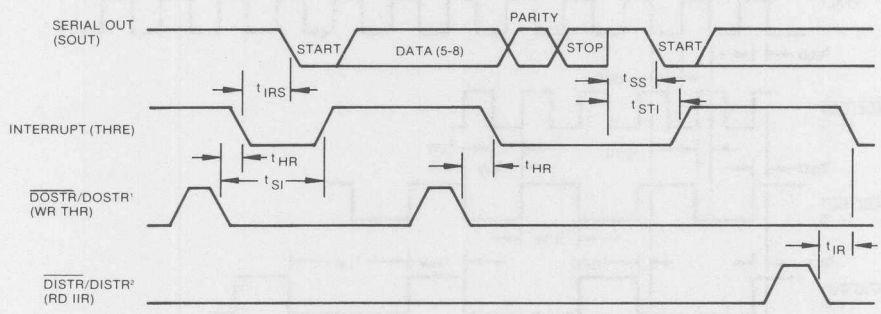


FIGURE 7. BAUDOUT TIMING



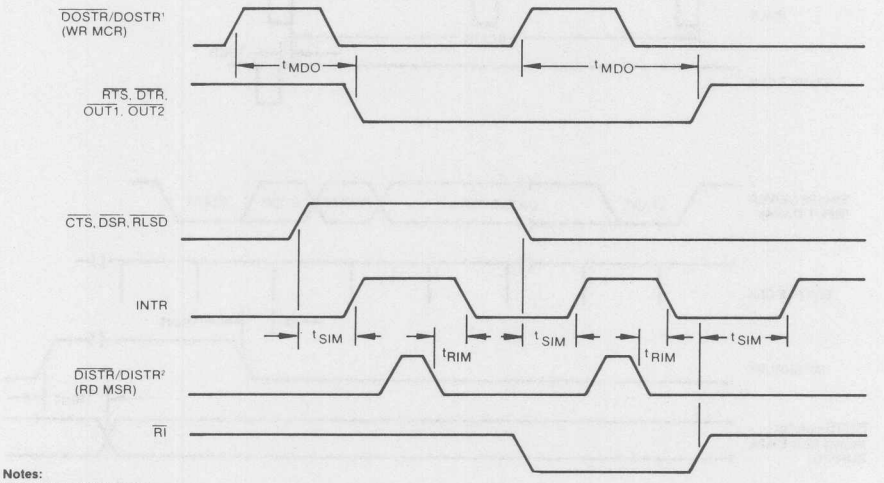
Notes:
¹See Write Cycle Timing
²See Read Cycle Timing

FIGURE 8. RECEIVER TIMING



Notes:
[1]See Write Cycle Timing
[2]See Read Cycle Timing

FIGURE 9. TRANSMITTER TIMING



Notes:
[1]See Write Cycle Timing
[2]See Read Cycle Timing

FIGURE 10. MODEM CONTROLS TIMING

ORDERING INFORMATION

Part Number	Max Clock Rate[1]	Bits/Character
WD8250*-00	3.1 MHz	5, 6, 7, 8
WD8250*-20	3.1 MHz	6, 7, 8
WD8250*-30	500 kHz	5, 6, 7, 8

NOTES:

1. This is the maximum clock rate that can be applied to pins 16 or 17.

* Consult your local Western Digital Sales Representative for information regarding package availability, price, and delivery.

Printed in U.S.A.

See page 429 for ordering information.

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ADVANCED INFORMATION

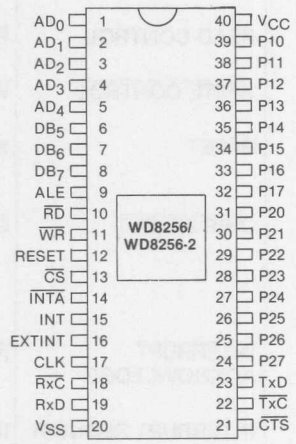
WD8256, WD8256-2 Programmable Multifunction UART (MUART)

FEATURES

- WD8256 COMPATIBLE WITH 3 MHZ SYSTEM CLOCK PROCESSORS.
- WD8256-2 COMPATIBLE WITH 5 MHZ SYSTEM CLOCK PROCESSORS.
- FULL-DUPLEX ASYNCHRONOUS SERIAL INTERFACE WITH PROGRAMMABLE 5-8 DATA BITS, 0.75-2 STOP BITS, PARITY GENERATION AND CHECKING.
- INTERNAL BAUD RATE GENERATOR PROGRAMMABLE FROM 50-19200 BAUD; 0-1 MEGABAUD POSSIBLE WITH EXTERNAL BAUD RATE CLOCK.
- INTERRUPT CONTROLLER WITH 8 PRIORITY LEVELS; EACH LEVEL INDEPENDENTLY MASKABLE, PROGRAMMABLE FOR NORMAL AND FULLY NESTED OPERATION.
- FIVE PROGRAMMABLE 8-BIT COUNTER/TIMERS, (INTERNAL OR EXTERNAL CLOCK) FOUR CASCADABLE TO TWO 16-BIT COUNTER/TIMERS.
- TWO 8-BIT I/O PORTS, BIT PROGRAMMABLE FOR INPUT/OUTPUT, HAND-SHAKE MODE SUPPORTED.

DESCRIPTION

WD8256 integrates four of the most used peripheral functions in a microcomputer system into a 40 pin package; serial interface, parallel interface, timer/counter and interrupt controller. It is primarily suited for system which have a multiplexed bus. With some additional circuitry, it can also be used with other processors. All the functions of WD8256 are programmable by software, leading to a great flexibility in system design.



PIN DESIGNATION

PIN DESCRIPTION

PIN NUMBER	PIN NAME	SYMBOL	FUNCTION
1-8	INTERFACE TO MULTIPLEXED BUS	AD0-AD4, DB5-DB7	Bidirectional lines to 8 data bits and 5 least significant address bits which are latched internally on the falling edge of ALE.
9	ADDRESS LATCH ENABLE	ALE	The five least significant address bits and $\overline{CS}$ are latched on the falling edge of ALE into an internal register.
10	READ CONTROL	$\overline{RD}$	The microprocessor reads data from the chip when this signal is low.
11	$\overline{WRITE\ CONTROL}$	$\overline{WR}$	The microprocessor writes data into the chip with a low on this pin.
12	RESET	RESET	A high on this pin forces the chip to its initial state. The chip remains in this state till control information is written into the chip.
13	$\overline{CHIP\ SELECT}$	$\overline{CS}$	A low on this pin during ALE enables the bus interface of the chip. Neither read nor write operations are possible without this enable. The signal has no effect on the internal operation of the chip.
14	$\overline{INTERRUPT}$ ACKNOWLEDGE	$\overline{INTA}$	The microprocessor informs the chip a low on this pin that an interrupt request is being serviced, if this function has been enabled.
15	INTERRUPT REQUEST	INT	The chip demands interrupt service from the microprocessor with a high on this output.
16	EXTERNAL INTERRUPT	EXTINT	An external source can request interrupt service through this input. The source can be either a peripheral or another WD8256 with its INT pin as the signal source. The input is level sensitive (high). The request must be held high until the processor acknowledges it.
17	SYSTEM CLOCK	CLK	Clock on this input is the reference clock for various function like timers, baud rate generator etc.
18	$\overline{RECEIVER\ CLOCK}$	$\overline{RxC}$	If this pin is programmed as an output, it provides a low-to-high transition at the sampling point of each received data bit (excluding the framing bits). When programmed as an input, an externally generated receiver clock must be connected to this pin. Its frequency can range from DC to 1.024 MHz matching the receiver baud rate. The internal baud rate generator is disabled if this pin is as input.
19	RECEIVER DATA	RxD	Input for serial data, which is converted to parallel format while discarding the framing bits and then is made available to the processor.

PIN DESCRIPTION (CONT.)

PIN NUMBER	PIN NAME	SYMBOL	FUNCTION
20	GROUND (0V)	V_{SS}	
21	CLEAR TO SEND	$\overline{CTS}$	This input enables the serial transmitter. If 1, 1.5 or 2 stop bits are selected, $\overline{CTS}$ is level sensitive. As long as $\overline{CTS}$ is low, any character loaded into the transmitter buffer register will be transmitted serially. For continuous transmission, this input must be tied to low. A single negative going pulse causes the transmission of a single character previously loaded into the transmitter buffer register. If the transmitter buffer is empty, this pulse will be ignored. If this pulse occurs during the transmission of a character upto the time where 0.5 of the first (or the only) stop bit is sent out, it will be ignored. If it occurs afterwards, but before the end of the stop bits the next character will be transmitted immediately following the current one. If $\overline{CTS}$ is still high when the transmitter register is sending the last stop bit, the transmitter will enter its idle state until the next high-to-low transition on $\overline{CTS}$ occurs. If 0.75 stop bits is chosen, $\overline{CTS}$ input is edge sensitive. A negative edge on $\overline{CTS}$ results in the immediate transmission of the next character. The length of the stop bits is determined by the time interval between the beginning of the first stop bit and the next negative edge on $\overline{CTS}$. A high-to-low transition has no effect if the transmitter buffer is empty or if the time interval between the beginning of the stop bit and next negative edge is less than 0.75 bit. A high or a low level or a low-to-high transition has no effect on the transmitter for the 0.75 stop bit mode.
22	$\overline{TRANSMITTER\ CLOCK}$	$\overline{TxC}$	The function of this pin can be programmed in 3 configurations. As an output it delivers the transmitter clock corresponding to the baud rate. If programmed as an input, an external clock of 32 or 64 times the baud rate that is common to transmitter and receiver, or a 1x clock matching the baud rate which is used for the transmitter only, can be tied to this pin. The maximum frequency is 1.024 MHz. Thus, baud rates ranging from 0 to 16 K Baud (64x) or from 0 to 32 K Baud (32x) or from 0 to 1.024 Mbaud (1x) are possible. The internal baudrate generator is disabled if $\overline{TxC}$ is selected as input.
23	TRANSMITTER DATA	TxD	Serial data output. The parallel data received from the processor and the framing bits added by the WD8256 are sent out serially over this output when the transmitter is enabled by the $\overline{CTS}$ signal.

PIN DESCRIPTION (CONT.)

PIN NUMBER	PIN NAME	SYMBOL	FUNCTION
24-31	PARALLEL I/O PORT 2	P27-P20	The eight general purpose I/O pins of parallel port 2 can be configured in sets of four pins (nibbles) as inputs or outputs or 8 bit I/O with handshake (control-signals at port 1). In the nibble mode the output signals are latched whereas the input signals are not. In the handshake mode both inputs and outputs are latched.
32-39	PARALLEL I/O PORT 1	P17-P10	Each one of these 8 pins can be programmed as input or output. Alternatively these pins can serve as control pins which extends considerably the functional spectrum of the chip. The pins are assigned special functions implicitly by programming. All outputs are latched whereas inputs are not.
40	POWER SUPPLY (+5 V)	V_{CC}	

See page 429 for ordering information.

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WESTERN DIGITAL
CORPORATION

PR1472 (PSAR)
Programmable Synchronous & Asynchronous Receiver

FEATURES

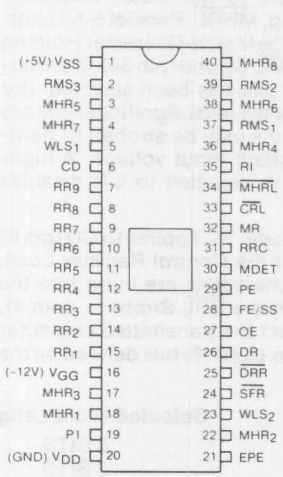
- SYNCHRONOUS, ASYNCHRONOUS OR ISOCHRONOUS OPERATION
- DC TO 640K BITS/SEC (1X CLOCK) PR1472-01; DC TO 100K BITS/SEC PR1472
- PROGRAMMABLE MATCH (FILL) CHARACTER WITH MATCH DETECT FLAG.
- INTERNAL OR EXTERNAL CHARACTER SYNCHRONIZATION
- NINE BIT WIDE RECEIVER HOLDING REGISTER
- SELECTABLE 5, 6, 7 OR 8 BITS PER CHARACTER
- EVEN/ODD OR NO PARITY SELECT
- PROGRAMMABLE CLOCK RATE; 1X, 16X, 32X OR 64X
- AUTOMATIC START AND STOP BIT STRIPPING
- AUTOMATIC CHARACTER STATUS AND FLAG GENERATION
- THREE STATE OUTPUTS — BUS STRUCTURE CAPABILITY
- DOUBLE BUFFERED
- TTL & DTL COMPATIBLE — INTERNAL ACTIVE PULLUP
- COMPATIBLE TRANSMITTER, PT1482

GENERAL DESCRIPTION

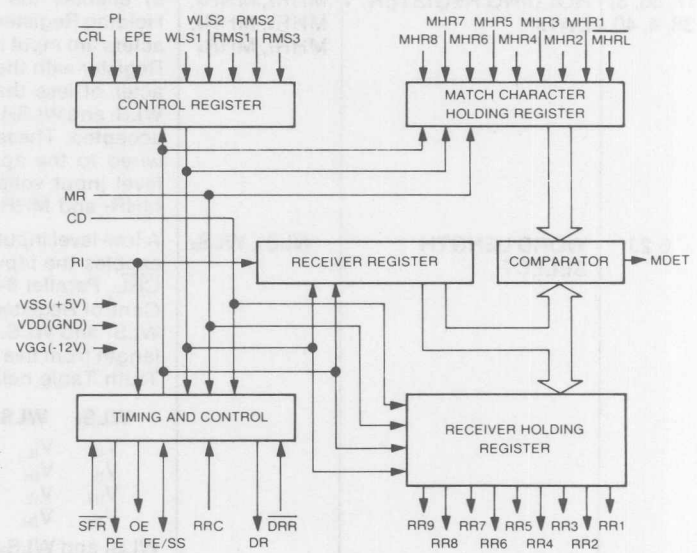
The Western Digital PR1472 (PSAR) is a programmable receiver that interfaces variable length serial data to a parallel data channel. The receiver converts a serial data stream into parallel characters with a format compatible with all standard Synchronous, Asynchronous, or Isochronous data communications media.

Contiguous synchronous serial characters are compared to a programmable Match-Character Holding Register, character synchronized and assembled. Programming the Asynchronous or Isochronous Mode provides assembly of characters with start and stop bit(s) which are stripped from the data. Four internal registers, in conjunction with Three-State Outputs provide full system versatility.

The PSAR is a TTL compatible device. The use of internal active pull-up devices and push-pull output drivers, provides direct compatibility with all forms of current sinking logic. Western Digital also offers a Compatible Transmitter, the PT1482.



PIN CONNECTIONS



PR1472 BLOCK DIAGRAM

PIN NUMBER	I/O NAME	SYMBOL	FUNCTION
1	POWER SUPPLY	V_{SS}	+5 Volt Supply
37, 39, 2	RECEIVER MODE SELECT	RMS_1, RMS_2, RMS_3	A low-level input voltage, V_{IL}, applied to CD (pin 6) enables RMS_1, RMS_2, and RMS_3 inputs. The Receiver Mode Select Inputs, in conjunction with the Control Register Load and Chip Disable, select the Receiver operating mode. RMS_1, RMS_2, and RMS_3 may be strobed or hard-wired to the appropriate input voltage.
			RMS_3 / RMS_2 / RMS_1 / Selected Operating Mode 0 0 0 ASYNCH OR ISOCH, 1X CLOCK 0 0 1 ASYNCH OR ISOCH, 16X CLOCK 0 1 0 ASYNCH OR ISOCH, 32X CLOCK 0 1 1 ASYNCH OR ISOCH, 64X CLOCK 1 X 0 SYNCH-EXTERNAL CHARACTER SYNCHRONIZATION 1 X 1 SYNCH-INTERNAL CHARACTER SYNCHRONIZATION
			NOTE: When operating in asynchronous or isochronous mode with 1X clock there is no protection against false start bits.
			A high-level input voltage, V_{IH}, applied to CD disables RMS_1, RMS_2 and RMS_3.
18,22 17, 36, 3, 38, 4, 40	MATCH-CHARACTER HOLDING REGISTER DATA	MHR_1, MHR_2, MHR_3, MHR_4, MHR_5, MHR_6, MHR_7, MHR_8	A low-level input voltage, V_{IL}, applied to CD (pin 6) enables the inputs to the Match-Character Holding Register Load, $\overline{MHRL}$. Parallel 8-bit characters are input into the Match-Character Holding Register with the $\overline{MHRL}$ Strobe (pin 34). If a character of less than 8 bits has been selected (by WLS_1 and WLS_2), only the least significant bits are accepted. These inputs may be strobed or hard-wired to the appropriate input voltage. A high-level input voltage, V_{IL}, applied to CD disables MHR_1 and MHR_8.
5,23	WORD LENGTH SELECT	WLS_1, WLS_2	A low-level input voltage, V_{IL}, applied to CD (pin 6) enables the inputs of the Control Register Load, $\overline{CRL}$. Parallel 8-bit characters are input into the Control Register with the $\overline{CRL}$ Strobe (pin 4), WLS_1 and WLS_2 select the transmitted character length from five (5) to eight (8) bits defined by the Truth Table below:
			WLS_2 / WLS_1 / Selected Word Length V_{IL} V_{IL} 5 BITS V_{IL} V_{IH} 6 BITS V_{IH} V_{IL} 7 BITS V_{IH} V_{IH} 8 BITS
			WLS_1 and WLS_2 may be strobed or hard-wired to the appropriate input voltage. A high-level input voltage, V_{IH}, applied to CD disables WLS_1 and WLS_2.

PIN NUMBER	I/O NAME	SYMBOL	FUNCTION
6	CHIP DISABLE	CD	This line controls the disable associated with busable inputs and Three-State outputs. A high-level input voltage, V_{IH}, applied to this line disables inputs and removes drive from push-pull output buffers causing them to float. Drivers of disables outputs are not required to sink or source current. The I/O Lines controlled by Chip Disable are defined below: **Input Lines** — **Three-State Output Lines** $\overline{CRL}$ — $\overline{DRR}$ — PE — RR_1-RR_8 EPE — $\overline{SFR}$ — FE PI — $\overline{MHRL}$ — OE WLS_1WLS_2 — MHR_1-MHR_8 RMS_1-RMS_3
7-15	RECEIVER HOLDING-REGISTER DATA OUTPUT	RR_9-RR_1	A low-level input voltage, V_{IL}, applied to CD (pin 6) enables the Receiver Holding Register outputs, RR_1-RR_9. The parallel data character, including parity (RR_9), appears on these lines. Program control selection of a word length less than eight (8) bits will cause the most significant bits of the character to be forced to a low-level output voltage, V_{OL}. The character will be right justified. RR_1 (pin 15) is the least significant bit of the character. A high-level input voltage, V_{IH}, applied to CD disables RR_1-RR_9.
16	POWER SUPPLY	V_{GG}	– 12 Volts Supply.
19	PARITY INHIBIT	PI	A low-level input voltage, V_{IL}, applied to CD (pin 6) enables the EPE and PI inputs.
20	POWER SUPPLY	V_{DD}	Ground = 0V
21	EVEN PARITY ENABLE	EPE	The Even Parity Enable Input and the Parity Inhibit Input to the Control Register, in conjunction with the Control Register Load and Chip Disable, select even, odd or no parity to be verified by the receiver. A high-level input voltage, V_{IH}, applied to EPE selects even parity and a low-level input voltage, V_{IL}, select odd parity if a low-level input voltage is applied to Parity Inhibit and Chip Disable. PI and EPE may be strobed or hard-wired to the appropriate input voltage. **PI** — **EPE** — **Selected Parity** — **Comments** V_{IL} — V_{IL} — Odd — CD = V_{IL} V_{IL} — V_{IH} — Even — CD = V_{IL} V_{IH} — X — None — CD = V_{IL} NOTE: If CD = V_{IH}, no programming is performed since inputs are disabled. X — either V_{IL} or V_{IH}. When programmed, the appropriate parity is verified following the last data bit of a character, immediately preceding the stop element of asynchronous and isochronous characters. A high-level input voltage, V_{IH}, applied to CD disables EPE, PI, and $\overline{CRL}$.
29	PARITY ENABLE	PE	A high-level input V_{IH} enables parity. A low level input V_{IH} disables parity.

PIN NUMBER	I/O NAME	SYMBOL	FUNCTION
24	$\overline{\text{STATUS FLAG RESET}}$	$\overline{\text{SFR}}$	A low-level input voltage, V_{IL}, applied to CD (pin 6) enables the $\overline{\text{SFR}}$ input. A low-level input voltage, V_{IL}, applied to this line resets the PE, FE and OE Status Flags.
25	$\overline{\text{DATA RECEIVED RESET}}$	$\overline{\text{DRR}}$	A low-level input voltage, V_{IL}, applied to CD (pin 6) enables the $\overline{\text{DRR}}$ input. A low-level input voltage, V_{IL}, applied to this line resets the DR Flag. A high-level input voltage, V_{IH}, applied to CD disables $\overline{\text{DRR}}$.
26	DATA RECEIVED FLAG	DR	A high-level output voltage, V_{OH}, indicates that an entire character has been received and transferred to the Receiver Holding Register. When operating in the synchronous mode, the first SYN character, when located and transferred to the Receiver Holding Register, will not cause DR to go to a high-level output voltage, V_{OH}, but will cause MDET to go to a high-level output voltage. Character transfer to the Receiver Holding Register occurs in the center of the last bit of a synchronous character or the center of the first STOP element of an asynchronous or isochronous character at which time this flag is updated.
27	OVERRUN ERROR FLAG	OE	A low-level input voltage, V_{IL}, applied to CD (pin 6) enables the OE input. A high-level output voltage, V_{OH}, indicates that the prevously received character was not read (DR line not reset) and was, therefore, lost before the present character was transferred to the Receiver Holding Register. This transfer occurs in the center of the last bit of a received synchronous character or in the center of the first STOP element of an asynchronous or isochronous character at which time this flag is updated. A high-level input voltage, V_{OH}, applied to CD disables OE.
28	FRAMING ERROR/ SYN SEARCH	FE/SS	FE/SS is a two-way (I/O) bus. If programmed for the ASYNCHRONOUS or ISOCHRONOUS MODE, a low-level input voltage, V_{IL}, applied to CD (pin 6) enables the FRAMING ERROR FLAG output which indicates the status of the STOP BIT detection circuit. A high-level output voltage, V_{OH}, indicates that the character transferred to the Receiver Holding Register has no valid STOP BIT; i.e., the bit following the PARITY BIT is not a high-level input voltage, V_{IH}. This transfer occurs in the center of the first stop element at which time this flag is updated. When programmed for the SYNCHRONOUS MODE, this line is an input and is not under control of CD. This line should be driven by a tri-state or an open collector device. If programmed for INTERNAL CHARACTER SYNCHRONIZATION, a transition from a low-level input voltage, V_{IL}, to a high-level input voltage, V_{IH}, initiates the automatic internal "SYN" CHARACTER search operation.

PIN NUMBER	I/O NAME	SYMBOL	FUNCTION
28	FRAMING ERROR/ SYN SEARCH	FE/SS	Prior to initiation of this operation, the Receiver Holding Register is "transparent" so that its contents are identical to that of the RECEIVER REGISTER. Upon receipt of a SYN character, (previously loaded into the Match-Character Holding Register during initialization), the Receiver Holding Register becomes non-transparent, the MATCH DETECT output (MDET) goes to a high-level output voltage. V_{OH}, but, the Data Received (DR) FLAG does not assume a high-level output voltage, V_{OH}. The P/SAR is now in character synchronization. Subsequent SYN or data character will be transferred to the RECEIVER HOLDING REGISTER as they are assembled (at the center of the last bit) and the DR FLAG will be raised. A transition from a high-level input voltage, V_{IH}, to a low-level input voltage, V_{IL}, causes the P/SAR to lose character synchronization and forces the Receiver Holding Register to become "transparent." If programmed for EXTERNAL CHARACTER SYNCHRONIZATION, the system external to the P/SAR examines the data stream for "SYN" characters when SYN SEARCH is a low-level input voltage, V_{IL}. The Receiver Holding Register is "transparent" which allows the contents of the RECEIVER REGISTER to be monitored as it ripples through the shift register. When the external logic locates a "SYN" CHARACTER, indicated by a high-level input voltage, V_{OH}, on MDET, the SYN SEARCH line is externally raised to a high-level input voltage, V_{IH}. This high-level input voltage causes character synchronization to be initiated, returns the Receiver Holding Register to a "non-transparent" condition, causing subsequent characters to be transferred to the RECEIVER HOLDING REGISTER (when the center of the last bit of a character is recognized) and raises the DR FLAG.
30	MATCH DETECT FLAG	MDET	A high-level output voltage, V_{OH}, indicates that the contents of the Transmitter Register are identical to the contents of the Match-Character Holding Register. This flag is set to a high-level output voltage, V_{OH}, at the center of the first STOP ELEMENT of an asynchronous or isochronous character.
31	RECEIVER REGISTER CLOCK	RRC	This fifty (50) percent duty cycle clock provides the basic receiver timing. The negative transition from a high-level input voltage, V_{IH}, to a low-level input voltage, V_{IL}, shifts data into the RECEIVER REGISTER at a rate determined by RMS_1, RMS_2 and RMS_3. Synchronous operation requires that this negative transition occur at the center of each data bit.

PIN NUMBER	I/O NAME	SYMBOL	FUNCTION
32	MASTER RESET	MR	A high-level input voltage, V_{IH}, applied to this line resets timing and control logic to an idle state, sets the contents of the Receiver Holding Register to a high-level output voltage, V_{OH}, resets the contents of the Match-Character Holding Register, the MDET, DR, PE, FE, and OE outputs to a low-level output voltage, V_{OL}, but does not effect the contents of the control register.
33	CONTROL REGISTER LOAD	$\overline{CRL}$	A low-level input voltage, V_{IL}, applied to CD (pin 6) enables the $\overline{CRL}$ input. A low-level input voltage, V_{IL}, applied to this line enables inputs to DC "D Type" Latches of the Control Register and loads it with Control Bits (EPE, PI, RMS_1, RMS_2, RMS_3, WLS_1, WLS_2). A high-level input voltage, V_{IH}, applied to this line disables the Control Register. This line may be strobed or hard-wired to a low-level input voltage, V_{IL}. A high-level input voltage, V_{IH}, applied to CD disables CRL.
34	MATCH CHARACTER HOLDING REGISTER LOAD	$\overline{MHRL}$	A low-level input voltage, V_{IL}, applied to CD (pin 6) enables the $\overline{MHRL}$ input. A low-level input voltage, V_{IL}, applied to this line enables input to DC "D Type" Latches of the Match-Character Holding Register and loads it with the Match-Character Holding Register. This line may be strobed or hard-wired to a low-level input voltage, V_{IL}. A high-level input voltage, V_{IH}, applied to CD disables $\overline{MHRL}$.
35	RECEIVER INPUT	RI	The serial input data stream received on this line enters the Receiver Register determined by the character length, parity and the number of stop bits programmed. A high-level input voltage, V_{IH}, must be present when no ASYNCHRONOUS data is being received.

ORGANIZATION

PR1472 block diagram is illustrated on page 1.

Control Register — Programming of the PSAR is accomplished by loading the 7 Bit Control register. Mode selection, clock division, word length, and parity are selected when the Control Register Load (CRL) signal is activated.

Receiver Register — The Receiver Register is used to store the incoming data stream. The contents of this register can be gated to the Holding register during the transparent mode, or compared with the Match Holding Register. When a character is assembled it is transferred to the Receiver Holding Register.

Receiver Holding Register — The Receiver Holding Register, a buffer register, is used to store the assembled character.

Match Holding Register — The Match Holding Register is used to store the match character. The contents of this register are compared with the receiver register to establish character synchronization.

Timing & Control — The Timing and Control Logic generates the required control signals to assemble characters, match comparison, bit stripping, and generation of status/flag signals.

SYNCHRONOUS MODE OPERATION

Synchronous data appears as a continuous bit stream of contiguous characters at the input to the receiver with no Start or Stop bits. Character synchronization (the "framing" of this continuous bit stream into characters of a predetermined fixed length), must be accomplished by a comparison of this bit stream and a synchronization sequence. The P/SAR is designed to accommodate internal or external character synchronization by program control.

Referring to the Block Diagram of the Receiver, the Chip Disable (CD) enables or disconnects various in-

puts and outputs of the P/SAR. This feature provides the device with the capability of being disconnected from the system bus. The inputs to the Control Register and Match-Character Holding Register and their respective load strobes, $\overline{CRL}$ and $\overline{MHRL}$ are under CD control. In addition, DRR, SFR, PE, and OE and the outputs of the Receiver Holding Register, are also controlled by CD. It is necessary that CD enable these lines to allow strobing information in these registers and to allow examination of these output flags and data.

Device operation is programmed subsequent to being forced into its "idle" state. The P/SAR will enter a defined "idle" state when the Master Reset (MR) line is strobed to a high-level input voltage. In this state, all timing and control logic are reset, the contents of the Receiver Holding Register is set to a high-level output voltage and all output flags are reset to a low-level output voltage. The Master Reset also causes the contents of the Match-Character Holding Register to be reset to a low-level output voltage.

Enabled by CD, the Control Register is loaded by strobing $\overline{CRL}$ to a low-level input voltage which defines mode of operation and clock rate selection, character length and selected parity if required. Table 1 illustrates all programmable synchronous formats.

Character synchronization from the data stream requires Receiver recognition of specific bit pattern(s) which define the relative position of synchronous characters in the data stream and subsequent character assembly. The P/SAR programmably accommodates internal or external character synchronization.

Programmed for internal character synchronization, a high-level input voltage on the Sync Search line, the Receiver Holding Register is "transparent" and its contents are identical to the Receiver Holding Register. The data stream, gated into the Receiver Input (RI) by the negative transition of the Receiver Register Clock (RRC), shifts through the Receiver Register and is compared with the preprogrammed character in the Match-Character Holding Register. A match, indicated by a high-level output voltage on Match Detect (MDET), returns the Receiver Holding register to its non-transparent state and initializes timing and control logic but does not set the Data Received Flag to a high-level output voltage. The character following the match will be transferred to the Receiver Holding Register at the receipt of the center of its last bit and the Data Received Flag is set to a high-level output voltage. Depending on line discipline, this last character may also be a synchronizing character, in which case, Match Detect will continue to be a high-level output voltage when the Data Received Flag is set. Therefore, sequence verification can be performed by the system (additional hardware or software as desired).

Parity, if programmed, is verified upon receipt of the center of the parity bit which is the last bit of a synchronous character. If a parity error exists, the associated PE register is set to a high-level output voltage.

Transfer of a character to the Receiver Holding Register sets the associated Data Received Register Flag (DR) to a high-level output voltage. The transfer of a character to the Receiver Holding Register, if the Data Received Register Flag had already been set to a high-level output voltage, causes the previous character to be lost (written over) and is alerted by an Overrun Error Flag which is a high-level output voltage. In normal operation, the Data Received Flag is reset by $\overline{DRR}$ when the Receiver Holding Register is serviced (unloaded). The Status Flags, PE and OE, are also provided with an external reset $\overline{SFR}$ so that block status and character status may be (accumulated) verified. A low-level input voltage on Sync Search causes character synchronization to be lost and initiates transparency of the Receiver Holding Register.

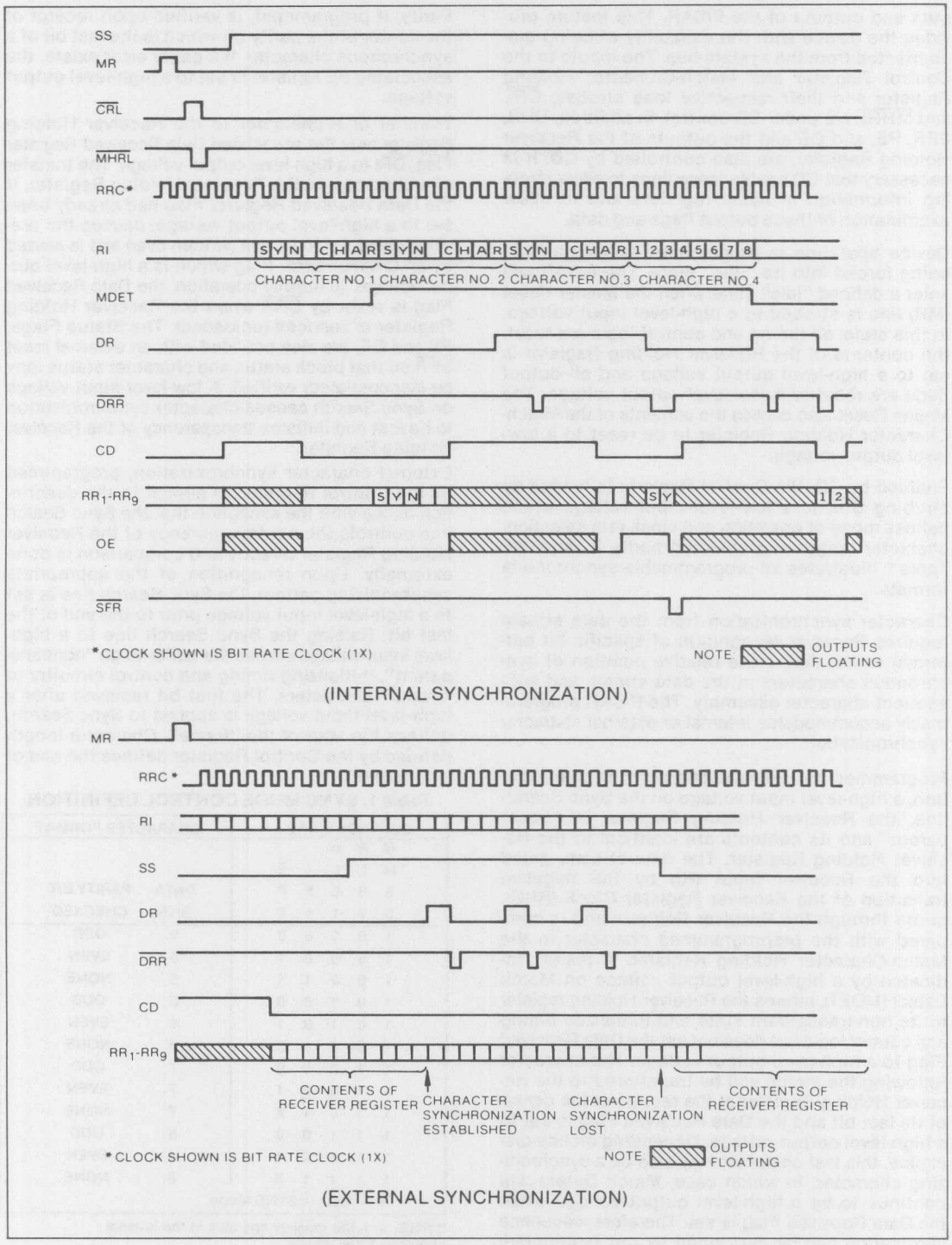
External character synchronization, programmed by the Control Register, is similar to the description above with the exception that the Sync Search line controls the nontransparency of the Receiver Holding Register directly and comparison is done externally. Upon recognition of the appropriate synchronizing pattern, the Sync Search line is set to a high-level input voltage prior to the end of the last bit. Raising the Sync Search line to a high-level input voltage causes the buffer to go "nontransparent", initializing timing and control circuitry to "frame" characters. The first bit received after a high-level input voltage is applied to Sync Search, defines the start of the "frame". Character length defined by the Control Register defines the end of the "frame".

Table 1. SYNC MODE CONTROL DEFINITION

CONTROL WORD						CHARACTER FORMAT	
	R M S 3	W L S 2	W L S 1	P I	E P E	DATA BITS	PARITY BIT CHECKED
	1	0	0	0	0	5	ODD
	1	0	0	0	1	5	EVEN
	1	0	0	1	X	5	NONE
	1	0	1	0	0	6	ODD
	1	0	1	0	1	6	EVEN
	1	0	1	1	X	6	NONE
	1	1	0	0	0	7	ODD
	1	1	0	0	1	7	EVEN
	1	1	0	1	X	7	NONE
	1	1	1	0	0	8	ODD
	1	1	1	0	1	8	EVEN
	1	1	1	1	X	8	NONE
↑ Sets to SYNC Mode							

If RMS_1 = 1, the receiver operates in the internal character SYNC mode.

If RMS_1 = 0, character SYNC must be externally provided.



SYNCHRONOUS TIMING DETAIL

ASYCHRONOUS & ISOCHRONOUS MODE

The completed assembly of a parallel character, by the P/SAR, from a serial data stream and buffered by its Receiver Holding Register is indicated by the status of the Data Received (DR) Flag. The assembly of character from a serial data stream consisting of a start bit, data, parity (if programmed), and a stop interval is initiated by the Start bit transition.

Verification of parity and receipt of a valid stop bit is accomplished prior to the character transfer to the Receiver Holding Register. Simultaneously, this data is compared with a preprogrammed character in the Match-Character Holding Register.

Status Flags, Data Received, Parity Error, Framing Error, Overrun Error and Match Detect are loaded into status registers during character transfer to the Receiver Holding Register.

Referring to the Block Diagram of the Receiver, the Chip Disable enables or disconnects various inputs and outputs of the P/SAR. This feature provides the device with the capability of being disconnected from the system bus. The inputs to the Control Register and Match-Character Holding Register and their respective load strobes, $\overline{CRL}$ and $\overline{MHRL}$ are under CD control. In addition, $\overline{DRR}$, $\overline{SFR}$, PE, FE, OE and the outputs of the Receiver Holding Register are also controlled by CD. It is necessary that CD enable these lines to allow strobing information into these registers and to allow examination of these output data and flags.

Device operation is programmed subsequent to being forced into its "idle" state. The P/SAR will enter a defined "idle" state when the Master Reset (MR) line is strobed to a high-level input voltage. In this state, all timing and control logic are reset, the contents of the Receiver Holding Register is set to a high-level output voltage, and all output flags are reset to a low-level output voltage. The Master Reset also causes the contents of the Match-Character Holding Register to be reset to a low-level output voltage.

When the Receiver is enabled by CD, loading the Control Register by strobing the Control Register Load ($\overline{CRL}$) line to a low-level input voltage defines the mode of operation and clock rate selection, character length and selected parity if required. Table 2 illustrates all the programmable asynchronous formats.

A mark to space transition on the receiver input initializes the clock counter causing it to count to the theoretical center of the start bit. At this time, the input is sampled. A high-level input voltage at the Receiver Input causes the first mark to space transition to be interpreted as a noise spike and resets all timing and control logic. This provides one-half data bit noise immunity on all clock selection rates except 1X. A low-level input voltage at the Receiver Input at the theoretical center of the start bit causes timing and control circuitry to sample the theoretical center of succeeding data bits. This data is shifted through the Receiver Register. When an entire character (as defined by the Control Register) is assembled in the Receiver Register, the line is "tested" for a valid stop bit at its theoretical center. This character is also compared with the contents of the Match-Character Holding Register at the center of the stop bit and its parity is verified. A parallel transfer occurs, loading the contents of the Receiver Register (less start and stop bits) into the Receiver Holding Register. The status of the parity verification, framing error, and overrun error circuitry are also loaded into their approriate registers to provide output error flags when the Data Received Flag is set. If the Data Received Flag had not been reset prior to the assembly of the current character, the previous character is lost and this is indicated by a high-level output voltage on the Overrun Error Flag.

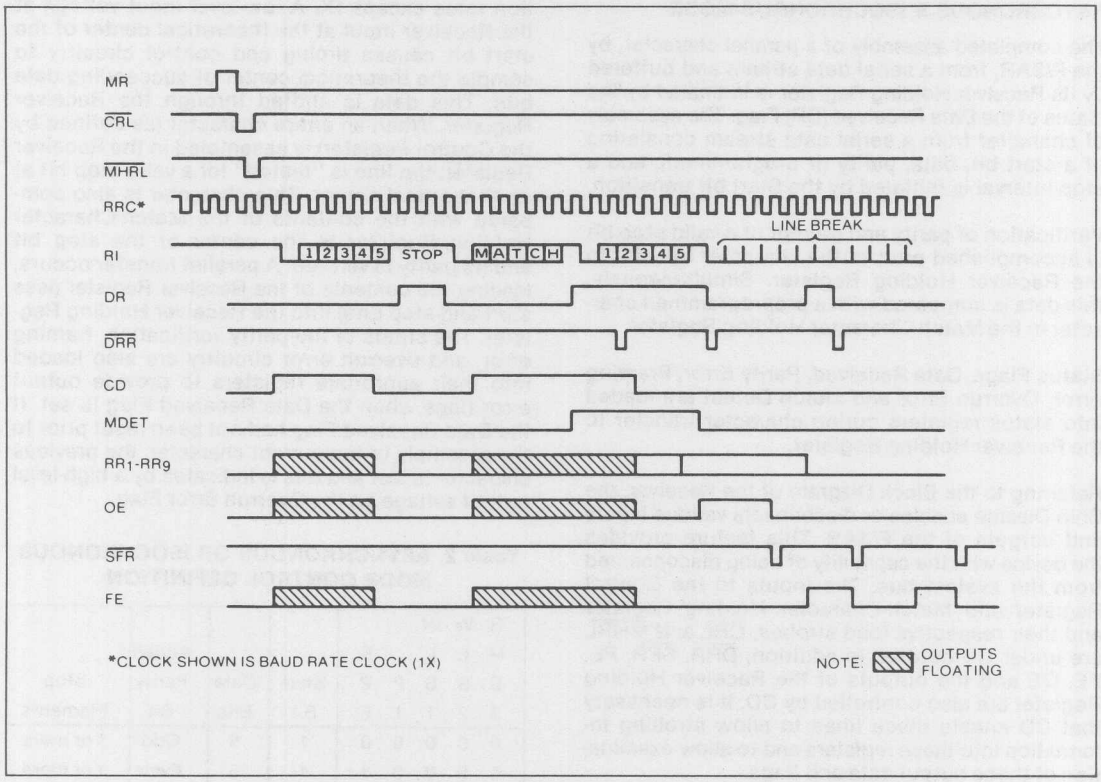
Table 2. ASYNCHRONOUS OR ISOCHRONOUS MODE CONTROL DEFINITION

RMS3	WLS2	WLS1	PI	EPE	Start Bit	Data Bits	Added Parity Bit	Stop Elements
0	0	0	0	0	1	5	Odd	1 or more
0	0	0	0	1	1	5	Even	1 or more
0	0	0	1	X	1	5	None	1 or more
0	0	1	0	0	1	6	Odd	1 or more
0	0	1	0	1	1	6	Even	1 or more
0	0	1	1	X	1	6	None	1 or more
0	1	0	0	0	1	7	Odd	1 or more
0	1	0	0	1	1	7	Even	1 or more
0	1	0	1	X	1	7	None	1 or more
0	1	1	0	0	1	8	Odd	1 or more
0	1	1	0	1	1	8	Even	1 or more
0	1	1	1	X	1	8	None	1 or more

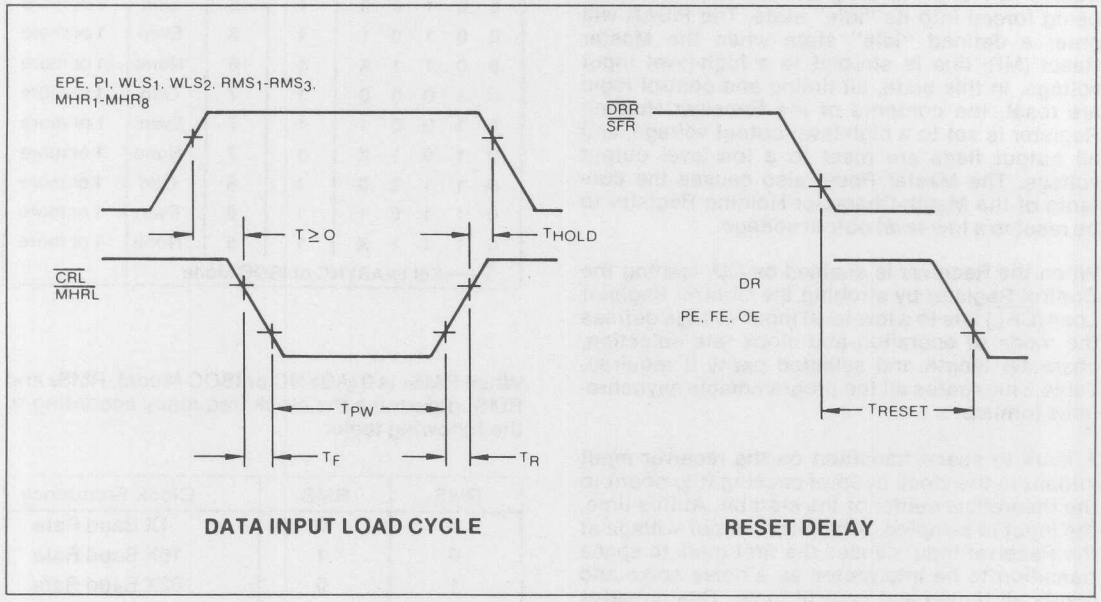
↑ Set to ASYNC or ISOC Mode

When RMS_3 is 0 (ASYNC or ISOC Mode), RMS_2 and RMS_3 determine the clock frequency according to the following table:

RMS_2	RMS_1	Clock Frequency
0	0	1X Baud Rate
0	1	16X Baud Rate
1	0	32X Baud Rate
1	1	64X Baud Rate

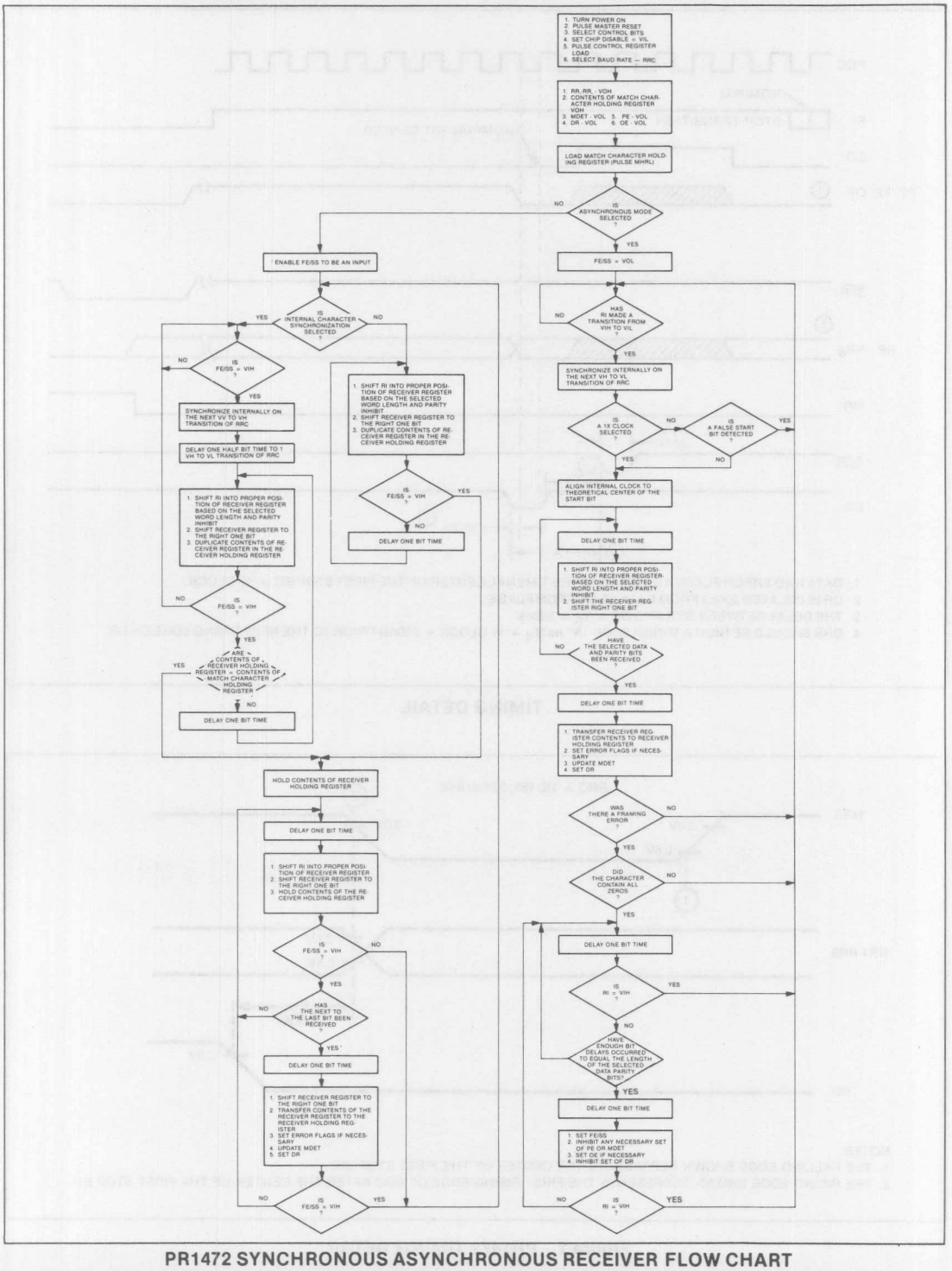


ASYNCHRONOUS & ISOCHRONOUS TIMING EXAMPLE

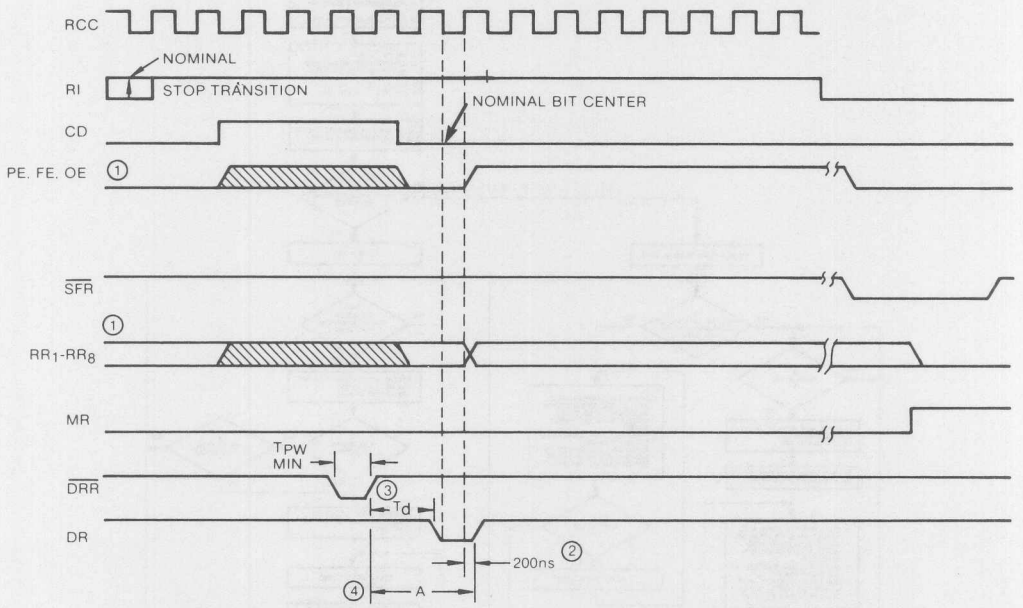


DATA INPUT LOAD CYCLE **RESET DELAY**

SWITCHING WAVEFORMS

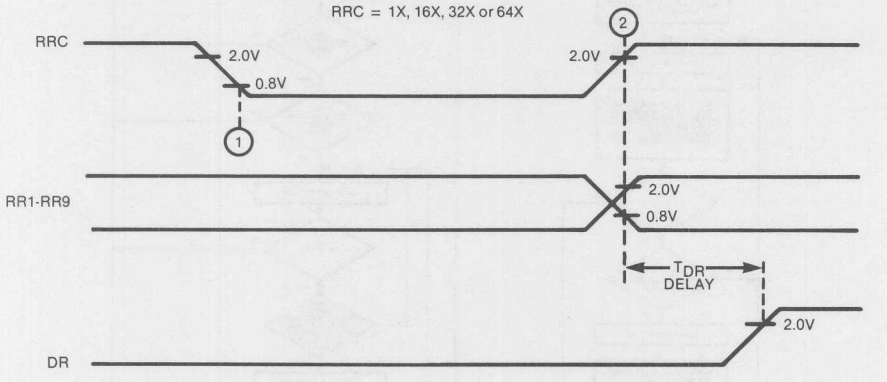


PR1472 SYNCHRONOUS ASYNCHRONOUS RECEIVER FLOW CHART



1. DATA AND ERROR FLAGS ARE VALID AT THE TIMENAL CENTER OF THE FIRST STOP BIT + ½ CLOCK.
2. DR IS DELAYED 200ns FROM DATA AND ERROR FLAGS
3. THE DELAY BETWEEN DRR AND DR = T_d = 500ns
4. DRR SHOULD BE HIGH A MINIMUM OF "A" ns (T_d + ½ CLOCK + 200ns) PRIOR TO THE NEXT RISING EDGE OF DR.

TIMING DETAIL



NOTES:
1. THE FALLING EDGE SHOWN REPRESENTS THE CENTER OF THE FIRST STOP BIT.
2. THE RISING EDGE SHOWN REPRESENTS THE FIRST RISING EDGE OF RRC AFTER THE CENTER OF THE FIRST STOP BIT.

Figure 1 PR1472 TIMING DETAIL

MAXIMUM RATINGS

V_{GG} Supply Voltage		+0.3V to −20V
V_{DD} Supply Voltage		+0.3V to −20V
Clock Input Voltage*		+0.3V to −20V
Logic Input Voltage*		+0.3V to −20V
Logic Output Voltage*		+0.3V to −20V
Storage Temperature	Ceramic	−65°C to +150°C
	Plastic	−55°C to +125°C
Operating Free-Air Temperature T_A Range		0°C to +50°C
Lead Temperature (Soldering, 10 sec)		300°C

*$V_{GG} = V_{DD} = 0V$

NOTE: These voltages are measured with respect to V_{SS} (Substrate).

ELECTRICAL CHARACTERISTICS

($V_{SS} = V_{CC} = 5V \pm 5\%$, $V_{DD} = 0V$, $V_{GG} = -12V \pm 5\%$, $T_A = 0°C$ to $+50°C$ unless otherwise specified.)

SYMBOL	PARAMETER	MIN.	MAX.	CONDITIONS
	INPUT LOGIC LEVELS[1]			
V_{IL}	Low-level Input Voltage		0.8V	$V_{SS} = 4.75V$
V_{IH}	High-level Input Voltage	V_{SS}-1.5V		
	OUTPUT LOGIC LEVELS[2]			
V_{OL}	Low-level Output Voltage		0.5V	$V_{SS} = 5.25V$ $I_{OL} = 1.6mA$
V_{OH}	High-level Output Voltage	V_{SS}-1.0V		$V_{SS} = 4.75V$ $I_{OH} = -100\mu A$
	INPUT CURRENT[1]			
I_{IL}	Low-level Input Current (each input)		−1.6mA	$V_{SS} = 5.25V$ $V_{IN} = 0.4V$
I_{LO}	Output Leakage Current		10μA	

NOTE: 1) Inputs under Chip Disable control when disabled, (V_{IH} applied to CD), are logically disabled and appear as a single TTL Load.

2) Outputs under Chip Disable control when disabled (V_{IH} applied to CD), are logically and electrically disconnected and caused to float. The Three-State Output has three stages; (1) Low impedance to V_{CC} (2) Low impedance to GND (3) High impedance OFF ≃ 10 Megohm.

SWITCHING CHARACTERISTICS

(V_{SS}-$V_{CC} = 5V$, $V_{DD} = 0V$, $V_{GG} = -12V$, $T_A = 25°C$, $C_L = 20$ pf)

SYMBOL	PARAMETER	MIN.	MAX.	CONDITIONS
F_C	Clock Frequency	DC	100 KHz	PR1472-00
		DC	640 KHz	PR1472-01
	PULSE WIDTH			
T_{HOLD}	Hold Time	20 nsec		
T_{CRL}	Control Register Load	250 nsec		
T_{MHRL}	Match-Character Holding Register Load	250 nsec		
T_{DRR}	Data Received Reset	200 nsec		
T_{SFR}	Status Flag Reset	200 nsec		
T_{MR}	Master Reset	500 nsec		
T_{PD}	Output Enable Delay		500 nsec	
T_R	Rise Time		150 nsec	
T_F	Fall Time		150 nsec	
$T_{DR\ DELAY}$	Data Ready Delay Time		200 nsec	

See page 429 for ordering information.

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WESTERN DIGITAL
CORPORATION

PT1482 (PSAT)
Programmable Synchronous & Asynchronous Transmitter

FEATURES

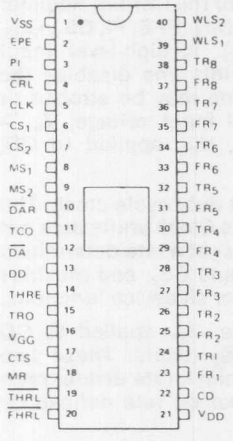
- SYNCHRONOUS, ASYNCHRONOUS OR ISOCHRONOUS OPERATION
- DC TO 640K BITS/SEC, 1X CLOCK PT1482-01
- DC TO 100K BITS/SEC, 1X CLOCK PT1482-00
- PROGRAMMABLE MATCH (FILL) CHARACTER
- SELECTABLE 5,6,7, OR 8 BIT PER CHARACTER
- EVEN/ODD PARITY GENERATOR. PARITY INHIBIT
- PROGRAMMABLE CLOCK RATE 1X, 16X, 32X, OR 64X.
- AUTOMATIC START & STOP BIT GENERATION IN ASYNCHRONOUS & ISOCHRONOUS MODES
- PROGRAMMABLE 1 AND 2 STOP BITS, (1½ IN 5 LEVEL MODE)
- AUTOMATIC CHARACTER STATUS AND DELIMITING SIGNAL GENERATION
- THREE STATE OUTPUTS — BUS STRUCTURE COMPATIBILITY
- DOUBLE BUFFERED
- TTL AND DTL COMPATIBLE — INTERNAL ACTIVE PULL UP
- COMPATIBLE RECEIVER, PR1472.

GENERAL DESCRIPTION

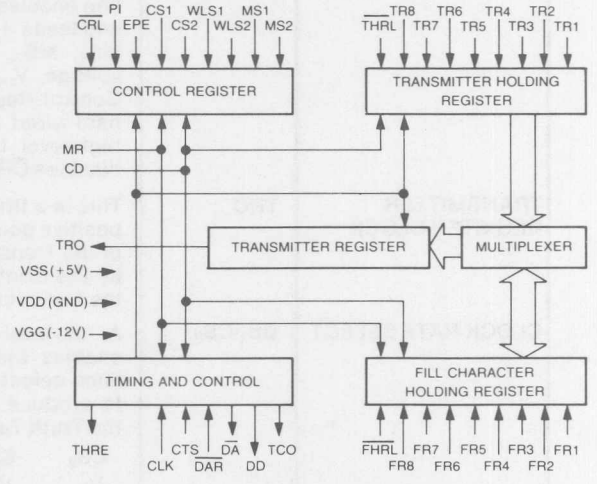
The Western Digital PT1482 (PSAT) is a programmable transmitter that interfaces variable length parallel data to a serial data channel. The transmitter converts parallel characters into a serial data stream with a format compatible with all standard Synchronous, Asynchronous or Isoschronous data communications media.

Contiguous serial characters are transmitted in the Synchronous Mode with the automatic insertion of a programmable Fill (Idle) Character during the absence of parallel input data. Programming the Asynchronous Mode selects serial transmission with automatic insertion of Start and Stop Bits. Isoschronous mode selects transmission with automatic fill character insertion during the absence of parallel input data. Four internal registers and a multiplexer, in conjunction with Three-State Output Lines, provide full system versatility.

The PSAT is a TTL compatible device. The use of internal active pull-up devices and push-pull output drivers, provides direct compatibility with all forms of current sinking logic. Western Digital also offers a compatible Receiver, PR1472.



PIN CONNECTIONS



PT1482 BLOCK DIAGRAM

PIN OUTS

PIN NUMBER	I/O NAME	SYMBOL	FUNCTION
1	V_{SS} POWER SUPPLY	V_{SS}	+ 5 Volt Supply
2	EVEN PARITY ENABLE	EPE	A low-level input voltage, V_{IL}, applied to CD (pin 22) enables the EPE and PI Inputs.
3	PARITY INHIBIT	PI	The Even Parity Enable Input and the Parity Inhibit Input to the Control Register, in conjunction with the Control Register Load and Chip Disable, select even, odd or no parity to be generated by the Transmitter. A high-level input voltage, V_{IH}, applied to EPE selects even parity and a low-level input voltage, V_{IL}, selects odd parity if a low-level input voltage is applied to Parity Inhibit and Chip Disable.
			PI / EPE / SELECTED PARITY / COMMENTS V_{IL} / V_{IL} / ODD / CD = V_{IL} V_{IL} / V_{IH} / EVEN / CD = V_{IL} V_{IH} / X / NONE / CD = V_{IL}
			NOTE: IF CD = V_{IH}, NO PROGRAMMING IS PERFORMED SINCE INPUTS ARE DISABLED.
			X – either V_{IL} or V_{IH} When programmed, the appropriate parity is generated following, and is contiguous with, the last data bit of a character, immediately preceding the stop element of asychronous and isochronous characters.
			A high-level input voltage, V_{IH}, applied to CD disables EPE, PI, and $\overline{CRL}$.
4	$\overline{CONTROL\ REGISTER\ LOAD}$	$\overline{CRL}$	A low-level input voltage, V_{IL}, applied to CD (pin 22) enables the $\overline{CRL}$ input.
			A low-level input voltage, V_{IL}, applied to this line enables DC Latches of the Control Register and loads it with Control Bits (EPE, PI, CS_1, CS_2, MS_1, MS_2, WLS_1, WLS_2). A high-level input voltage, V_{IH}, applied to this line disables the Control Register. This line may be strobed or hard-wired to a low-level input voltage, V_{IL}. A high-level input voltage, V_{IH}, applied to CD, disables $\overline{CRL}$.
5	TRANSMITTER REGISTER CLOCK	TRC	This is a fifty (50) percent duty cycle clock. The positive going edge of this Clock shifts data out of the Transmitter Register at a rate determined by the Control Bits CS_1 and CS_2, and provides the basic time reference for all device functions.
6-7	CLOCK RATE SELECT	CS_1-CS_2	A low-level input voltage, V_{IL}, applied to CD enables the CS_1 and CS_2 inputs. These two lines select the internal clock rate divider ratio to produce the transmitter bit rate defined by the Truth Table below:
			CS_2 / CS_1 / SELECTED CLOCK INPUT RATE V_{IL} / V_{IL} / 1X BIT RATE V_{IL} / V_{IH} / 16X BIT RATE V_{IH} / V_{IL} / 32X BIT RATE V_{IH} / V_{IH} / 64X BIT RATE

PIN NUMBER	I/O NAME	SYMBOL	FUNCTION
			A high-level input voltage, V_{IH}, applied to CD disables CS_1 and CS_2.
8-9	MODE SELECT	MS_1-MS_2	These lines may be strobed or hard-wired to the appropriate input voltage. A low-level input voltage, V_{IL}, applied to CD (pin 22) enables the MS_1 and MS_2 inputs. These lines select the transmitter operating mode. **MS_2 MS_1 MODE** V_{IL} V_{IL} ASYNCHRONOUS — ONE STOP BIT V_{IL}* V_{IH}*ASYNCHRONOUS — TWO STOP BITS V_{IH} V_{IL} SYNCHRONOUS V_{IH} V_{IH} ISOCHRONOUS *Selects 1.5 stop bits for 5-level codes. A high-level input voltage, V_{IH}, applied to CD disables MS_1 and MS_2.
10	$\overline{\text{DATA NOT AVAILABLE}}$ RESET	$\overline{\text{DAR}}$	A low-level input voltage, V_{IL}, applied to CD (pin 22) enables the $\overline{\text{DAR}}$ input. A low-level input voltage, V_{IL}, applied to this line resets the Data Not Available Flag. A high-level Input, V_{IH}, applied to CD disables $\overline{\text{DAR}}$. This input is not used during asynchronous operation.
11	TRANSMITTER CLOCK OUTPUT	TCO	This output is a clock at the transmitted bit rate. The negative going edge of this clock corresponds to the center of each transmitted data bit. The positive going edge corresponds to the start of each data bit transmission. All waveforms in this specification are referenced to TCO.
12	$\overline{\text{DATA NOT AVAILABLE}}$ FLAG	$\overline{\text{DA}}$	A low-level input voltage, V_{IL}, applied to CD (pin 22) enables the $\overline{\text{DA}}$ input. A high-level output voltage, V_{OH}, on this line indicates that a Fill-Character has been transmitted, since a character was not loaded into the Transmitter Holding Register by the center of the last bit of a Synchronous Character or the center of the Stop Element of an Isochronous character. A high-level input voltage, V_{IH}, applied to CD disables $\overline{\text{DA}}$. This input is not used during asynchronous operation.
13	DATA DELIMIT/ END OF CHARACTER	DD/EOC	During asynchronous operation, a high-level output voltage, V_{OH}, indicates data is being transmitted. A low-level output voltage, V_{OL}, indicates that a Start or Stop Element is being transmitted. A low-level output voltage during synchronous operation indicates that the last bit of a character is being transmitted.

PIN NUMBER	I/O NAME	SYMBOL	FUNCTION
14	TRANSMITTER HOLDING REGISTER EMPTY	THRE	A low-level input voltage applied to CD (pin 22) enables the THRE input. A high-level output voltage, V_{OH}, on this line indicates the Transmitter Holding Register is empty and has transferred its contents to the Transmitter Register and may be loaded with a new character. This line goes to a low-level output voltage, V_{OL}, when THRL goes to a low-level input voltage, V_{IL}. A high-level input voltage, V_{IH}, applied to CD disables THRE.
15	TRANSMITTER REGISTER OUTPUT	TRO	The contents of the Transmitter Holding Register are serially shifted out as an NRZ waveform on this line provided that a character was loaded into the Transmitter Holding Register prior to $\overline{DA}$ Flag (in Synchronous or Isochronous Modes). If a character was not loaded prior to a $\overline{DA}$ Flag, the contents of the Fill-Character Register are transmitted as the next character.
16	V_{GG} POWER SUPPLY	V_{GG}	– 12 Volts Supply.
17	CLEAR-TO-SEND	CTS	The Clear-To-Send Control initiates or disables transmission as a function of the state of this line. A high-level input voltage, V_{IH}, initiates serial data transmission provided a character has been loaded into the Transmitter Holding Register. A low-level input voltage, V_{IL}, applied to this line during transmission allows completion of that character only, after which the output will continue to mark until a high-level input voltage is applied.
18	MASTER RESET	MR	The rising edge of a high-level input voltage, V_{IH}, applied to this line resets timing and control logic to an idle state, sets THRE, the contents of the Fill-Character Holding Register, and TRO to a high-level output voltage, V_{OH}.
19	$\overline{\text{TRANSMITTER HOLDING REGISTER LOAD}}$	$\overline{THRL}$	A low-level input voltage, V_{IL}, applied to CD (pin 22) enables the $\overline{THRL}$ input. A low-level input voltage, V_{IL}, applied to this line enables DC Latches of the Transmitter Holding Register and loads it with the Transmitter Holding Register data and forces THRE to a low-level output voltage, V_{OL}. A high-level input voltage, V_{IH}, applied to this line disables the Transmitter Holding Register. A high-level input voltage, V_{IH}, applied to CD disables $\overline{THRL}$.
20	$\overline{\text{FILL-CHARACTER HOLDING REGISTER LOAD}}$	$\overline{FHRL}$	A low-level input voltage, V_{IL}, applied to CD (pin 22) enables the $\overline{FHRL}$ input. A low-level input voltage, V_{IL}, applied to this line enables DC Latches of the Fill-Character Holding Register and loads it with the Fill-Character Register data FR_1-FR_8. A high-level input voltage, V_{IH}, applied to this line disables the $\overline{FHRL}$ Register. This line may be strobed or hard-wired to a low-

PIN NUMBER	I/O NAME	SYMBOL	FUNCTION
			level input voltage, V_{IL}. This input is not used during asynchronous operation. A high-level input voltage, V_{IH}, applied to CD disables $\overline{FHRL}$.
21	V_{DD} POWER SUPPLY	V_{DD}	Ground.
22	CHIP DISABLE	CD	This line controls the disconnect associated with busable inputs and Three-State outputs. A high-level input voltage, V_{IH}, applied to this line removes drive from push-pull outputs causing them to float. Drivers of disabled inputs are required to sink or source current. The I/O Lines controlled by Chip Disable are defined below: **INPUT LINES** / **TRI-STATE OUTPUT LINES** $\overline{CRL}$, $\overline{THRL}$, $\overline{DA}$ EPE, $\overline{FHRL}$, THRE PI, FR_1-FR_8 CS_1-CS_2, TR_1-TR_8 $\overline{MS_1}$-MS_2, WLS_1, WLS_2 $\overline{DAR}$
23, 25 27, 29 31, 33 35, 37	FILL-CHARACTER HOLDING REGISTER DATA INPUTS	FR_1-FR_8	A low-level input voltage, V_{IL}, applied to CD (pin 22) enables the inputs of the Fill-Character Holding Register and associated Load Strobe, $\overline{FHRL}$. Parallel 8-bit characters are input into the Fill-Character Holding Register with the $\overline{FHRL}$ Strobe (pin 20). If a character of less than 8 bits has been selected (by WLS_1 and WLS_2) only the least significant bits are accepted. These lines may be strobed or hard-wired to the appropriate input voltage. These inputs are not used during asynchronous operation. During Synchronous or Isochronous transmission, the Fill-Character is transmitted if a character was not loaded into the Transmitter Holding Register prior to a $\overline{DA}$ Flag; i.e., the Transmitter Holding Register did not contain a character at the center of the last bit being transmitted from the Transmitter Register. A high-level input voltage, V_{IH}, will cause a high-level output voltage, V_{OH}, to be transmitted, Least Significant Bit (FR_1) to Most Significant Bit (FR_n) order. A high-level input voltage, V_{IH}, applied to CD disables FR_1-FR_8.
24, 26 28, 30 32, 34 36, 38	TRANSMITTER HOLDING REGISTER DATA INPUTS	TR_1-TR_8	A low-level input voltage, V_{IL}, applied to CD (pin 22) enables the inputs to the Transmitter Holding Register and associated Load Strobe, $\overline{THRL}$. If a character of less than 8 bits has been selected (by WLS_1 and WLS_2), only the least significant bits are accepted. A high-level input

PIN NUMBER	I/O NAME	SYMBOL	FUNCTION
39-40	WORD LENGTH	WLS_1-WLS_2	voltage, V_{IH}, will cause a high-level output voltage to be transmitted, Least Significant Bit (TR_1) to Most Significant Bit (TR_n) order. A high-level input voltage, V_{IH}, applied to CD disables TR_1-TR_8. A low-level input voltage, V_{IL}, applied to CD (pin 22) enables the inputs of the Control Register and Load, $\overline{CRL}$. Parallel 8-bit characters are input into the Control Register with the $\overline{CRL}$ Strobe (pin 4), WLS_1 and WLS_2 select the transmitted character length from five (5) to eight (8) bits defined by the Truth Table below: WLS_2 / WLS_1 / SELECTED WORD LENGTH V_{IL} / V_{IL} / 5 BITS V_{IL} / V_{IH} / 6 BITS V_{IH} / V_{IL} / 7 BITS V_{IH} / V_{IH} / 8 BITS A high-level input voltage, V_{IH}, applied to CD disables WLS_1 and WLS_2, forcing them to float.

ORGANIZATION

PT1482 block diagram is illustrated on page 1.

Control Register — Programming of the PSAT is accomplished by loading the 8 Bit Control Register. Mode selection, clock divisor, word length, and parity are selected when the Control Register Load signal is activated.

Transmitter Register — The Transmitter Register is used to store the outgoing data stream. The contents of this register are derived from either the Transmitter Holding Register or the Fill (Match) Character Holding Register with the Control and Timing Logic automatically adding the required start and stop bits during Asynchronous and Isoschronous Modes.

Transmitter Holding Register — The Transmitter Holding Register, a buffer register, is used to store the parallel character to be serially transmitted.

Fill Character Holding Register — The Fill Character Holding Register is used to store the Fill (Match) Character which is transmitted during the absence of characters in the Transmitter Holding Register.

Timing and Control — The Timing and Control Logic generates the required control signals to transmit Data and Fill Characters. Character transmission status signals are also derived from this logic.

SYNCHRONOUS MODE OPERATION

Synchronous transmission requires that characters (programmably variable from 5 to 8 data bits plus parity) are contiguous with no start or stop bits. Since the requirement that characters are contiuous does not imply that the system servicing the transmitter always has ample time to load the Transmitter Holding Register, it is necessary that a character be transmitted when data has not been loaded into the Transmitter Holding Register. This character is defined as the Fill or Idle Character and a separate register has been provided to load this character upon initialization. The Fill-Character Holding Register is loaded by strobing the Fill-Character Holding Register Load ($\overline{FHRL}$) line or hard-wiring it to a low-level input voltage.

Referring the Block Diagram of the Transmitter, it can be seen that the Chip Disable (CD) enables or disconnects various inputs and outputs of the P/SAT. The inputs to the Control Register, Transmitter Holding Register, Fill-Character Holding Register and their respective load strobes, $\overline{CRL}$, $\overline{THRL}$, and $\overline{FHRL}$ are under CD control. In addition, the Transmitter Holding Register Empty (THRE) Flag, Data Not Available ($\overline{DA}$) Flag, and the Data Not Available Reset ($\overline{DAR}$) are also controlled by CD. It is necessary that CD enable these lines to allow strobing information into these registers and to allow examination of these output flags. The P/SAT will enter a defined "idle" state when the Master Reset (MR) is strobed to a high-level input voltage. In this state, all timing and control logic are reset, the Transmitter Register Output continues to mark, the Transmitter Holding Register Flag is set to a high-level output voltage, the Data Delimit/End of Character (DD/EOC) Flag

is set to a low-level output voltage, and the contents of the Fill-Character Holding Register are forced to a high-level output voltage.

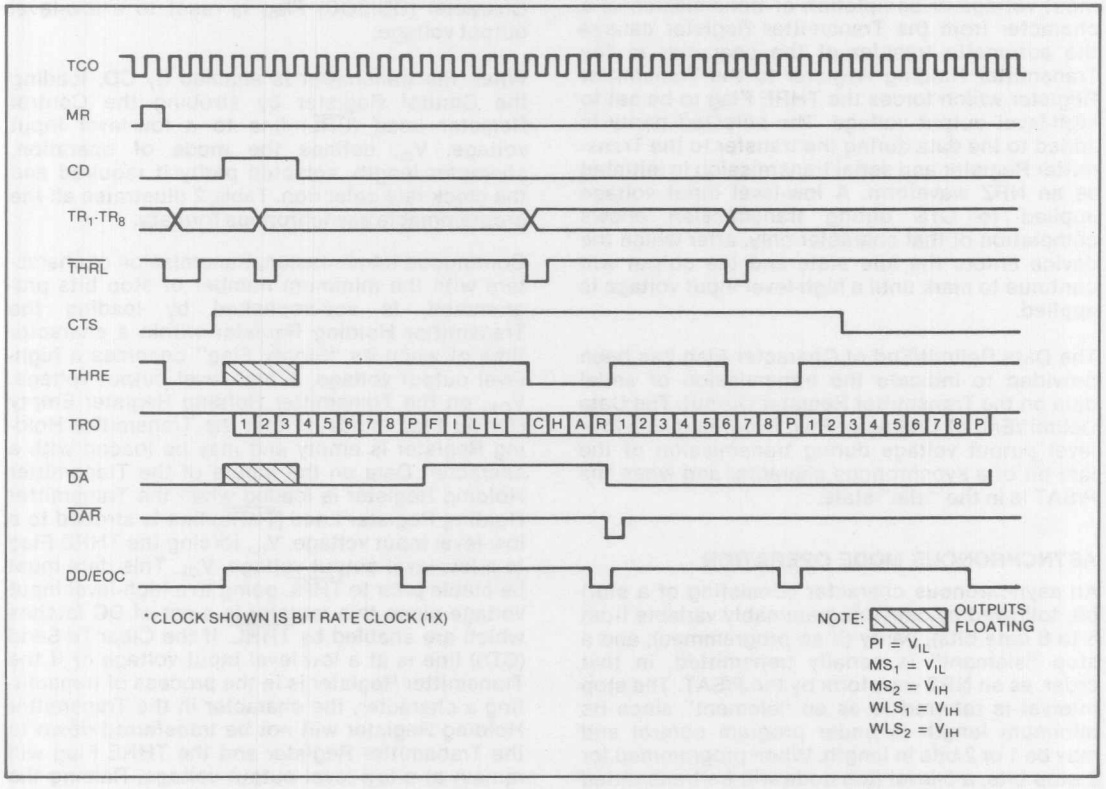
When the P/SAT is enabled by CD, loading the Control Register by strobing the Control Register Load ($\overline{CRL}$) line to a low-level input voltage, defines the mode of operation, character length, selected parity if required, and the clock rate selection. Table 1 illustrates all the programmable synchronous character formats.

To initialize transmission the CTS signal must be set to a high state and the transmitter holding register must be loaded with a character to be transmitted. The transmitter will remain in an idle state until this is accomplished.

The character transferred into the Transmitter Register (from the Transmitter Holding Register or the Fill-Character Holding Register) is determined at the center of the last bit of the character being transmitted. If, at this time, no character has been loaded into the Transmitter Holding Register, the Fill-Character is loaded into the Transmitter Register at the end of the bit being transmitted

Table 1. SYNC MODE CONTROL DEFINITION

CONTROL WORD						CHARACTER FORMAT	
MSS2	MSS1	WLS2	WLS1	PI	EPE	DATA BITS	ADDED PARITY BIT
1	0	0	0	0	0	5	ODD
1	0	0	0	0	1	5	EVEN
1	0	0	0	1	X	5	NONE
1	0	0	1	0	0	6	ODD
1	0	0	1	0	1	6	EVEN
1	0	0	1	1	X	6	NONE
1	0	1	0	0	0	7	ODD
1	0	1	0	0	1	7	EVEN
1	0	1	0	1	X	7	NONE
1	0	1	1	0	0	8	ODD
1	0	1	1	0	1	8	EVEN
1	0	1	1	1	X	8	NONE
↑ Sets to SYNC Mode							



SYNCHRONOUS TIMING EXAMPLE

and a Data Not Available ($\overline{DA}$) Flag is set to a high-level output voltage. This Fill-Character will be repeatedly transmitted until a character is loaded into the Transmitter Holding Register, at which time, the Data Not Available Flag is reset, the Fill-Character will be completed and the newly loaded synchronous character will follow contiguously.

A high-level output voltage, on the THRE Flag indicates that the Transmitter Holding Register is empty and may be loaded with a character. Data on the inputs of the Transmitter Holding Register is loaded when the Transmitter Holding Register Load ($\overline{THRL}$) line is strobed to a low-level input voltage, forcing the THRE Flag to a low-level output voltage. This data must be stable prior to $\overline{THRL}$ going to a high-level input voltage since this register is a set of DC latches which are enabled by $\overline{THRL}$.

If the Clear-To-Send (CTS) line is at a low-level input voltage, or if the Transmitter Register is in the process of transmitting a character, the character in the Transmitter Holding Register will not be transferred down to the Transmitter Register and the THRE Flag will remain at a low-level output voltage. Raising the CTS line to a high-level input voltage or completion of transmission of a character from the Transmitter Register causes the automatic transfer of the character in the Transmitter Holding Register to the Transmitter Register which forces the THRE Flag to be set to high-level output voltage. The selected parity is added to the data during the transfer to the Transmitter Register and serial transmission is initiated as an NRZ waveform. A low-level input voltage applied to CTS during transmission allows completion of that character only, after which the device enters the idle state and the output will continue to mark until a high-level input voltage is applied.

The Data Delimit/End of Character Flag has been provided to indicate the transmission of serial data on the Transmitter Register Output. The Data Delimit/End of Character Flag is defined as a low-level output voltage during transmission of the last bit of a synchronous character and when the P/SAT is in the "idle" state.

ASYNCHRONOUS MODE OPERATION

An asynchronous character consisting of a start bit, followed by data (programmably variable from 5 to 8 data bits), parity (if so programmed), and a stop "element" is serially transmitted, in that order, as an NRZ waveform by the P/SAT. The stop interval is referred to as an "element" since its minimum length is under program control and may be 1 or 2 bits in length. When programmed for 2 stop bits, a 5-level (bit) code will be transmitted with 1.5 stop bits.

Referring to the Block Diagram of the Transmitter, it can be seen that the Chip Disable enables or disconnects various inputs and outputs of the P/SAT. The inputs to the Control Register, Transmitter Holding Register, Fill-Character Holding Register and their respective load strobes, $\overline{CRL}$, $\overline{THRL}$ and $\overline{FHRL}$ are under CD control. In addition, the Transmitter Holding Register Empty Flag (THRE), the Data Not Available Flag ($\overline{DA}$), and the Data Not Available Reset ($\overline{DAR}$) are also controlled by CD. It is necessary that CD enable these lines to allow strobing information into these registers and to allow examination of these output flags. It should be noted that the Fill-Character Holding Register and its associated load strobe, $\overline{FHRL}$, the Data Not Available Flag and its associated reset, $\overline{DAR}$, play no role in asynchronous communications and are only mentioned here for completeness.

The P/SAT will enter a defined "idle" state when the Master Reset (MR) line is strobed to a high-level input voltage. In this state, all timing and control logic are reset, the Transmitter Register Output continues to mark, the Transmitter Holding Register Empty Flag is set to a high-level output voltage, V_{OH}, and the Data Delimit/End of Character (DD/EOC) Flag is reset to a low-level output voltage.

When the transmitter is enabled by CD, loading the Control Register by strobing the Control Register Load ($\overline{CRL}$) line to a low-level input voltage, V_{IL}, defines the mode of operation, character length, selected parity if required and the clock rate selection. Table 2 illustrates all the programmable asynchronous formats.

Continuous transmission, transmission of characters with the minimum number of stop bits programmed, is accomplished by loading the Transmitter Holding Register within a character time of when its "Empty Flag" becomes a high-level output voltage. A high-level output voltage, V_{OH}, on the Transmitter Holding Register Empty (THRE) Flag indicates that the Transmitter Holding Register is empty and may be loaded with a character. Data on the inputs of the Transmitter Holding Register is loaded when the Transmitter Holding Register Load ($\overline{THRL}$) line is strobed to a low-level input voltage, V_{IL}, forcing the THRE Flag to a low-level output voltage, V_{OL}. This data must be stable prior to $\overline{THRL}$ going to a high-level input voltage since this register is a set of DC latches which are enabled by $\overline{THRL}$. If the Clear-To-Send (CTS) line is at a low-level input voltage or if the Transmitter Register is in the process of transmitting a character, the character in the Transmitter Holding Register will not be transferred down to the Transmitter Register and the THRE Flag will remain at a low-level output voltage. Raising the CTS line to a high-level input voltage or comple-

tion of transmission of a character from the Transmitter Register causes the automatic transfer of the character in the Transmitter Holding Register to the Transmitter Register and the THRE flag will be set to a high-level output voltage.

The start bit, selected parity and stop bit(s), determined by the Control Register programming, are added to the data during the transfer to the Transmitter Register and serial transmission is initiated as an NRZ waveform.

A low-level input voltage, applied to CTS during transmission, allows completion of that character only, after which the output will continue to mark until a high-level input voltage is applied.

The Data Delimit/End of Character Flag has been provided to indicate the transmission of serial data on the Transmitter Register Output. Data Delimit is a low-level output voltage during start and stop bits and is a high-level output voltage during transmission of data and parity. Neither TRO, CTS nor DD/EOC is under control of Chip Disable.

ISOCHRONOUS MODE OPERATION

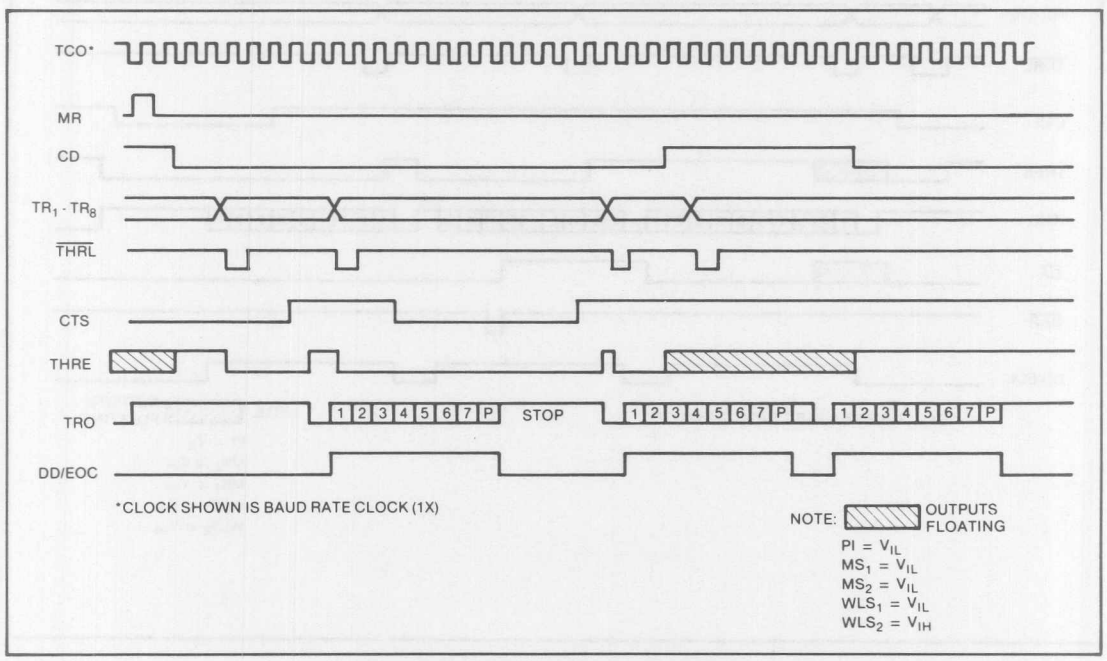
In the Isochronous Mode of operation all (Synchronous Mode) definitions apply with the exception of those for the Data Delimit/End of Character (DD/EOC) Flag and the Data Not Available Flag (DA).

This is the case since Isochronous Data Transmission requires contiguous characters with the addition of a start and a single stop bit added to each character.

Table 2. ASYNC MODE CONTROL DEFINITION

CONTROL WORD							CHARACTER FORMAT			
MSS2	MSS1	WLS2	WLS1	PI	EPE		START BIT	DATA BITS	ADDED PARITY BIT	STOP ELEMENTS
0	0	0	0	0	0		1	5	ODD	1
0	1	0	0	0	0		1	5	ODD	1.5
0	0	0	0	0	1		1	5	EVEN	1
0	1	0	0	0	1		1	5	EVEN	1.5
0	0	0	0	1	X		1	5	NONE	1
0	1	0	0	1	X		1	5	NONE	1.5
0	0	0	1	0	0		1	6	ODD	1
0	1	0	1	0	0		1	6	ODD	2
0	0	0	1	0	1		1	6	EVEN	1
0	1	0	1	0	1		1	6	EVEN	2
0	0	0	1	1	X		1	6	NONE	1
0	1	0	1	1	X		1	6	NONE	2
0	0	1	0	0	0		1	7	ODD	1
0	1	1	0	0	0		1	7	ODD	2
0	0	1	0	0	1		1	7	EVEN	1
0	1	1	0	0	1		1	7	EVEN	2
0	0	1	0	1	X		1	7	NONE	1
0	1	1	0	1	X		1	7	NONE	2
0	0	1	1	0	0		1	8	ODD	1
0	1	1	1	0	0		1	8	ODD	2
0	0	1	1	0	1		1	8	EVEN	1
0	1	1	1	0	1		1	8	EVEN	2
0	0	1	1	1	X		1	8	NONE	1
0	1	1	1	1	X		1	8	NONE	2

▲ Sets to ASYNC Mode



ASYNCHRONOUS TIMING EXAMPLE

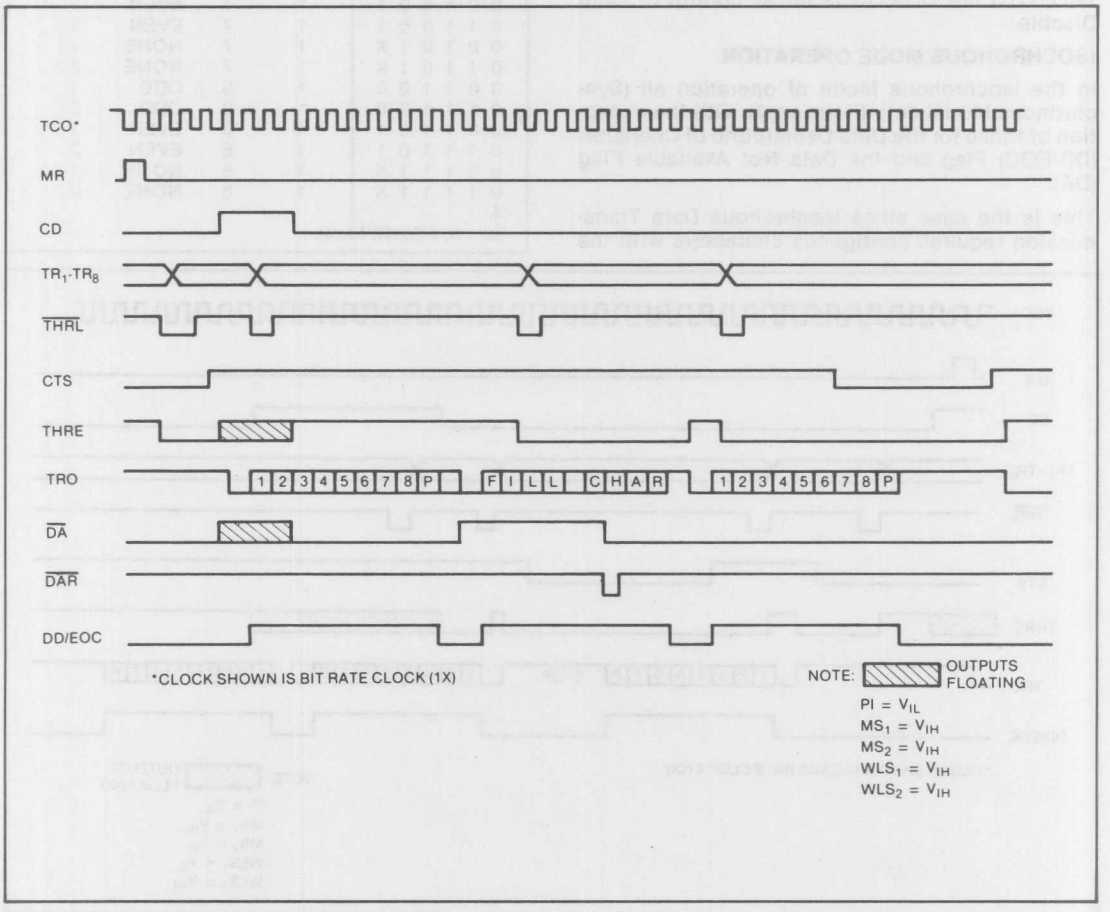
The Data Delimit/End of Character Flag is a low-level output voltage during start and stop bits and is a high-level output voltage during transmission of data and parity. The Data Not Available Flag ($\overline{DA}$) is set to a high-level output voltage at the end of the stop bit if a character has not been loaded into the Transmitter Holding Register at the center of the stop bit. The contents of the Fill-Character Holding Register will be transferred into the Transmitter Register and repeatedly transmitted until a character is loaded into the Transmitter Holding Register. At this time, the Fill-Character will be completed and the newly loaded isochronous character will follow contiguously.

Table 3 illustrates all the programmable isochronous character formats.

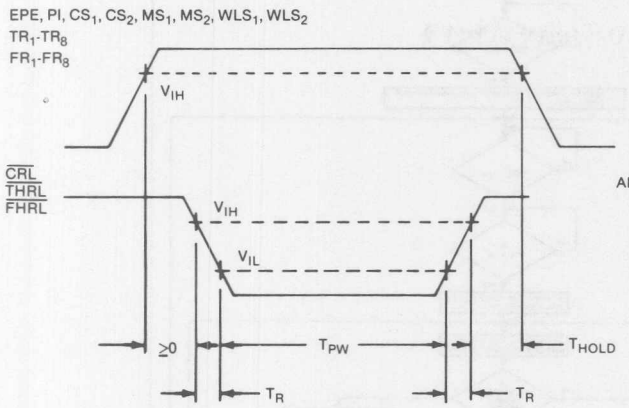
Table 3. ISOC MODE CONTROL DEFINITION

CONTROL WORD							CHARACTER FORMAT			
MSB2	MSB1	WLS2	WLS1	PI	EPE		START BIT	DATA BITS	ADDED PARITY BIT	STOP ELEMENTS
1	1	0	0	0	0		1	5	ODD	1
1	1	0	0	0	1		1	5	EVEN	1
1	1	0	0	1	X		1	5	NONE	1
1	1	0	1	0	0		1	6	ODD	1
1	1	0	1	0	1		1	6	EVEN	1
1	1	0	1	1	X		1	6	NONE	1
1	1	1	0	0	0		1	7	ODD	1
1	1	1	0	0	1		1	7	EVEN	1
1	1	1	0	1	X		1	7	NONE	1
1	1	1	1	0	0		1	8	ODD	1
1	1	1	1	0	1		1	8	EVEN	1
1	1	1	1	1	X		1	8	NONE	1

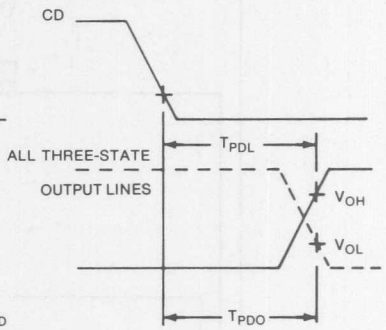
↑ Sets to ISOC Mode



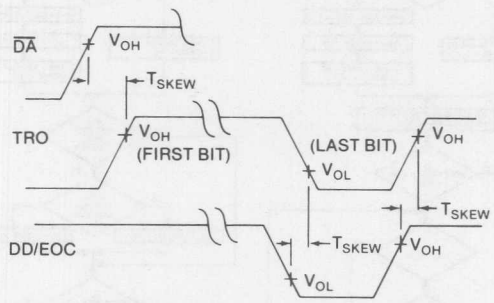
ISOCHRONOUS TIMING EXAMPLE



DATA INPUT LOAD CYCLE

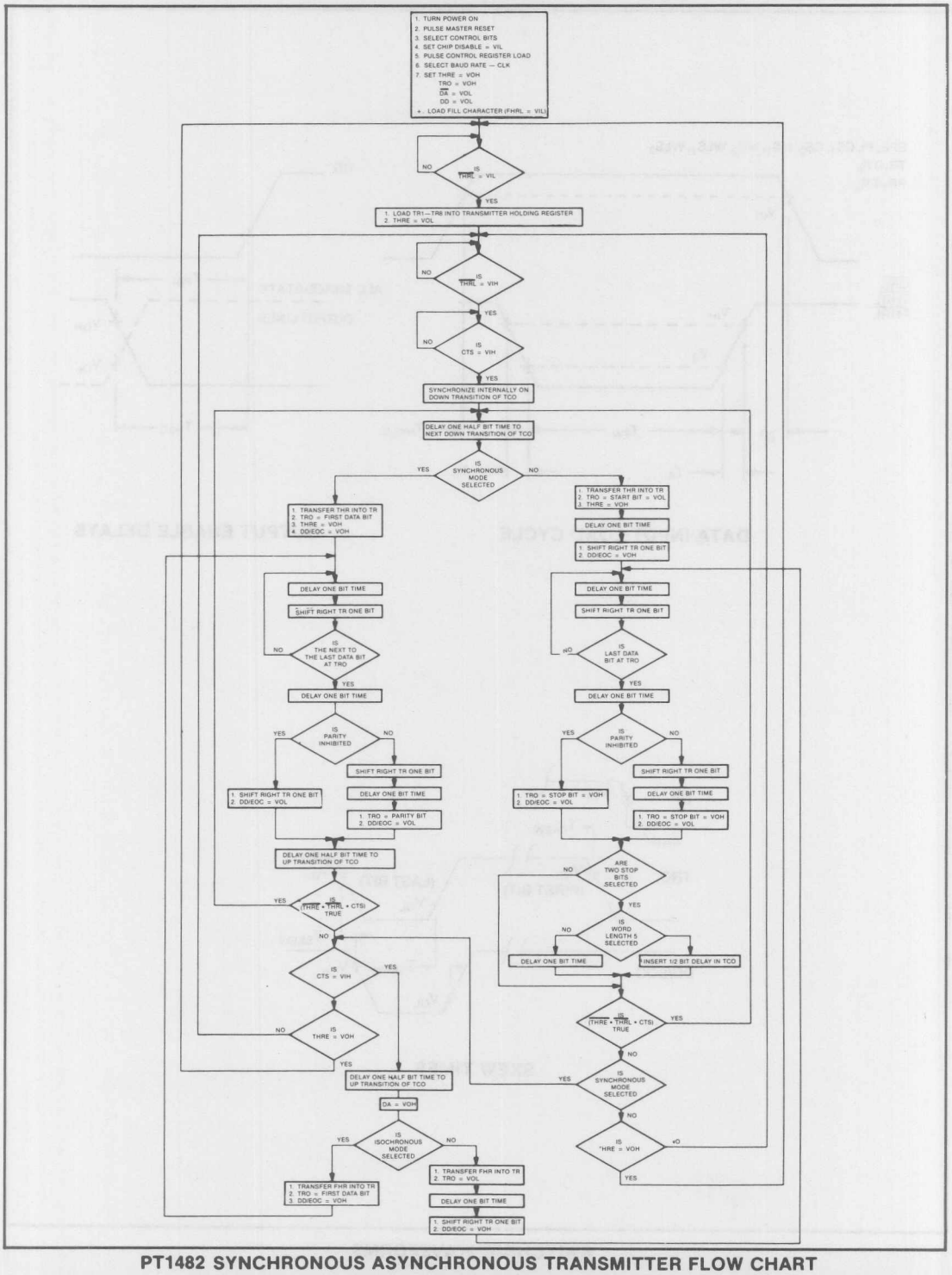


OUTPUT ENABLE DELAYS

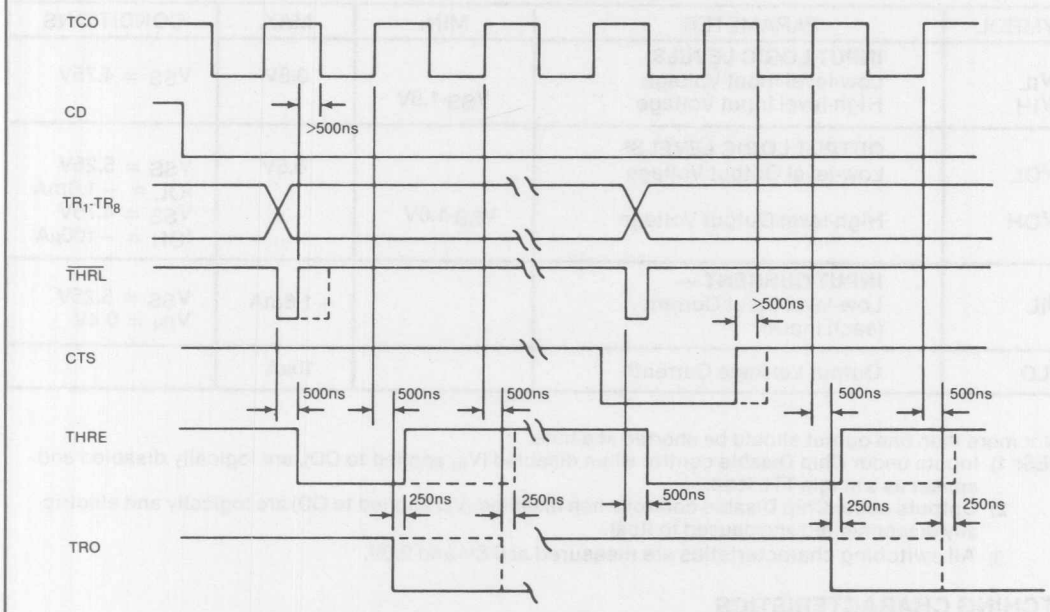


SKEW TIMES

SWITCHING WAVEFORMS



PT1482 SYNCHRONOUS ASYNCHRONOUS TRANSMITTER FLOW CHART



TIMING DETAIL

ABSOLUTE MAXIMUM RATINGS

V_{GG} Supply Voltage		+0.3V to −20V
V_{DD} Supply Voltage		+0.3V to −20V
Clock Input Voltage*		+0.3V to −20V
Logic Input Voltage*		+0.3V to −20V
Logic Output Voltage*		+0.3V to −20V
Storage Temperature	Ceramic	−65°C to +150°C
	Plastic	−55°C to +125°C
Operating Free-Air Temperature T_A Range		0°C to +50°C
Lead Temperature (Soldering, 10 sec.)		300°C

*$V_{GG} = V_{DD} = 0V$

NOTE: These voltages are measured with respect to V_{SS} (Substrate)

ELECTRICAL CHARACTERISTICS

($V_{SS} = V_{CC} = 5V \pm 5\%$, $V_{DD} = 0V$, $V_{GG} = -12V \pm 5\%$, $T_A = 0°C$ to $+50°C$ unless otherwise specified)

SYMBOL	PARAMETER	MIN.	MAX.	CONDITIONS
	INPUT LOGIC LEVELS[1]			
V_{IL}	Low-level Input Voltage		0.8V	$V_{SS} = 4.75V$
V_{IH}	High-level Input Voltage	V_{SS}-1.5V		
	OUTPUT LOGIC LEVELS[2]			
V_{OL}	Low-level Output Voltage		0.5V	$V_{SS} = 5.25V$, $I_{OL} = -1.6mA$
V_{OH}	High-level Output Voltage	V_{SS}-1.0V		$V_{SS} = 4.75V$, $I_{OH} = -100\mu A$
I_{IL}	**INPUT CURRENT —** Low-level Input Current (each input)		−1.6mA	$V_{SS} = 5.25V$, $V_{IN} = 0.4V$
I_{LO}	Output Leakage Current[2]		10μA	

**Not more than one output should be shorted at a time.

NOTES: 1) Inputs under Chip Disable control when disabled (V_{IH} applied to CD), are logically disabled and appear as a single TTL load.

2) Outputs under Chip Disable control when disabled (V_{IH} applied to CD) are logically and electrically disconnected and caused to float.

3) All switching characteristics are measured at 0.8V and 2.0V.

SWITCHING CHARACTERISTICS

($V_{SS} = V_{CC} = 5V \pm 5\%$, $V_{DD} = 0V$, $V_{GG} = -12V \pm 5\%$, $T_A = 0°C$ to $+50°C$, $C_L = 20pf$)

SYMBOL	PARAMETER	MIN.	MAX.	CONDITIONS
F_C	Clock Frequency	DC	100 KHz	1482B-00
		DC	640 KHz	1482B-01
	PULSE WIDTH			
T_{HOLD}	Hold Time	20 nsec		
$T_{\overline{CRL}}$	Control Register Load	250 nsec		
$T_{\overline{THRL}}$	Transmitter Holding Register Load	250 nsec		
$T_{\overline{FHRL}}$	Fill-Character Holding RegisterLoad	250 nsec		
$T_{\overline{DAR}}$	Data Not Available Reset	200 nsec		
T_{MR}	Master Reset	500 nsec		
T_{PD}	Output Enable Delay		500 nsec	
T_{SKEW}	Skew Time		250 nsec	
T_R	Rise Time		150 nsec	
T_F	Fall Time		150 nsec	

See page 429 for ordering information.

UC1671 ASTRO

FEATURES

SYNCHRONOUS AND ASYNCHRONOUS
- Full Duplex Operations

SYNCHRONOUS MODE
- Selectable 5-8 Bit Characters
- Two Successive SYN Characters Sets Synchronization
- Programmable SYN and DLE Character Stripping
- Programmable SYN and DLE-SYN Fill

ASYNCHRONOUS MODE
- Selectable 5-8 Bit Characters
- Line Break Detection and Generation
- 1-, 1½-, or 2-Stop Bit Selection
- False Start Bit Detection Automatic Serial Echo Mode

SYSTEM COMPATIBILITY
- Double Buffering of Data
- 8-Bit Bi-Directional Bus For Data, Status, and Control Words
- All Inputs and Outputs TTL Compatible
- Up to 32 ASTROS Can Be Addressed On Bus
- On-Line Diagnostic Capability

TRANSMISSION ERROR DETECTION-PARITY
- Overrun and Framing

BAUD RATE — DC TO 1M BIT/SEC

8 SELECTABLE CLOCK RATES
- Accepts 1X Clock and Up to 4 Different 32X Baud Rate Clock Inputs
- Up to 47% Distortion Allowance with 32X Clock

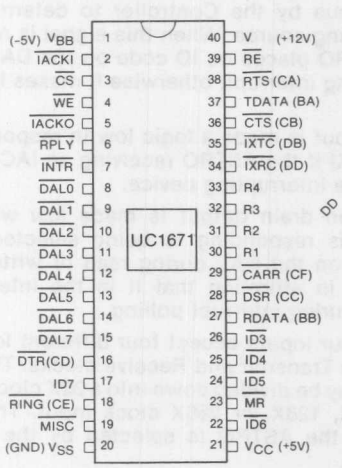
APPLICATIONS

SYNCHRONOUS COMMUNICATIONS
ASYNCHRONOUS COMMUNICATIONS
SERIAL/PARALLEL COMMUNICATIONS

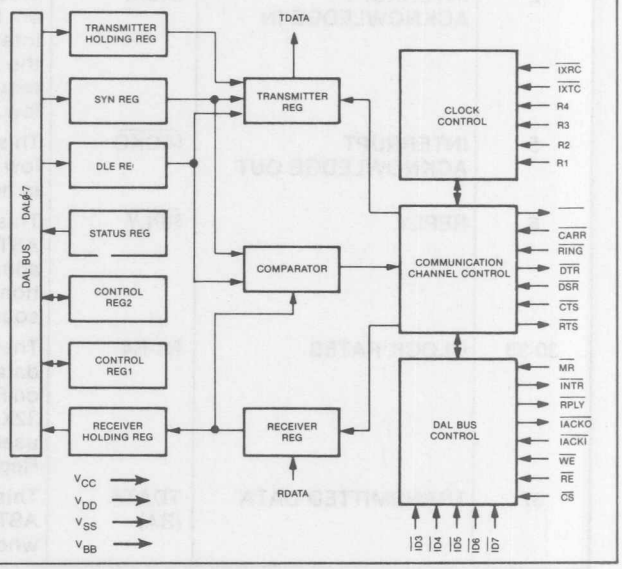
GENERAL DESCRIPTION

The UC1671 (ASTRO) is a MOS/LSI device which performs the functions of interfacing a serial data communication channel to a parallel digital system. The device is capable of full duplex communications (receiving and transmitting) with synchronous or asynchronous systems. The ASTRO is designed to operate on a multiplexed bus with other bus-oriented devices. Its operation is programmed by a processor or controller via the bus and all parallel data transfers with these machines are accomplished over the bus lines.

The ASTRO is fabricated in n-channel silicon gate MOS technology and is TTL compatible on all inputs and outputs.



PIN CONNECTIONS



UC1671 BLOCK DIAGRAM

PIN OUTS

The device is packaged in a 40-pin plastic or ceramic cavity package. The interface signals are defined below with all input/output signals complemented to facilitate bussing and interfacing with TTL. The Data Set controls and Status signals are also complemented to allow for an inversion when converting to EIA RS232C levels. The names and symbols assigned to the Data Set interface signals follows EIA standard nomenclature.

A bar over a signal ($\overline{\text{SIGNAL}}$), means active low (set = low).

PIN NUMBER	PIN NAME	SYMBOL	FUNCTION
1	POWER SUPPLIES	V_{BB}	– 5V
21		V_{CC}	+ 5V
40		V_{DD}	+ 12V
20		V_{SS}	Ground
23	MASTER RESET	$\overline{MR}$	The Control and Status Registers and other controls are cleared when this input is low.
8-15	DATA ACCESS LINES	$\overline{DAL0\text{-}DAL7}$	Eight-bit bi-directional bus used for transfer of data, control, status, and address information.
17,22,24, 25,26	SELECT CODE	$\overline{ID7\text{-}ID3}$	Five input pins which when hard-wired assign the device a unique identification code used to select the device when addressing and used as an identification when responding to interrupts.
3	CHIP SELECT	$\overline{CS}$	The low logic transition of CS identifies a valid address on the DAL bus during Read and Write operations.
39	READ ENABLE	$\overline{RE}$	This signal, when low, gates the contents of an addressed register from a selected ASTRO onto the DAL bus.
4	WRITE ENABLE	$\overline{WE}$	This signal, when low, gates the contents of the DAL bus into the addressed register of a selected ASTRO.
7	INTERRUPT	$\overline{INTR}$	This open drain output is made low when one of the communication interrupt conditions occur.
2	INTERRUPT ACKNOWLEDGE IN	$\overline{IACKI}$	This input becomes low when polling takes place on the bus by the Controller to determine the interrupting source. When this signal is received, the ASTRO places its ID code on the DAL if it is requesting interrupt, otherwise it makes IACKO a low.
5	INTERRUPT ACKNOWLEDGE OUT	$\overline{IACKO}$	This output is made a logic low in response to a low IACKI if the ASTRO receiving an IACKI input is not the interrupting device.
6	REPLY	$\overline{RPLY}$	This open drain output is made low when the ASTRO is responding to being selected by an address on the DAL during read or write operations or in affirming that it is the interrupting source during interrupt polling.
30-33	CLOCK RATES	R1-R4	These four inputs accept four different local 32X data rate Transmit and Receive clocks. The input on R4 may be divided down into a 32X clock from a 32X, 64X, 128X, or 256X clock input. The clock used in the ASTRO is selected by the Control Register.
37	TRANSMITTED DATA	TDATA (BA)	This output is the transmitted serial data from the ASTRO. This output is held in a Marking condition when the transmitter section is not enabled.

PIN NUMBER	PIN NAME	SYMBOL	FUNCTION
27	RECEIVED DATA	RDATA (BB)	This input receives serial data into the ASTRO.
38	REQUEST TO SEND	$\overline{\text{RTS}}$ ($\overline{\text{CA}}$)	This output is enabled by the Control Register and remains in a low state during transmitted data from the ASTRO.
36	CLEAR TO SEND	$\overline{\text{CTS}}$ ($\overline{\text{CB}}$)	This input, when low, enables the transmitter section of the ASTRO.
28	DATA SET READY	$\overline{\text{DSR}}$ ($\overline{\text{CC}}$)	This input generates an interrupt when going On or Off while the Data Terminal Ready signal is On. It appears as a bit in the Status Register.
16	DATA TERMINAL READY	$\overline{\text{DTR}}$ ($\overline{\text{CD}}$)	This output is generated by a bit in the Control Register and indicates Controller readiness.
18	RING INDICATOR	$\overline{\text{RING}}$ ($\overline{\text{CE}}$)	This input from the Data Set generates an interrupt when made low with Data Terminal Ready in the "Off" condition.
29	CARRIER DETECTOR	$\overline{\text{CARR}}$ ($\overline{\text{CF}}$)	This input from the Data Set generates an interrupt when going On or Off if Data Terminal Ready is On. It appears as a bit in the Status Register.
35	TRANSMITTER TIMING	$\overline{\text{IXTC}}$ ($\overline{\text{DB}}$)	This input is the Transmitter 1X Data Rate Clock. Its use is selected by the Control Register. The transmitted data changes on the negative transition of this signal.
34	RECEIVER TIMING	$\overline{\text{IXRC}}$ ($\overline{\text{DD}}$)	This input is the Receiver 1X Data Rate Clock. Its use is selected by the Control Register. The Received Data is sampled by the ASTRO on the positive transition of this signal.
19	MISCELLANEOUS	$\overline{\text{MISC}}$	This output is controlled by a bit in the Control Register and is used as an extra programmable signal.

RECEIVER REGISTER — This 8-bit shift register inputs the received data at a clock rate determined by the Control Register. The incoming data is assembled to the selected character length and then transferred to the Receiver Holding Register with logic zeroes filling out any unused high-order bit positions.

RECEIVER HOLDING REGISTER — This 8-bit parallel buffer register presents assembled receiver characters to the DAL bus lines when requested through a Read operation.

COMPARATOR — The 8-bit comparator is used in the Synchronous mode to compare the assembled contents of the Receiver Register and the SYN register or DLE register. A match between the registers sets up stripping of the received character, when programmed, by preventing the data from being loaded into the Receiver Holding Register. A bit in the Status Register is set when stripping is performed. The comparator output also enables character synchronization of the Receiver on two successive matches with the SYN register.

SYN REGISTER — This 8-bit register is loaded from the DAL lines by a Write operation and holds the synchronization code used to establish receiver character synchronization. It serves as a fill character when no new data is available in the Transmitter Holding Register during transmission. This register cannot be read onto the DAL lines. It must be loaded with logic zeroes in all unused high-order bits.

DLE REGISTER — This 8-bit register is loaded from the DAL lines by a Write operation and holds the "DLE" character used in the Transparent mode of operation in which an idle transmit period is filled with the combination DLE-SYN pair of characters rather than a single SYN character. In addition the ASTRO may be programmed to force a single DLE character prior to any data character transmission while in the transmitter transparent mode.

TRANSMITTER HOLDING REGISTER — This 8-bit parallel buffer register holds parallel transmitted data transferred from the DAL lines by a Write operation. This data is transferred to the Transmitter Register when the transmitter section is enabled and the Transmitter Register is ready to send new data.

TRANSMITTER REGISTER — This 8-bit shift register is loaded from the Transmitter Holding Register, SYN register, or DLE register. The purpose of this register is to serialize data and present it to the transmitted Data output.

CONTROL REGISTERS — There are two 8-bit Control Registers which hold device programming signals such as mode selection, clock selection, interface signal control, and data format. Each of the Control Registers can be loaded from the DAL lines by a Write operation or read onto the DAL lines by a Read operation. The registers are cleared by a Master Reset.

STATUS REGISTER — This 8-bit register holds information on communication errors, interface data register status, match character conditions, and communication equipment status. This register may be read onto the DAL lines by a Read operation.

DATA ACCESS LINES — The DAL is an 8-bit bidirectional bus port over which all address, data, control, and status transfers occur. In addition to transferring data and control words the DAL lines also transfer information related to addressing of the device, reading and writing requests, and interrupting information.

ASTRO OPERATION

ASYNCHRONOUS MODE

Framing of asynchronous characters is provided by a Start bit (logic low) at the beginning of a character and a Stop bit (logic high) at the end of a character. Reception of a character is initiated on recognition of the first Start bit by a positive transition of the receiver clock, after a preceding Stop bit. The Start and Stop bits are stripped off while assembling the serial input into a parallel character.

The character assembly is completed by the reception of the Stop bit after reception of the last character or parity bit. If this bit is a logic high, the character is determined to have correct framing and the ASTRO is prepared to receive the next character. If the Stop bit is a logic low the Framing Error Status flag is set and the Receiver assumes this bit to be the Start bit of the next character. Character assembly continues from this point if the input is still a logic low when sampled at the theoretical center of the assumed Start bit. As long as the Receive input is spacing, all zero characters are assembled and error flags and data received interrupts are generated so that line breaks can be determined. After a character of all zeroes is assembled along with a zero in the Stop bit location, the first received logic high is determined as a Stop bit and this resets the Receiver circuit to a Ready state for assembly of the next character.

In the Asynchronous mode the character transmission occurs when information contained in the Transmitter Holding Register is transferred to the Transmitter Register. Transmission is initiated by the Insertion of a Start bit, followed by the serial output of the character least significant bit first with parity, if enabled, following the most significant bit; then the insertion of a 1-, 1.5-, or 2-bit length Stop condition. If the Transmitter Holding Register is full, the next character transmission starts after the transmission of the Stop bit of the present character in the Transmitter Register. Otherwise, the Mark (logic high) condition is continually transmitted until the Transmitter Holding Register is loaded.

In order to allow re-transmission of data received at a slightly faster character rate, means are provided for shortening the Stop bit length to allow transmission of characters to occur at the same rate as the reception of characters. The Stop bit is shortened by 1/16 of a bit period for 1-Stop bit selection and 3/16 of a bit period for 1.5-, or 2-Stop bit selection, if the next character is ready in the Transmitter Holding Register.

SYNCHRONOUS MODE

Framing of characters is carried out by a special Synchronization Character Code (SYN) transmitted at the beginning of a block of characters. The Receiver, when enabled, searches for two continuous characters matching the bit pattern contained in the SYN register. During the time the Receiver is searching, data is not transferred to the Receiver Holding Register, status bits are not updated, and the Receiver interrupt is not activated. After the detection of the first SYN character, the Receiver assembles subsequent bits into characters whose length is determined by contents of the Control Register. If, after the first SYN character detection, a second SYN character is present, the Receiver enters the Synchronization mode until the Receiver Enable Bit is turned off. If a second successive SYN character is not found, the Receiver reverts back to the Search mode.

In the Synchronous mode a continuous stream of characters are transmitted once the Transmitter is enabled. If the Transmitter Holding Register is not loaded at the time the Transmitter Register has completed transmission of a character, this idle time will be filled by a transmission of the character contained in the SYN register in the Nontransparent mode, or the characters contained in the DLE and SYN registers respectively while in the Transparent mode of operation.

DETAILED OPERATION

Receiver — The Receiver Data input is clocked into the Receiver Register by a 1X Receiver Clock from a modem Data Set, or by a local 32X bit rate clock selected from one of four externally supplied clock

inputs. When using the 1X clock, the Receiver Data is sampled on the positive transition of the clock in both the Asynchronous and Synchronous modes. When using a 32X clock in the Asynchronous mode, the Receive Sampling Clock is phased to the Mark-To-Space transition of the Received Data Start bit and defines, through clock counts, the center of each received Data bit within +0%, −3% at the positive transition 16 clock periods later.

In the Synchronous mode the Sampling Clock is phased to all Mark-To-Space transitions of the Received Data inputs when using a 32X clock. Each transition of the data causes an incremental correction of the Sampling Clock by 1/32nd of a bit period. The Sampling Clock can be immediately phased to every Mark-To-Space Data transition by setting Bit 4 of Control Register 1 to a logic high, while the Receiver is disabled.

When the complete character has been shifted into the Receiver Register it is then transferred to the Receiver Holding Register; the unused, higher number bits are filled with zeroes. At this time the Receiver Status bits (Framing Error/Sync Detect, Parity Error/DLE Detect, Overrun Error, and Data Received) are updated in the Status Register and the Data Received interrupt is activated. Parity Error is set, if encountered while the Receiver parity check is enabled in the Control Register. Overrun Error is set if the Data Received status bit is not cleared through a Read operation by an external device when a new character is ready to be transferred to the Receiver Holding Register. This error flag indicates that a character has been lost, as new data is lost and the old data and its status flags are saved.

The characters assembled in the Receiver Register that match the contents of the SYN or DLE register are not loaded into the Receiver Holding Register, and the DR interrupt is not generated, if Bit 3 of Control Register 2 (CR23 = SYN Strip) or Bit 4 of Control Register 1 (CR14 = DLE Strip) are set respectively, the SYN-DET and DLE-DET status bits are set with the next non SYN or DLE character. When both CR23 and CR14 are set (Transparent mode), the DLE-SYN combination is stripped. The SYN comparison occurs only with the character received after the DLE character. If two successive DLE characters are received only the first DLE character is stripped. No parity check is made while in this mode.

Transmitter — Information is transferred to the Transmitter Holding Register by a Write operation. Information can be loaded into this register at any time, even when the Transmitter is not enabled. Transmission of data is initiated only when the Request To Send bit is set to a logic one in the Control Register and the $\overline{\text{Clear To Send}}$ input is a logic low. Information is normally transferred from the Transmitter Holding Register to the Transmitter Register when the latter has completed transmission of a character. However, information in the DLE register may be transferred prior to the information contained in the Transmitter Holding Register if the Force DLE signal condition is enabled (Bit 5 = Force DLE and 6 = TX Transparent Control Register 1 set to a logic one). The control bit CR15 must be set prior to loading of a new character in the transmitter holding register to insure forcing the DLE character prior to transmission of the data character. The Transmitter Register output passes through a flip-flop which delays the output by one clock period. When using the 1X clock generated by the Modem Data Set, the output data changes state on the negative clock transition and the delay is one bit period. When using a local 32X clock the transmitter section selects one of the four selected rate inputs and divides the clock down to the baud rate. This clock is phased to the Transmitter Holding Register empty flag such that transmission of characters occurs within two data bit times of the loading of the Transmitter Holding Register when the Transmitter Register is empty.

When the Transmitter is enabled, a Transmitter interrupt is generated each time the Transmitter Holding Register is empty. If the Transmitter Holding Register is empty when the Transmitter Register is ready for a new character the Transmitter enters an idle state. During this idle time a logic high will be presented to the Transmitted Data output in the Asynchronous mode or the contents of the SYN register will be presented in the Synchronous Non-transparent mode (CR16 = 0). In the Synchronous Transmit Transparent mode (enabled by Bit 6 of Control Register 1 = Logic 1), the idle state will be filled by a DLE-SYN character transmission in that order. When entering the Transparent mode the DLE-SYN fill will not occur until the first forced DLE.

If the Transmitter section is disabled by a reset of the Request to Send, any partially transmitted character is completed before the transmitter section of the ASTRO is disabled. As soon as the CTS goes high the transmitted data output will go high.

When the Transmit parity is enabled, the selected Odd or Even parity bit is inserted into the last bit of the character in place of the last bit of the Transmitted Register. This limits transfer of character information to a maximum of seven bits plus parity or eight bits without parity. Parity cannot be enabled in the Synchronous Transparency mode.

DEVICE PROGRAMMING

The two 8-bit Control Registers of the ASTRO determine the operative conditions of the ASTRO chip. Control Register 1 is shown in the following table.

BIT 7 7	6	5	4	3	2	1	0
SYNC/ASYNC 0—LOOP MODE 1—NORMAL MODE	ASYNC 0—NON BREAK MODE 1—BREAK MODE SYNC 0—NON TRANSMITTER TRANSPARENT MODE 1—TRANSMIT TRANSPARENT MODE	ASYNC (TRANS. ENABLED) 0—1 1/2 or 2 STOP BIT SELECTION 1—SINGLE STOP BIT ASYNC (TRANS. DISABLED 0—$\overline{\text{MISC OUT}}$ RESET 1—$\overline{\text{MISC OUT}}$ SET SYNC (CR16 = 0) 0—NO PARITY GENERATED 1—TRANSMIT PARITY ENABLED SYNC (CR16 = 1) 0—NO FORCE DLE 1—FORCE DLE	ASYNC 0—NON ECHO MODE 1—AUTO ECHO MODE SYNC (CR12 = 1) 0—DLE STRIPPING NOT ENABLED 1—DLE STRIPPING ENABLED SYNC (CR12 = 0) 0—$\overline{\text{MISC}}$ RESET 1—$\overline{\text{MISC}}$ SET	ASYNC 0—NO PARITY ENABLED 1—PARITY CHECK ENABLED ON RECEIVER PARITY GENERATION ENABLED ON TRANSMITTER SYNC 0—RECEIVER PARITY CHECK IS DISABLED 1—RECEIVER PARITY CHECK IS ENABLED	SYNC/ASYNC 0—RECEIVER DISABLED 1—RECEIVER ENABLED	SYNC/ASYNC 0—$\overline{\text{RTS}}$ RESET 1—$\overline{\text{RTS}}$ SET	SYNC/ASYNC 0—$\overline{\text{DTR}}$ RESET 1—$\overline{\text{DTR}}$ SET

CONTROL REGISTER 1

Control Register 1

Bit 7 — A logic 0 configures the ASTRO into an Internal Data and Control Loop mode and disables the Ring interrupt. In this diagnostic mode the following loops are connected internally:

a. The Transmit Data is connected to the Receive Data with the TD pin held in a Mark condition and the input to the RD pin disregarded.

b. With a 1X clock selected, the Transmitter Clock also becomes the Receive Clock.

c. The $\overline{\text{Data Terminal Ready}}$ ($\overline{\text{DTR}}$) is connected to the $\overline{\text{Data Set Ready}}$ ($\overline{\text{DSR}}$) input, with the $\overline{\text{DTR}}$ output in held in an Off condition (logic high), and the $\overline{\text{DSR}}$ input pin is disregarded.

d. The Request to Send Control bit is connected to the $\overline{\text{Clear To Send}}$ ($\overline{\text{CTS}}$) and Carrier Detector inputs, with the $\overline{\text{RTS}}$ output pin held in an Off condition (logic high), and the $\overline{\text{CTS}}$ and $\overline{\text{Carrier Detector}}$ input pins are disregarded.

3. The $\overline{\text{Miscellaneous}}$ pin is held in an Off (logic high) condition.

A logic 1 on Bit 7 enables the Ring interrupt and returns the ASTRO to the normal full duplex configuration.

Bit 6 — In the *Asynchronous* mode a logic 1 holds the Transmitted Data output in a Spacing (Logic 0) condition, starting at the end of any current transmitted character, when the Transmitter is enabled. Normal Transmitter timing continues so that this Break condition can be timed out after the loading of new characters into the Transmitter Holding Register.

In the *Synchronous* mode a logic 1 sets the Transmitter in a transparent transmission which implies that idle transmitter time will be filled by DLE-SYN character transmission and a DLE can be forced ahead of any character in the Transmitter Holding Register when CR15 is a logic one in the sync mode.

Bit 5 — In the *Asynchronous* mode a logic 1, with the Transmitter enabled, causes a single Stop bit to be transmitted. A logic 0 causes 2-Stop bit transmission for character lengths of 6, 7, or 8 bits and one-and-a-half Stop bits for a character length of 5 bits.

With the Transmitter disabled this bit controls the Miscellaneous output on Pin 19, which may be used for Make Busy on 103 Data Sets, Secondary Transmit on 202 Data Sets, or dialing on CBS Data Couplers.

In the *Synchronous* mode a logic 1 combined with a logic 0 on Bit 6 of control Register 1 enables Transmit parity; if CR15 = 0 or CR15 = 1 no parity is generated. When set to a logic 1 with Bit 6 also a logic 1, the contents of the DLE register are transmitted prior to the next character loaded in the Transmitter Holding Register as part of the Transmit Transparent mode.

Bit 4 — In the *Asynchronous* mode a logic 1 enables the Automatic Echo mode when the receiver section is enabled. In this mode the clocked regenerated data is presented to the Transmit Data output in place of normal transmission through the Transmitter Register. This serial method of echoing does not present any abnormal restrictions on the transmit speed of the terminal. Only the first character of a Break condition of all zeroes (null character) is echoed when a Line Break condition is detected. For all subsequent null characters, with logic zero Stop bits, a steady Marking condition is transmitted until normal character reception resumes. Echoing does not start until a character has been received and the Transmitter is idle. The Transmitter does not have to be enabled during the Echo mode.

In the *Synchronous* mode a logic 1, with the Receiver enabled, does not allow assembled Receiver data matching the DLE register contents to be transferred to the Receiver Holding Register; also, parity checking is disabled.

When the Receiver is not enabled this bit controls the Miscellaneous output on Pin 19, which may be used for New Sync on a 201 Data Set. When operating with a 32X clock and a disabled Receiver a logic 1 on this bit also causes the Receiver timing to synchronize on Mark-To-Space transitions.

Bit 3 — In the *Asynchronous* mode a logic 1 enables check of parity on received characters and generation of parity for transmitted characters.

In the *Synchronous* mode a logic 1 bit enables check of parity on received characters only. **Note:** Transmitter parity enable is controlled by CR15.

Bit 2 — A logic 1 enables the ASTRO to receive data into the Receiver Holding Register, update Receiver Status Bits 1, 2, 3, and 4, and to generate Data Received interrupts. A logic 0 disables the Receiver and clears the Receiver Status bits.

Bit 1 — Controls the $\overline{\text{Request To Send}}$ output on Pin 38 to control the CA circuit of the Data Set. The $\overline{\text{RTS}}$ output is inverted from the state of CR11. A logic 1 combined with a low logic $\overline{\text{Clear To Send}}$ input enables the Transmitter and allows THRE interrupts to be generated. A logic 0 disables the Transmitter and turns off the external $\overline{\text{Request To Send}}$ signal. Any character in the Transmitter Register will be completely transmitted before the Transmitter is turned off. The Request To Send output may be used for other functions such as "Make Busy" on 103 Data Sets.

Bit 0 — Controls the $\overline{\text{Data Terminal Ready}}$ output on Pin 16 to control the CD circuit of the Data Set. A logic 1 enables the Carrier and Data Set Ready interrupts. A logic 0 enables only the telephone line Ring interrupt. The $\overline{\text{DTR}}$ output is inverted from the state of CR10.

Control Register 2

Control Register 2, unlike Control Register 1, cannot be changed at any time. This register should be changed only while both the receiver and transmitter sections of the ASTRO are in the idle state.

Bits 7-6 — These bits select the character length as follows:

Bits 7-6	Character Length
00	8 bits
01	7 bits
10	6 bits
11	5 bits

When parity is enabled it must be considered as a bit when making character length selection, i.e. 5 character bits plus parity = 6 bits.

Bit 5 — A logic 1 selects the Synchronous Character mode. A logic 0 selects the Asynchronous Character mode.

Bit 4 — A logic 1 selects odd parity and a logic 0 selects even parity, when parity is enabled by CR13 and/or CR15.

Bit 3 — In the *Asynchronous* mode a logic 0 selects the rate 1(-32X) clock input (pin 30) as the Receiver Clock rate and a logic 1 selects the same clock rate for the Receiver as selected by Bits 2-0 for the Transmitter. This bit must be a logic 1 for the 1X clock selection by Bits 2-0.

In the *Synchronous* mode a logic 1 causes all DLE-SYN combination characters in the Transparent mode when DLE strip CR14 is a logic 1, or all SYN characters in the Non-transparent mode to be stripped and no Data Received interrupt to be generated. The SYN Detect status bit is set with reception of the next assembled character as it is transferred to the Receiver Holding Register.

Bits 2-0 — These bits select the Transmit and Receive clocks. The Input Clock to the Rate 4 pin may be divided down to form the 32X clock from a multiple clock as shown:

Bits 2-0	Clock
000	1X clock for Transmit and Receive (Pins 35 and 34 respectively)
001	32X clock — Rate 1 input (Pin 30)
010	32X clock — Rate 2 input (Pin 31)
011	32X clock — Rate 3 input (Pin 32)
100	32X clock — Rate 4 input ÷ 1 (Pin 33)
101	32X clock — Rate 4 input ÷ 2 (Pin 33)
110	32X clock — Rate 4 input ÷ 4 (Pin 33)
111	32X clock — Rate 4 input ÷ 8 (Pin 33)

BIT 7 6	5	4	3	2 1 0
SYNC/ASYNC CHARACTER LENGTH SELECT 00 = 8 BITS 01 = 7 BITS 10 = 6 BITS 11 = 5 BITS	MODE SELECT 0—ASYNCHRONOUS MODE 1—SYNCHRONOUS MODE	SYNC/ASYNC 1—ODD PARITY SELECT 0—EVEN PARITY SELECT	ASYNC 1—RECEIVER CLOCK DETERMINED BY BITS 2-0 0—RECEIVER CLK = RATE 1 SYNC (CR14 = 0) 0—NO SYN STRIP 1—SYN STRIP SYNC (CR14 = 1) 0—NO DLE-SYN STRIP 1—DLE-SYN STRIP	SYNC/ASYNC CLOCK SELECT 000 - IX CLOCK 001 - RATE 1 CLOCK 010 - RATE 2 CLOCK 011 - RATE 3 CLOCK 100 - RATE 4 CLOCK 101 - RATE 4 CLOCK ÷ 2 110 - RATE 4 CLOCK ÷ 4 111 - RATE 4 CLOCK ÷ 8

CONTROL REGISTER 2

Status Register

The data contained in the Status Register define Receiver and Transmitter data conditions and status of the Data Set. The Status word is shown and defined below.

Bit 7 — This bit is set to a logic 1 whenever there is a change in state of the Data Set Ready or Carrier Detector inputs while Data Terminal Ready (Bit 0 of Control Register 1) is a logic 1 or the Ring Indicator is turned on, with DTR a logic 0. This bit is cleared when the Status Register is read onto the Data Access Lines.

Bit 6 — This bit is the logic complement of the Data Set Ready input on Pin 28. With 202-type Data Sets it can be used for Secondary Receive.

Bit 5 — This bit is the logic complement of the Carrier Detector input on Pin 29.

Bit 4 — In the *Asynchronous* mode a logic 1 indicates that received data contained a log 0 bit after the last data bit of the character in the stop bit slot, while the Receiver was enabled. This indicates a Framing error. This bit is set to a logic 0 if the proper logic 1 condition for the Stop bit was detected.

In the *Synchronous* mode a logic 1 indicates that the contents of the Receiver Register matched the contents of the SYN Register. The condition of this bit remains for a full character assembly time. If SYN strip (CR23) is enabled this status bit is updated with the character received after the SYN character. In both modes the bit is cleared when the Receiver is disabled.

Bit 3 — When the DLE Strip is enabled (Bit 4 of Control Register 1) the Receiver parity check is disabled and this bit is set to a logic 1 if the *previous character* to the presently assembled character matched the contents of the DLE register; otherwise it is cleared. The DLE DET remains for one character time and is reset on the next character transfer or on a Status Register Read. If DLE Strip is not enabled, this bit is set to a logic 1 when the Receiver is enabled, Receiver parity (Bit 3 of Control Register 1) is also enabled, and the last received character has a Parity error. A logic 0 on this bit indicates correct parity. This bit is cleared in either of the above modes when the Receiver is disabled.

Bit 2 — A logic 1 indicates an Overrun error which occurs if the previous character in the Receiver Holding Register has not been read and Data Received is not reset, at the time a new character is to be transferred to the Receiver Holding Register. This bit is cleared when no Overrun condition is detected, i.e., the next character transfer time or when the Receiver is disabled.

Bit 1 — A logic 1 indicates that the Receiver Holding Register is loaded from the Receiver Register, if the Receiver is enabled. It is cleared to a logic 0 when the Receiver Holding Register is read onto the Data Access Lines, or the Receiver is disabled.

Bit 0 — A logic 1 indicates that the Transmitter Holding Register does not contain a character while the Transmitter is enabled. It is set to a logic 1 when the contents of the Transmitter Holding Register is transferred to the Transmitter Register. It is cleared to a 0 bit when the Transmitter Holding Register is loaded from the DAL, or when the Transmitter is disabled.

INPUT/OUTPUT OPERATIONS

All Data, Control, and Status words are transferred over the Data Access Lines (DAL 0-7). Additional input lines provide controls for addressing a particular unit, and regulating all input and output operations. Other lines provide interrupt capability to indicate to a Controller that an input operation is requested by the ASTRO. All input/output terminology below is referenced to the Controller so that a Read or Input takes data from the ASTRO and places it on the DAL lines, while a Write or Output places data from the DAL lines into the ASTRO. Bit 0 (DALO) must be a logic low in a Read or Write operation.

Read

A Read Operation is initiated by the placement of an *eight-bit address* on the DAL by the Controller. When the Chip Select signal goes to a logic low state, the ASTRO compares Bits 7-3 of the DAL with its hardwired ID code (Pins 17, 22, 24, 25, and 26) and becomes selected on a Match condition. The ASTRO then sets its REPLY line low to acknowledge its readiness to transfer data. Bits 2-0 of the address are used to select ASTRO registers to read from as follows:

Bits 2-0	Selected Register
000	Control Register 1
010	Control Register 2
100	Status Register
110	Receiver Holding Register

BIT 7	6	5	4	3	2	1	0
• DATA SET CHANGE	• DATA SET READY	• CARRIER DETECTOR	• FRAMING ERROR • SYN DETECT	• DLE DETECT • PARITY ERROR	• OVERRUN ERROR	• DATA RECEIVED	• TRANSMITTER HOLDING REGISTER EMPTY

STATUS REGISTER

When the Read Enable ($\overline{RE}$) line is set to a logic low condition by the Controller the ASTRO gates the contents of the addressed register onto the DAL. The Read operation terminates, and the devices becomes unselected, when both the Chip Select and Read Enable return to a logic high condition. Reading of the Receiver Holding Register clears the DR Status bit.

Write

A Write operation is initiated by the placement of an eight-bit address on the DAL by the Controller. The ASTRO compares Bits 7-3 of the DAL with its ID code when the Chip Select input goes to a logic low state. If a Match condition exists, the device is selected and makes it's $\overline{RPLY}$ line low to acknowledge its readiness to transfer data. Bits 2-0 of the address are used to select ASTRO registers to be written into as follows:

Bits 2-0	Selected Register
000	Control Register 1
010	Control Register 2
100	SYN and DLE Register
110	Transmitter Holding Register

When the Write Enable ($\overline{WE}$) line is set to a logic low condition by the Controller the ASTRO gates the data from the DAL into the addressed register. If data is written into the Transmitter Holding Register, the THRE Status bit is cleared to a logic zero.

The 100 address loads both the SYN and DLE registers. After writing into the SYN register the device is conditioned to write into the DLE if followed by another Write pulse with the 100 address. Any intervening Read or Write operation with other addresses resets this condition such that the next 100 will address the SYN register.

Interrupts

The following conditions generate interrupts:

1. **Data Received (DR) —** Indicates transfer of a new character to the Receiver Holding Register while the Receiver is enabled.
2. **Transmitter Holding Register Empty (THRE) —** Indicates that the THR register is empty while the Transmitter is enabled. The first interrupt occurs when the Transmitter becomes enabled if there is an empty THR, or after the character is transferred to the Transmitter Register making the THR empty.
3. **Carrier On —** Indicates Carrier Detector input goes low when DTR is on.
4. **Carrier Off —** Indicates Carrier Detector input goes high when DTR is on.
5. **DSR On —** Indicates the Data Set Ready input goes low when DTR is on.
6. **DSR Off —** Indicates the Data Set Ready input goes high when DTR is on.
7. **Ring On —** Indicates the Ring Indicator input goes low when DTR is off.

Each time an Interrupt condition exists the $\overline{INTR}$ output from the ASTRO is made a logic low. The following interrupt procedure is then carried out even if the interrupt condition is removed.

The Controller acknowledges the Interrupt request by setting the Chip Select ($\overline{CS}$) and the Interrupt Acknowledge Input ($\overline{IACKI}$) to the ASTRO to a Low state. On this transition all non-interrupting devices receiving the $\overline{IACKI}$ set their Interrupt Acknowledge Output ($\overline{IACKO}$) low, enabling lower priority daisy-chained devices to respond to the Interrupt request. The highest priority device that is interrupting will then set its $\overline{RPLY}$ low. This device places its ID code on Bit Positions 7-3 of the DAL when a low $\overline{RE}$ signal is received. In addition Bit 2 is set to a logic one if any of the interrupt numbers 1 and 3-7 above occurred, and remains a logic zero if the THRE has caused the interrupt.

To reset the Interrupt condition ($\overline{INTR}$) Chip Select ($\overline{CS}$) and ($\overline{IACKI}$) must be received by the ASTRO. A setup time must exist between $\overline{CS}$ and the $\overline{RE}$ or $\overline{WE}$ signals to allow chip selection prior to read/write operations and deselection control through the latter signals. The data is removed from the DAL when the $\overline{RE}$ signal returns to the logic high state.

MAXIMUM RATINGS

V_{DD} With Respect to V_{SS} (Ground)		+20 to −0.3V
Max Voltage To Any Input With Respect to V_{SS}		+20 to −0.3V
Operating Temperature		0°C to 70°C
Storage Temperature	Plastic	−55°C to +125°C
	Ceramic	−65°C to +150°C
Power Dissipation		1000 mW

Note: Absolute maximum ratings indicate limits beyond which permanent damage may occur. Continuous operation at these limits is not intended and should be limited to those conditions specified under DC Electrical Characteristics.

OPERATING CHARACTERISTICS

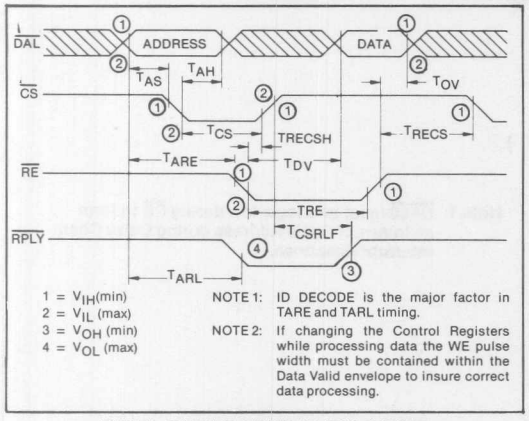
T_A = 0°C to 70°C, V_{DD} = +12.0V ±5%, V_{BB} = −5.0V ±5%, V_{SS} = 0V, V_{CC} = +5V ±5%

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNITS	CONDITIONS
I_{LI}	Input Leakage			10	µA	$V_{IN} = V_{DD}$
I_{LO}	Output Leakage			10	µA	$V_{OUT} = V_{DD}$
I_{BB}	V_{BB} Supply Current			1	mA	V_{BB} = −5V
I_{CCAVE}	V_{CC} Supply Current			80	mA	
I_{DDAVE}	V_{DD} Supply Current			10	mA	
V_{IH}	Input High Voltage	2.4			V	
V_{IL}	Input Low Voltage (All Inputs)			.8	V	
V_{OH}	Output High Voltage	2.8			V	I_O = −100 µA
V_{OL}	Output Low Voltage			.45	V	I_O = 1.6 mA

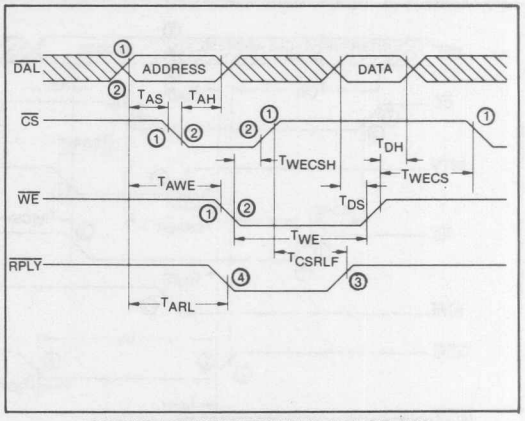
AC CHARACTERISTICS

T_A = 0°C to 70°C, V_{DD} = +12.0V ±5%, V_{BB} = −5.0V ±5%, V_{CC} = +5.0 ±5%, V_{SS} = 0V
CL_{MAX} = 20 pf

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNITS	CONDITIONS
T_{AS}	Address Set-Up Time	0			ns	
t_{AH}	Address Hold Time	150			ns	
T_{ARL}	Address to $\overline{RPLY}$ Delay			400	ns	
T_{CS}	$\overline{CS}$ Width	250			ns	
T_{CSRLF}	$\overline{CS}$ to Reply OFF Delay	0		250	ns	R_L = 2.7 KΩ
T_{MR}	MR Width	1.0			µs	
READ						
T_{ARE}	Address and $\overline{RE}$ Spacing	250			ns	
T_{RECSH}	$\overline{RE}$ and $\overline{CS}$ Overlap	20			ns	
T_{RECS}	$\overline{RE}$ to $\overline{CS}$ Spacing	250			ns	
T_{DV}	$\overline{RE}$ to Data Out Delay			180	ns	C_L = 20 pf
T_{OV}	$\overline{RE}$ Off to DAL Open Delay	20		250	ns	
T_{RE}	$\overline{RE}$ Width	200		1000	ns	
WRITE						
T_{AWE}	Address to $\overline{WE}$ Spacing	250			ns	
T_{WECSH}	$\overline{WE}$ and $\overline{CS}$ Overlap	20			ns	
T_{WE}	$\overline{WE}$ Width	200		1000	ns	
T_{DS}	Data Set-Up Time	150			ns	
T_{DH}	Data Hold Time	100			ns	
TWECS	$\overline{WE}$ to $\overline{CS}$ Spacing	250			ns	



READ CYCLE TIMING DIAGRAM

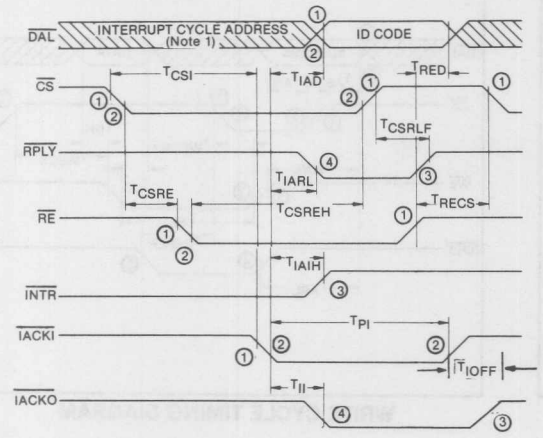


WRITE CYCLE TIMING DIAGRAM

INTERRUPT

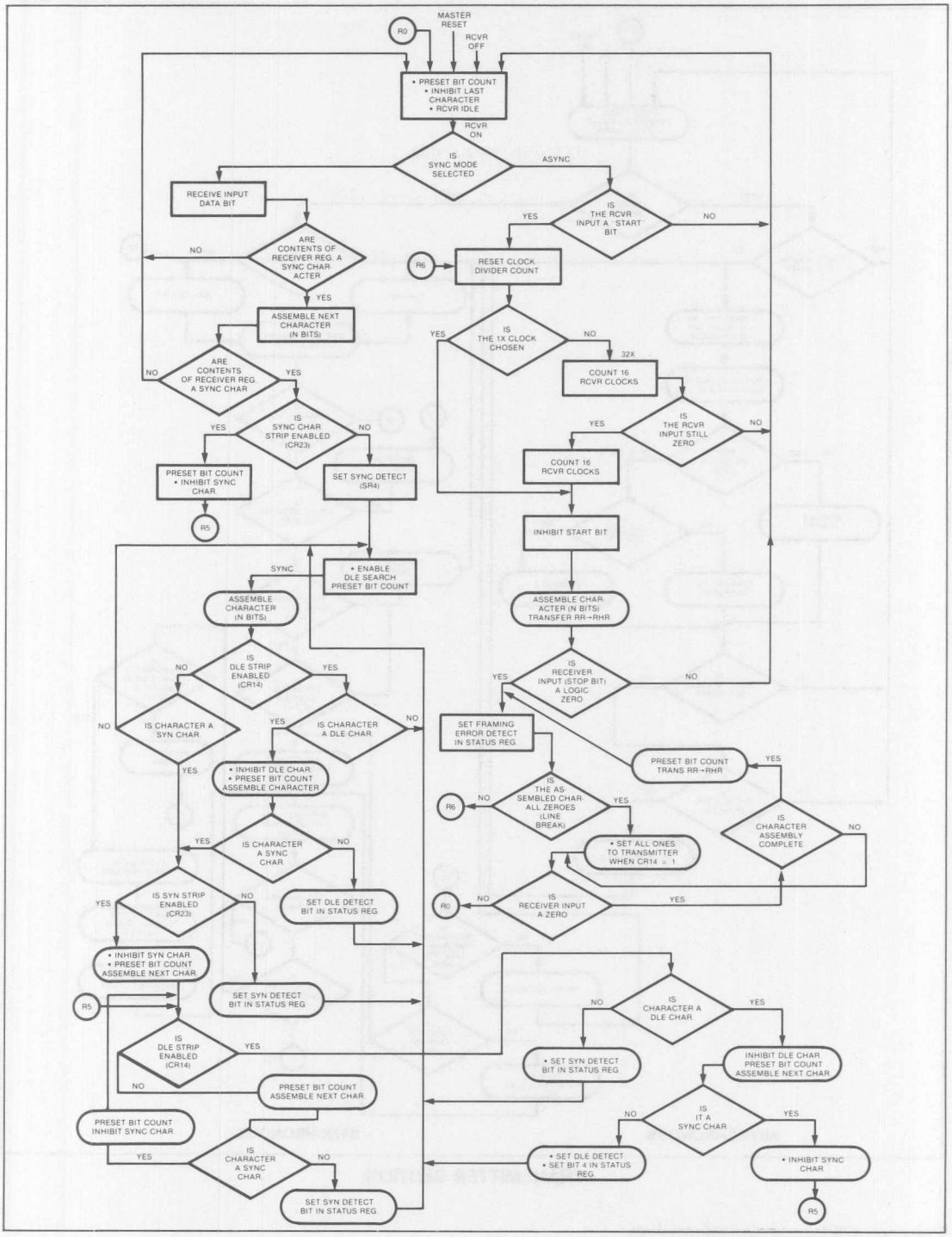
	CHARACTERISTIC	MIN	TYP	MAX	UNITS	CONDITIONS
T_{CSI}	$\overline{CS}$ to $\overline{IACKI}$ Delay	0			ns	
T_{CSRE}	$\overline{CS}$ to $\overline{RE}$ Delay	250			ns	
T_{CSREH}	$\overline{CS}$ and $\overline{RE}$ Overlap	20			ns	
T_{RECS}	$\overline{RE}$ to $\overline{CS}$ Spacing	250			ns	
T_{PI}	$\overline{IACKI}$ Pulse Width	200			ns	
T_{IAD}	$\overline{IACKI}$ to Valid ID Code Delay			250	ns	See Note 1.
T_{OV}	$\overline{RE}$ OFF to $\overline{DAL}$ Open Delay	20		250	ns	
T_{IARL}	$\overline{IACKI}$ to $\overline{RPLY}$ Delay			250	ns	
T_{CSRLF}	$\overline{CS}$ to $\overline{RPLY}$ OFF Delay	0		250	ns	R_L = 2.7 KΩ
T_{IAIH}	$\overline{IACKI}$ ON to $\overline{INTR}$ OFF Delay			300	ns	
T_{II}	$\overline{IACKI}$ to $\overline{IACKO}$ Delay			200	ns	
T_{IOFF}	$\overline{IACKO}$ OFF Delay From $\overline{CS}$ OFF, $\overline{RE}$ OFF, or $\overline{IACKI}$ HIGH.			250	ns	See Note 2.

Note 1: If $\overline{RE}$ goes low after $\overline{IACKI}$ goes low, the delay will be from the falling edge of $\overline{RE}$.
Note 2: $\overline{IACKO}$ goes false after the last one of the following three signals go false: $\overline{CS}$, $\overline{RE}$ and $\overline{IACKI}$. T_{IOFF} is measured from the last signal going false.

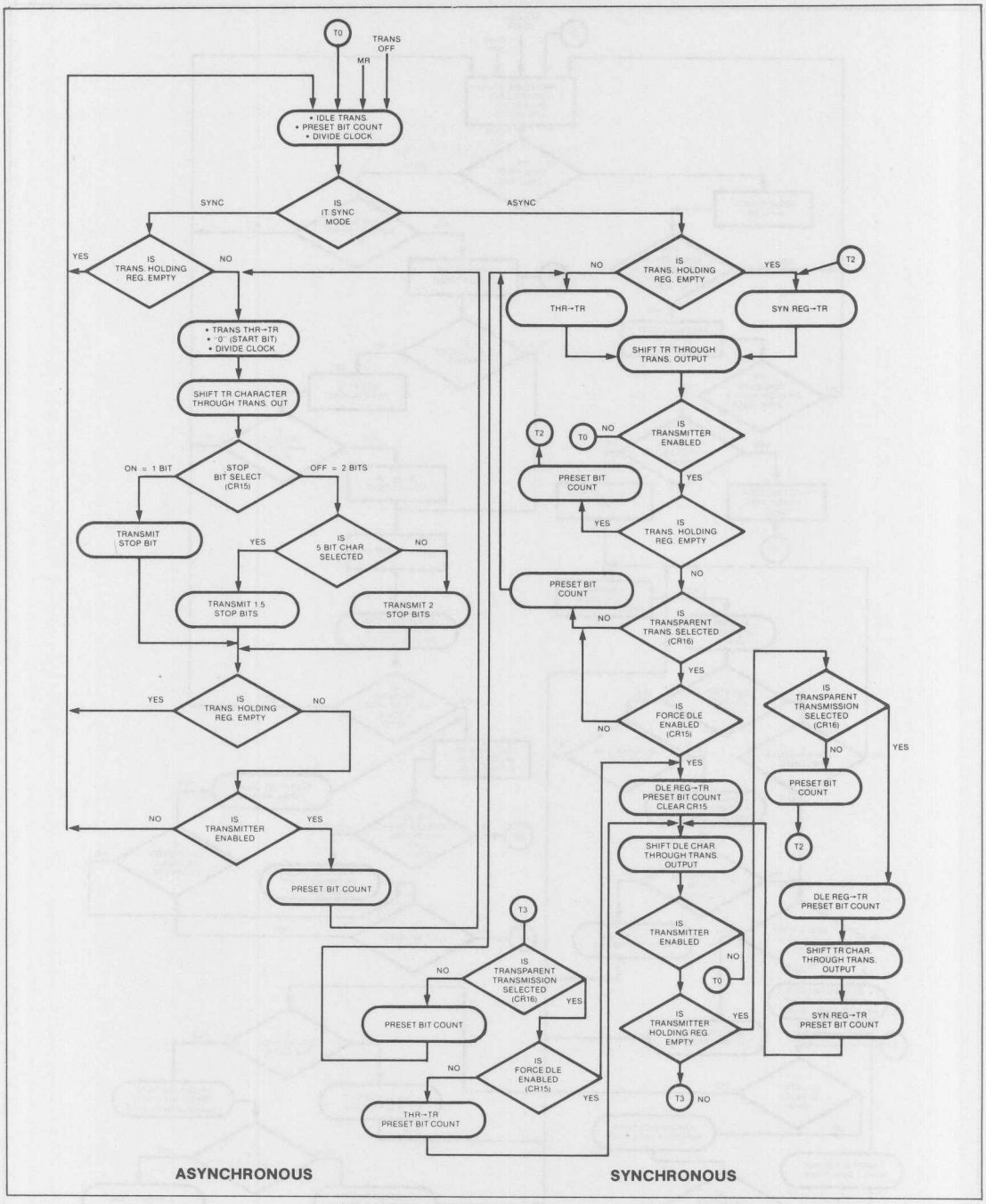


Note 1: $\overline{DAL0}$ must be a logic low during $\overline{CS}$ to form an Interrupt Cycle Address during Daisy Chain Interrupt Response.

INTERRUPT CYCLE TIMING DIAGRAM



RECEIVER SECTION



TRANSMITTER SECTION

See page 429 for ordering information.

WD1931 Asynchronous/Synchronous Receiver/Transmitter

FEATURES

SYNCHRONOUS AND ASYNCHRONOUS
- Full Duplex Operations
- Selectable Character Length (5, 6, 7 or 8 Bits)

SYNCHRONOUS MODE
- Two Successive SYN Characters Sets Synchronization
- Programmable SYN and DLE Character Detection and Stripping
- Programmable SYN and DLE-SYN Fill
- Transparent BI-SYNC Operation
- DDCMP Compatible

ASYNCHRONOUS MODE
- Line Break Detection and Generation
- 1-, 1½-, or 2-Stop Bit Selection
- False Start Bit Detection
- Automatic Serial Echo Mode
- Overrun and Framing Error Detection

SYSTEM COMPATIBILITY
- Double Buffering of Data
- 8-Bit Bi-Directional Bus for Data, Status, and Control Words
- All Inputs and Outputs TTL Compatible
- Chip Select, RE, WE, A0, A1 Interface to CPU
- On-Line Diagnostic Capability
- Data Set, Carrier Detect, and Ring Interrupts

BAUD RATE — DC TO 1M BIT/SEC

8 SELECTABLE CLOCK RATES
- Accepts 1X Clock and Up to Four Different 32X Baud Rate Clock Inputs
- Up to 47% Distortion Allowance with 32X Clock

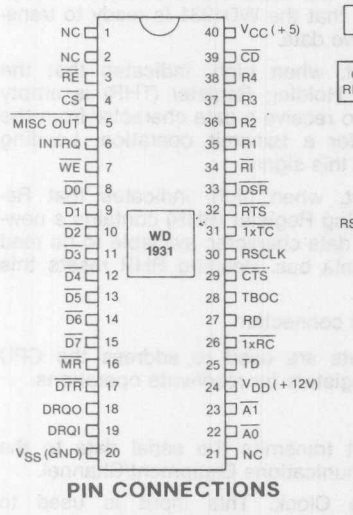
PINOUT COMPATIBLE TO WD193X FOR MULTIPROTOCOL BOARD APPLICATIONS

APPLICATIONS

SYNCHRONOUS COMMUNICATIONS
ASYNCHRONOUS COMMUNICATIONS
SERIAL/PARALLEL COMMUNICATIONS

GENERAL DESCRIPTIONS

The WD1931 is a MOS/LSI device which performs the functions of interfacing a serial data communications channel to a parallel digital system. This device is capable of full duplex communications with asynchronous and/or synchronous systems. Western Digital has made device pin assignments for the WD1931 to make it compatible with the WD193X (Synchronous Data Link Controller). This pin out allows the user to implement a one-board multiprotocol design. For character-oriented asynchronous and/or synchronous (bi-sync) protocols, the WD1931 is used, and for bit-oriented SDLC, HDLC and ADCCP protocols the WD193X is used (see WD193X data sheets and WD1931/WD193X compatibility application notes).



PIN CONNECTIONS

Figure 1. WD1931 PIN CONNECTIONS

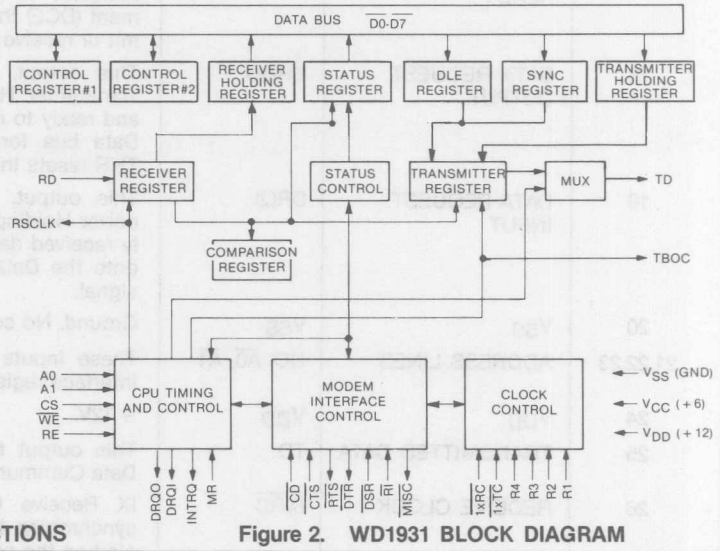


Figure 2. WD1931 BLOCK DIAGRAM

DESCRIPTION OF PIN FUNCTIONS

The WD1931 is packaged in a 40 pin DIP. The following is a functional description of each pin. A bar over a signal (SIGNAL), means active Low.

Table 1. DESCRIPTION OF WD1931 PIN FUNCTIONS

PIN NUMBER	PIN NAME	SYMBOL	FUNCTION
1		NC	No connection allowed to this pin. Used internally only.
2		NC	No connection.
3	READ ENABLE	$\overline{RE}$	This input, when low (and $\overline{CS}$ is active), gates the content of addressed register onto the Data bus.
4	CHIP SELECT	$\overline{CS}$	This input, when low, selects the WD1931 for a read or write operation to/from the Data bus.
5	MISC OUTPUT	$\overline{MISC\ OUT}$	This output is an extra programmable output signal for the convenience of the user. Is controlled by the CR4 bit (sync. mode) or CR5 bit (async mode).
6	INTERRUPT REQUEST	INTRQ	This output is high whenever any of the interrupt conditions occur. Reading the status register resets this signal
7	WRITE ENABLE	$\overline{WE}$	This input when low (and $\overline{CS}$ is active), gates the content of the Data bus into the addressed register.
8-15	DATA BUS	$\overline{D0\text{-}D7}$	Bidirectional three-state Data Bus. Bit 7 is MSB.
16	MASTER RESET	$\overline{MR}$	This input, when low, initializes all the registers, and forces the WD1931 into an idle state. The WD1931 will remain idle until a command is issued by the CPU.
17	DATA TERMINAL READY	$\overline{DTR}$	Modem Control Signal. This output when low, indicates to the Data Communication Equipment (DCE) that the WD1931 is ready to transmit or receive data.
18	DATA REQUEST OUTPUT	DRQO	This output, when high, indicates that the Transmitter Holding Register (THR) is empty and ready to receive a data character from the Data bus for a transmit operation. Loading THR resets this signal.
19	DATA REQUEST INPUT	DRQI	This output, when high, indicates that Receiver Holding Register (RHR) contains a newly received data character, available to be read onto the Data bus. Reading RHR resets this signal.
20	V_{SS}	V_{SS}	Ground. No connection.
21,22,23	ADDRESS LINES	NC, $\overline{A0}$, $\overline{A1}$	These inputs are used to address the CPU interface registers for read/write operations.
24	V_{DD}	V_{DD}	+12V.
25	TRANSMITTED DATA	TD	This output transmits the serial data to the Data Communications Equipment/Channel.
26	RECEIVE CLOCK	$\overline{IXRC}$	IX Receive Clock. This input is used to synchronize the received data. Data is sampled on the positive transition of this signal.

Table 1. PIN FUNCTIONS (Continued)

PIN NUMBER	PIN NAME	SYMBOL	FUNCTION
27	RECEIVED DATA	RD	This input receives the serial data from the Data Communication Equipment/Channel.
28	TRANSMITTER BYTE OUTPUT COMPLETE	TBOC	This output goes high after the last bit of a byte is transmitted including parity if enabled, and is valid for one bit period.
29	CLEAR TO SEND	$\overline{CTS}$	Modem Control Signal. This input when low, indicates that the DCE is ready to accept data from the WD1931.
30	RECEIVER SAMPLE CLOCK	RSCLK	This output goes high when the receiver data is sampled, and is valid for one clock period.
31	TRANSMIT CLOCK 1X TRANSMIT CLOCK	$\overline{1XTC}$	This input is used to synchronize the transmitted data. The falling edge of this signal generates new transmitted data.
32	REQUEST TO SEND	$\overline{RTS}$	Modern Control Signal. This output, when low, indicates to the DCE that the WD1931 is ready to transmit data. If Bit 1 of Control Register 1 is reset during a transmission then $\overline{RTS}$ will go high on the falling edge of the transmitter clock that follows the last bit of the current transmission character.
33	DATA SET READY	$\overline{DSR}$	Modem Control Signal. This input, when low, indicates that the DCE is ready to receive or transmit data.
34	RING INDICATOR	$\overline{RI}$	Modem Control Signal. This input generates an interrupt when made low with DTR off.
35-38	CLOCK RATES	R1-R4	These four rate inputs are used for 32X Local Transmit and Receive clocks. The rate is selected by the Control Register. R1 is common to both Transmitter and Receiver. R2-R4 are clock rates for the Transmitter only.
39	CARRIER DETECT	$\overline{CD}$	Modem Control Signal. This input appears as Status Bit 5 and generates interrupts when going on or off if DTR is on.
40	V_{CC}	V_{CC}	+5V

ORGANIZATION

The WD1931 block diagram is illustrated on page 1. The primary sections include the control, buffer, status, receiver, transmitter, comparison and sync registers.

CONTROL REGISTERS — There are two 8-bit Control Registers which hold device programming signals such as mode selection, clock selection, interface signal control, and data format. Each of the Control Registers can be loaded from the Data Bus by a Write operation or read onto the Data Bus by a Read operation. The registers are cleared by a Master Reset.

RECEIVER HOLDING REGISTER — This 8-bit parallel buffer register presents assembled received characters to the Data Bus when requested through a Read operation.

STATUS REGISTER — This 8-bit register holds information on communication errors, interface data register status, match character conditions, and communication equipment status. This register may be read onto the Data Bus by a Read operation.

DLE REGISTER — This 8-bit register is loaded from the Data Bus by a Write operation and holds the DLE character used in the Transparent mode of operation in which an idle transmit period is filled with the combination DLE-SYN pair of characters rather than a single SYN character. In addition the WD1931 may be programmed to force a single DLE character prior to any data character transmission while in the transmitter transparent mode. This register cannot be read onto the Data Bus. It must be loaded with logic zeroes in all unused high-order bits.

SYN REGISTER — This 8-bit register is loaded from the Data Bus by a Write operation and holds the synchronization code used to establish receiver character synchronization. It serves as a fill character when no new data is available in the Transmitter Holding Register during transmission. This register cannot be read onto the Data Bus. It must be loaded with logic zeroes in all unused high-order bits.

TRANSMITTER HOLDING REGISTER — This 8-bit parallel buffer register holds parallel transmitted data transferred from the Data Bus by a Write operation. This data is transferred to the Transmitter Register when the transmitter section is enabled and the Transmitter Register is empty.

RECEIVER REGISTER — This 8-bit shift register inputs the received data at a clock rate determined by the selected receiver clock. This incoming data is assembled to the selected character length and then transferred to the Receiver Holding Register with logic zeroes filling out any unused high-order bit positions.

TRANSMITTER REGISTER — This 8-bit shift register is loaded from the Transmitter Holding Register, SYN register, or DLE register. The purpose of this register is to serialize data and present it to the transmitted Data output.

COMPARATOR — The 8-bit comparator is used in the Synchronous mode to compare the assembled contents of the Receiver Register to the SYN register or DLE register. A match between the registers sets up stripping of the received character, if so programmed, by preventing the data from being loaded into the Receiver Holding Register. A bit in the Status Register is set when stripping is performed. The comparator output also enables character synchronization of the Receiver on two successive matches with the SYN register.

DATA BUS — The Data Bus is an 8-bit inverted bidirectional bus port over which all data, control, and status transfers occur.

WD1931 OPERATION

ASYNCHRONOUS MODE

Framing of asynchronous characters is provided by a Start bit (logic zero) at the beginning of a character and a Stop bit (logic one) at the end of a character. Reception of a character is initiated on recognition of the first Start bit after a preceding Stop bit. The Start and Stop bits are stripped off while assembling the serial input into a parallel character. If enabled, the parity bit is checked and then stripped off.

The character assembly is completed by the reception of the Stop bit after reception of the last character or parity bit. If this bit is a logic one, the character is determined to have correct framing and the WD1931 is prepared to receive the next character. If the Stop bit is a logic zero, the Framing Error Status flag is set and the Receiver assumes this bit to be the Start bit of the next character. Character assembly continues from this point if the input is still a logic zero when sampled at the theoretical center of the assumed Start bit. As long as Received Data is spacing, all zero characters are assembled and error flags and data received interrupts are generated so that line breaks can be determined. After a character of all zeroes is assembled along with a zero in the Stop bit location, the first received logic one is determined as a Stop bit and this resets the Receiver circuit to a Ready state for assembly of the next character.

In the Asynchronous mode the character transmission occurs when information contained in the Transmitter Holding Register is transferred to the Transmitter Register. Transmission is initiated by the insertion of a Start bit, followed by the serial output of the character (least significant bit first) with parity, if enabled, following the most significant bit, then the insertion of a 1-, 1.5-, or 2-bit length Stop bit. If the Transmitter Holding Register is full, the next character transmission starts after the transmission of the Stop bit(s) of the present character in the Transmitter Register. Otherwise, the Mark (logic one) condition is continually transmitted until the Transmitter Holding Register is loaded.

In order to allow re-transmission of data received at a slightly faster character rate, means are provided for

shortening the Stop bit length to allow transmission of characters to occur at the same rate as the reception of characters. The Stop bit may be shortened a maximum of 1/16 of a bit period for 1-Stop bit selection and 3/16 of a bit period for 1.5-*, or 2-Stop bit selection. To shorten the Stop bit the user must load the Transmitter Holding Register exactly (X + 2) 16ths of a bit period before the end of a stop bit transmission, where X = the number of 16ths the user wishes to strip. If X + 2 exceeds the maximum then no shortening occurs. This feature does not work in 1X clocking mode.

***NOTE:** As a special case, the 1.5 stop bit mode can be shortened from 1/24 to 11/24 of the whole period if the Transmitter Holding Register is loaded (X + 2) 24ths (of the whole period) before the end of the stop bit transmission.

SYNCHRONOUS MODE

Framing of characters is carried out by a special Synchronization Character Code (SYN) transmitted at the beginning of a block of characters. The Receiver, when enabled, searches for two continuous characters matching the bit pattern contained in the SYN register. During the time the Receiver is searching, data is not transferred to the Receiver Holding Register, status bits are not updated, and the DRQI is not activated. After the detection of the first SYN character, the Receiver assembles subsequent bits into characters whose length is determined by contents of the Control Register. If, after the first SYN character detection, a second SYN character is present, the Receiver enters the Synchronization mode until the Act Rec bit is turned off. If a second successive SYN character is not found, the Receiver reverts back to the Search mode.

In the Synchronous mode a continuous stream of characters are transmitted once the Transmitter is enabled. If the Transmitter Holding Register is not loaded at the time the Transmitter Register has completed transmission of a character, this idle time will be filled by a transmission of the character contained in the SYN register in the Non-transparent mode, or the characters contained in the DLE and SYN registers respectively while in the Transparent mode of operation.

DETAILED OPERATION

Receiver — The Received Data input is clocked into the Receiver Register by a 1X Receive Clock from a modem Data Set, or by a local 32X bit rate clock selected from one of four externally supplied clock inputs (R1-R4). When using the 1X clock, the Received Data is sampled on the positive transition of the clock in both the Asynchronous and Synchronous modes. When using a 32X clock in the Asynchronous mode, the Receive Sampling Clock is phased to the Mark-To-Space transition of the Received Data Start bit and defines, through clock counts, the center of each received Data bit within +0%, −3% at the positive transition 16 clock periods later.

In the Synchronous mode the Sampling Clock is phased to all Mark-To-Space transitions of the Received Data inputs when using a 32X clock. Each transition of the data causes an incremental correction of the Sampling Clock by 1/32nd of a bit period. The Sampling Clock can be immediately phased to every Mark-To-Space Data transition by setting Bit 4 of Control Register 1 to a logic one while the Receiver is disabled.

After a complete character has been shifted into the Receiver Register, this is transferred to the Receiver Holding register. The unused higher number bits are filled with zeroes. At this time the Receiver Status bits (Framing Error/Syn Detect, Parity Error/DLE Detect, Overrun Error and DRQI) are updated in the Status Register and the DRQI interrupt is activated. Parity Error is set, if encountered and if the Receiver parity check is enabled in the Control Register. Overrun Error is set if the DRQI bit is not cleared through a Read operation when a new character is ready to be transferred to the Receiver Holding Register. This error flag indicates that new data is lost and the old data character and its status flags are saved.

The characters assembled in the Receiver Register that match the contents of the SYN or DLE registers are not loaded into the Receiver Holding Register and the DRQI is not set if Bit 3 of Control Register 2 (CR23 = SYN Strip) or Bit 4 of Control Register 1 (CR14 = DLE Strip) are set respectively. The SYN DETECT and DLE DETECT status bits are then set with the next non-SYN or DLE character. When both CR23 and CR14 are set (Transparent mode), the DLE-SYN combination is stripped. The SYN comparison occurs only with the character received after the DLE character. If two successive DLE characters are received only the first DLE character is stripped. No parity check is made while in this mode.

Transmitter — A character is transferred to the Transmitter Holding Register by a Write operation. This can be done at any time, even when the Transmitter is not enabled. Transmission of data is initiated only when the ACT TRAN bit is set in the Control Register and the Clear To Send input is Low. A character is normally transferred from the Transmitter Holding Register to the Transmitter Register when the latter has completed transmission of an earlier character. However, information in the DLE register may be transferred prior to this character contained in the Transmitter Holding Register if the Force DLE signal condition is enabled (CR15 and CR16 are set). The control bit CR15 must be set prior to loading of a new character in the transmitter holding register to ensure forcing the DLE character prior to transmission of this new data character. The Transmitter Register output passes through a flip-flop which delays the output by one serial data bit time. When using the 1X clock the output data changes state on the negative clock transition. When

using a local 32X clock the transmitter section selects one of the four selected clock rate inputs (R1-R4) and divides the clock (by 32) down to the baud rate. This clock is phased to the Transmitter Holding Register empty flag (DRQO) such that transmission of characters occurs within two data bit times of the loading of the Transmitter Holding Register when the Transmitter Register is empty.

When the Transmitter is enabled, the DRQO will set each time the Transmitter Holding Register is empty. If the Transmitter Holding Register still is empty when the Transmitter Register is ready for a new character, the Transmitter enters an idle state. During this idle time a logic one will be presented to the Transmitted Data output in the Asynchronous mode or the contents of the SYN register will be presented in the Synchronous Non-transparent mode (CR16 = 0). In the Synchronous Transmit Transparent mode (CR16 is set), the idle state will be filled by a DLE-SYN character transmission in that order. When entering the Transparent mode the DLE-SYN fill will not occur until the first forced DLE.

If the ACT TRAN bit is reset while a character is currently being transmitted, this character will be completed before the transmitter goes idle. When CTS goes high however, the transmitter (TD) immediately goes idle.

When the Transmit parity is enabled, the selected Odd or Even parity bit is inserted between the character and the Stop-bit/s. Parity cannot be enabled in the Synchronous Transparency mode.

CLOCKING

Two clocking schemes are used. In one case a 1X Receiver Timing and Transmitter Timing are used to clock their respective data. In the second case a 32X clock is used to clock the data. The device is capable of selecting from four externally supplied clock-rates (R1-R4).

The use of the 1X clock is the same for the receiver and the transmitter in both the Synchronous and Asynchronous Character modes.

The use of the 32X clock in the receiver differs depending on mode. In the Asynchronous Character mode the receive sampling clock is phased to the mark-space transition of Received Data input at the beginning of the Start bit, causing the Sampling clock to be approximately in the middle of the bit. The accuracy of sampling is +0%, −3%. In the Synchronous Character mode the Receive Sampling clock is phased to all the mark-space transitions on the Received Data input. Each such transition of the data causes an incremental correction of the Sampling clock of 1/32 of the bit period. The Sampling clock can be immediately phased with the data transitions by setting Bit 4 of Control Register 1 to a 1 bit with the receiver disabled. As long as this bit is a one the Sampling clock is locked to every mark-space data transition.

The transmitter divides the selected rate input down to the baud rate. This clock is phased to the DRQO so that character transmission starts within two clocks of the THR loading when the transmitter is idle.

AUTO ECHO FEATURE

The device is capable of serially echoing the received data with a one bit delay when in the Asynchronous mode and the Receiver on. This causes the clocked regenerated received data to be presented to the Transmit Data output rather than the output of the Transmitter Register and a steady marking on TD output. This serial method of echoing does not present any abnormal restrictions on the transmit speed of the terminal. Breaks are not echoed back. When the device detects a Zero Stop bit and a character of all zeroes, the echoing stops and a steady marking is transmitted until such time as normal character reception resumes. Because echoing is taking place during determination of a break condition, a single character of all zeroes (Null character) is echoed when a break is initiated at the terminal. The Echoing is enabled by setting Bit 4 of Control Register 1. Echoing does not start until the start of a receive character at a time when the transmitter is idle and $\overline{CTS}$ is low. If the Transmitter is forced out of the idle mode while a character is being echoed transmission of that character is halted. The Transmitter is idle when CR11 is a zero or the Transmitter is waiting for the THR to be loaded in the Asynchronous mode.

LOOP FEATURE

The device has on-line diagnostic capability. When bit CR17 is a zero (LOOP), the data and data set controls are appropriately looped as follows:

- Transmit Data is connected to Receive Data, with the TD output pin held in a MARK condition and the RD input pin disregarded.
- Transmitter clock is connected to the Receive clock.
- The Data Terminal Ready output is connected to the Data Set Ready input with the $\overline{DTR}$ output pin held in an OFF condition and the $\overline{DSR}$ input pin disregarded.
- The Request To Send output is internally connected to the Clear To Send input and Carrier Detect inputs, with the $\overline{RTS}$ output pin held in an OFF condition and the $\overline{CTS}$ and $\overline{CD}$ input pins disregarded.
- $\overline{MISCELLANEOUS}$ output is also held in an OFF condition.

INPUT/OUTPUT OPERATIONS

All data, control, and status information is when needed transferred to the Data bus. Control and address lines provide for controlling and addressing of input and output operations. In addition, other lines provide interrupt capability for alerting a CPU that input/output is required. Input/output terminology is referenced to the CPU; therefore, a Read or In-

put receives data from the device and places it on the Data bus, while a Write or Output places data from the Data bus into the device.

Read

A read operation is initiated when both $\overline{CS}$ and $\overline{RE}$ go low. When the Read Enable ($\overline{RE}$) line goes low, the device gates the contents of the addressed register onto the Data bus. The device becomes unselected when either the $\overline{CS}$ or $\overline{RE}$ go high. When the Receiver Holding Register is read, the DRQI is reset.

Write

A Write operation is initiated when both $\overline{CS}$ and $\overline{WE}$ go low. When the Write Enable ($\overline{WE}$) line goes low, the device gates the data from the Data bus into the addressed register. When either the $\overline{CS}$ or $\overline{WE}$ go high the device becomes unselected. When the Transmitter Holding Register is written into, the DRQO is reset.

After first writing into SYN the device is conditioned to write into DLE if followed by another Write to that same address. Any intervening Read or Write to other addresses reset this condition.

$\overline{A0}$ and $\overline{A1}$ address device registers for Read/Write operations are shown here:

Table 2. REGISTER ADDRESS FOR READ/WRITE OPERATIONS

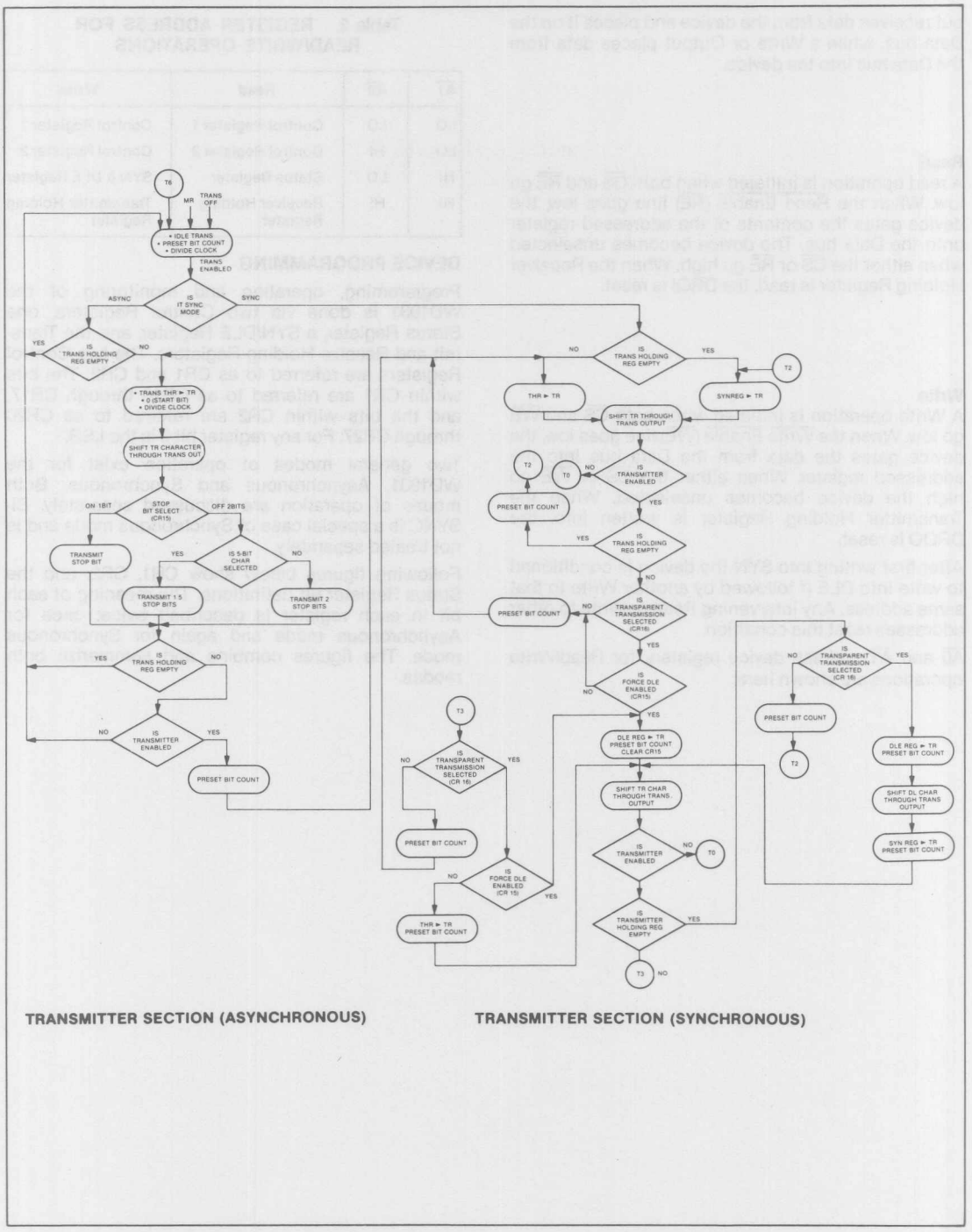
$\overline{A1}$	$\overline{A0}$	Read	Write
LO	LO	Control Register 1	Control Register 1
LO	HI	Control Register 2	Control Register 2
HI	LO	Status Register	SYN & DLE Register
HI	HI	Receiver Holding Register	Transmitter Holding Register

DEVICE PROGRAMMING

Programming, operating and monitoring of the WD1931 is done via two Control Registers, one Status Register, a SYN/DLE Register, and the Transmit and Receive Holding Registers. The two Control Registers are referred to as CR1 and CR2. The bits within CR1 are referred to as CR10 through CR17, and the bits within CR2 are referred to as CR20 through CR27. For any register bit 0 is the LSB.

Two general modes of operation exist for the WD1931, Asynchronous and Synchronous. Both modes of operation are discussed separately. BISYNC is a special case of Synchronous mode and is not treated separately.

Following figures below show CR1, CR2, and the Status Register bit definitions. The meaning of each bit in each register is described twice: once for Asynchronous mode and again for Synchronous mode. The figures combine and summarize both modes.



TRANSMITTER SECTION (ASYNCHRONOUS) **TRANSMITTER SECTION (SYNCHRONOUS)**

Figure 5. TRANSMITTER FLOW CHART

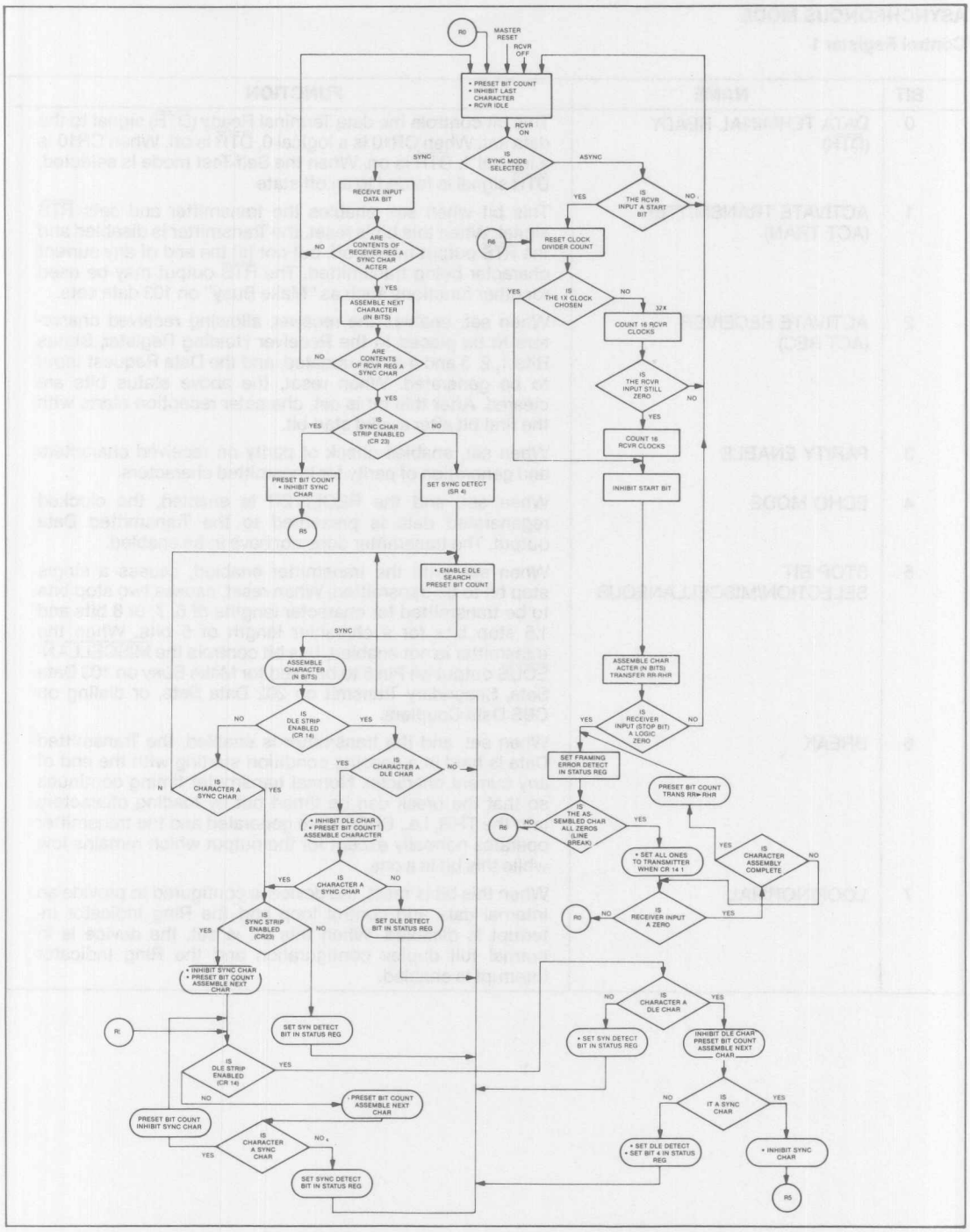


Figure 6. RECEIVER FLOW CHART

ASYNCHRONOUS MODE

Control Register 1

BIT	NAME	FUNCTION
0	DATA TERMINAL READY ($\overline{DTR}$)	This bit controls the data Terminal Ready ($\overline{DTR}$) signal to the data set. When CR10 is a logical 0, $\overline{DTR}$ is off. When CR10 is a logical 1, $\overline{DTR}$ is on. When the Self-Test mode is selected, $\overline{DTR}$ signal is forced to an off state
1	ACTIVATE TRANSMITTER (ACT TRAN)	This bit when set, enables the transmitter and sets $\overline{RTS}$ signal. When this bit is reset, the Transmitter is disabled and the $\overline{RTS}$ output turned off, but not till the end of any current character being transmitted. The $\overline{RTS}$ output may be used for other functions such as "Make Busy" on 103 data sets.
2	ACTIVATE RECEIVER (ACT REC)	When set, enables the receiver, allowing received characters to be placed in the Receiver Holding Register, Status Bits 1, 2, 3 and 4 to be updated, and the Data Request input to be generated. When reset, the above status bits are cleared. After this bit is set, character reception starts with the first bit after a valid start bit.
3	PARITY ENABLE	When set, enables check of parity on received characters and generation of parity for transmitted characters.
4	ECHO MODE	When set, and the RECEIVER is enabled, the clocked regenerated data is presented to the Transmitted Data output. The transmitter does not have to be enabled.
5	STOP BIT SELECTION/MISCELLANEOUS	When set, with the transmitter enabled, causes a single stop bit to be transmitted. When reset, causes two stop bits to be transmitted for character lengths of 6, 7, or 8 bits and 1.5 stop bits for a character length of 5 bits. When the transmitter is not enabled, this bit controls the $\overline{MISCELLANEOUS}$ output on Pin 5 to be used for Make Busy on 103 Data Sets, Secondary Transmit on 202 Data Sets, or dialing on CBS Data Couplers.
6	BREAK	When set, and the transmitter is enabled, the Transmitted Data is held in a spacing condition starting with the end of any current character. Normal transmitter timing continues so that the break can be timed out by loading characters into the THR, i.e., DRQOs are generated and the transmitter operates normally except for the output which remains low while this bit is a one.
7	LOOP/NORMAL	When this bit is reset, the device is configured to provide an internal data and control loop and the Ring Indicator interrupt is disabled. When this bit is set, the device is in normal full duplex configuration and the Ring Indicator interrupt is enabled.

Control Register 2

BIT	NAME	FUNCTION
2-0	CLOCK SELECT	Selects Transmit and Receive clock as follows: 0 — $\overline{IXRC}/\overline{IXTC}$ (IX) Transmitter Clock and if RX = 0, also Receive Clock 1 — Rate 1 (32X) 2 — Rate 2 (32X) 3 — Rate 3 (32X) 4 — Rate 4 (32X) 5 — Rate 4 (64X) 6 — Rate 4 (32X) (128X) 7 — Rate 4 (32X) (256X) } Transmitter Clock Only
3	ALTERNATE RECEIVER X CLOCK	When reset, selects Rate 1 as the Receiver clock rate. When set, provides the same rate as Transmitter Clock (R1-R4). This bit must be set if 1X clocking is selected in bits 2-0.
4	PARITY ODD/EVEN	When set, selects Odd Parity and reset selects Even Parity, when Parity is enabled.
5	CHARACTER MODE	When reset, selects Asynchronous Character Mode. When set selects Synchronous Character Mode.
7-6	CHARACTER LENGTH	Selects number of bits per character as follows (excluding parity bit): 0-8 bits 1-7 bits 2-6 bits 3-5 bits

SYNCHRONOUS MODE

Control Register 1

BIT	NAME	FUNCTION
0	DATA TERMINAL READY (DTR)	This bit controls the data Terminal Ready ($\overline{DTR}$) signal to the data set. When CR10 is a logical 0, $\overline{DTR}$ is off. When CR10 is a logical 1, $\overline{DTR}$ is on. When the Self-Test mode is selected, $\overline{DTR}$ signal is forced to an off state
1	ACTIVATE TRANSMITTER (ACT TRAN)	This bit when set, enables the transmitter and sets $\overline{RTS}$ signal. When this bit is reset, the Transmitter is disabled and the $\overline{RTS}$ output turned off, but not till the end of any current character being transmitted. The $\overline{RTS}$ output may be used for other functions such as "Make Busy" on 103 data sets.
2	ACTIVATE RECEIVER (ACT REC)	When set, enables the receiver, allowing received characters to be placed in the Receiver Holding Register, Status Bits 1, 2, 3 and 4 to be updated, and the Data Request input to be generated. When reset, the above status bits are cleared. After this bit is set, character reception starts after two matches to the contents of SYN Register.

Control Register 1 (Sync Mode continued)

BIT	NAME	FUNCTION
3	PARITY ENABLE	When set, enables check of parity on received characters only.
4	DLE STRIP/MISCELLANEOUS	When set, and the receiver is activated, received characters which match the contents of the DLE Register are stripped out. Also parity checking is disabled. When the receiver is not activated, this bit controls the $\overline{\text{MISCELLANEOUS}}$ output on Pin 5 to be used for New Sync on a 201 Data Set. When operating with a 32X clock and the receiver is not activated, this bit set also causes the receiver bit timing to synchronize on mark-space transitions.
5	TX PARITY ENABLE/ FORCE DLE	When set, with Bit 6 of Control Register 1 reset, Transmit Parity is enabled, otherwise no parity is generated. When set, with Bit 6 set, it causes the contents of the DLE Register to be transmitted prior to the next character loaded in the Transmitter Holding Register. (See description of Transparency)
6	TX TRANSPARENT	When set, the transmitter is conditioned for transparent transmission, which implies that idle fill will be DLE-SYN and a DLE can be forced ahead of any character in the THR by use of Bit 5. (See description of Transparency)
7	LOOP/NORMAL	When this bit is reset, the device is configured to provide an internal data and control loop (see Loop feature) and the Ring Indicator interrupt is disabled. When this bit is set, the device is in normal full duplex configuration and the Ring Indicator interrupt is enabled.

Control Register 2

BIT	NAME	FUNCTION
2-0	CLOCK SELECT	Selects Transmit and Receive clock as follows: 0 — $\overline{\text{IXRC}}$/$\overline{\text{IXTC}}$ (IX) Transmitter Clock, and if RX = 0, also Receive Clock 1 — Rate 1 (32X) 2 — Rate 2 (32X) 3 — Rate 3 (32X) 4 — Rate 4 (32X) 5 — Rate 4 (64X) 6 — Rate 4 (128X) 7 — Rate 4 (256X) } Transmitter Clock Only
3	STRIP SYN	When set, and the receiver is enabled, received characters which match the contents of the SYN Register are stripped out. Also the SYN Detect status bit will be set for the next input character. No SYN stripping occurs when reset.
4	PARITY ODD/EVEN	When set, selects Odd Parity, when reset, selects Even Parity, when parity is enabled.
5	CHARACTER MODE	When reset, selects Asynchronous Mode. When set, selects Synchronous Mode.
7-6	CHARACTER LENGTH	Selects number of bits per character as follows (excluding parity bit): 0-8 bits 1-7 bits 2-6 bits 3-5 bits

TRANSPARENCY

The Transmit Transparency mode causes Idle Fill to be the pair of characters DLE-SYN rather than a single SYN, and provides for preceding a character loaded into the THR with a DLE without the possibility of an intervening DLE-SYN fill. Transparency is enabled by Bit 6 of Control Register 1, which allows force DLE to be controlled by Control Register 1, Bit 5, but the DLE-SYN fill is not activated until after the first forced DLE. All aspects of Transparency are disabled when Bit 6 is reset. When forcing transmission of a DLE, Bit 5 should be set prior to loading the Transmitter Holding Register, otherwise the character in the Transmitter Holding Register may be transferred to the Transmitter Register prior to the setting of the Control Bit.

STATUS

The Status Register contains the following status information:

BIT	NAME	FUNCTION
0	DATA REQUEST OUTPUT (DRQO)	When set, indicates a Data Request Output, meaning THR is empty and CPU is allowed to load the new character to be transmitted into the THR register. This bit is a mirror image of DPQO signal (pin 18). Loading of THR resets DRQO.
1	DATA REQUEST INPUT (DRQI)	When set, indicates a Data Request Input meaning RHR is loaded with a new received character, and CDU is allowed to read RHR register. This bit is a mirror image of DRQI signal (pin 19). Reading RHR, resets DRQI.
2	OVERRUN ERROR (OE)	This bit is set, when the previous character in the Receiver Holding Register has *not* been read at the time a new character is ready to be transferred to the Receiver Holding Register. The bit is reset when a character is transferred to the Receiver Holding Register. It is also reset when the receiver is deactivated.
3	PARITY ERROR (PE)/ DLE DETECT	This bit is set, when the receiver is activated and Receive parity is enabled and the last received character has a parity error, and is reset if the character has correct parity. When the DLE strip is enabled, the Receiver parity check is disabled and this bit is set if the *previous character* matched the contents of the DLE Register and was stripped, otherwise it is reset. This bit is reset when the receiver is deactivated.
4	FRAMING ERROR (FE)/SYN DETECT (SD)	In the asynchronous mode this bit is set if the bit after the last data bit, in the stop-bit slot, is a zero and the receiver is enabled. This bit is reset if the stop-bit is a one. In the synchronous mode this bit is set when the contents of the Receiver Register matches the contents of the SYN Register and SYN strip is not enabled. In both modes the bit is reset when the receiver is deactivated. If SYN strip is enabled this status bit is updated when a character is received after the SYN character.
5	CARRIER DETECTOR (CD)	This bit is a mirror image of CD signal. When this signal is set, SR5 is set.
6	DATA SET READY (DRS)	This bit is a mirror image of $\overline{\text{DSR}}$ signal. When this signal is set SR6 is set. With 202-type data sets it can be used for Secondary Receive.
7	DATA SET CHANGE (DSC)	This bit is set when there is a change in the state of the Data Set Ready or Carrier Detect inputs when DTR is on, or when the Ring Indicator goes on and DTR is off. This bit is reset when the Status Register is read.

Control Registers 1, 2 and STATUS Bit Assignments

(See Note 1 and 2)

CONTROL REGISTER 1

BIT 7	6	5	4	3	2	1	0
SYNC/ASYNC 0—LOOP MODE 1—NORMAL MODE	ASYNC 0—NON BREAK MODE 1—BREAK MODE SYNC 0—NON TRANSMITTER TRANSPARENT MODE 1—TRANSMIT TRANSPARENT MODE	ASYNC (TRANS. ENABLED) 0—1 1/2 or 2 STOP BIT SELECTION 1—SINGLE STOP BIT SELECTION ASYNC (TRANS. DISABLED) 0—$\overline{\text{MISC OUT}}$ RESET (= HI) 1—$\overline{\text{MISC OUT}}$ SET (= LO) SYNC (CR16 = 0) 0—NO PARITY GENERATED 1—TRANSMIT PARITY GENERATED SYNC (CR16 = 1) 0—NO FORCE DLE 1—FORCE DLE	ASYNC 0—NON ECHO MODE 1—AUTO ECHO MODE SYNC (CR12 = 1) 0—DLE STRIPPING NOT ENABLED 1—DLE STRIPPING ENABLED SYNC (CR12 = 0) 0—$\overline{\text{MISC OUT}}$ RESET (= HI) 1—$\overline{\text{MISC OUT}}$ SET (= LO)	ASYNC 0—PARITY DISABLED 1—PARITY CHECK ENABLED ON RECEIVER PARITY GENERATION ENABLED ON TRANSMITTER SYNC 0—RECEIVER PARITY CHECK DISABLED 1—RECEIVER PARITY CHECK ENABLED	SYNC/ASYNC 0—RECEIVER DEACTIVATED 1—RECEIVER ACTIVATED	SYNC/ASYNC 0—TRANSMITTER DEACTIVATED 1—TRANSMITTER ACTIVATED	SYNC/ASYNC 0—RESETS $\overline{\text{DTR}}$ OUT (HI) 1—SETS $\overline{\text{DTR}}$ OUT (LO)

(See Note 1 and 2)

CONTROL REGISTER 2

BIT 7 6	5	4	3	2 1 0
SYNC/ASYNC CHARACTER LENGTH SELECT 00 = 8 BITS 01 = 7 BITS 10 = 6 BITS 11 = 5 BITS	MODE SELECT 0—ASYNCHRONOUS MODE 1—SYNCHRONOUS MODE	SYNC/ASYNC 1—ODD PARITY SELECT 0—EVEN PARITY SELECT	ASYNC 1—RECEIVER CLOCK DETERMINED BY BITS 2-0 0—RECEIVER CLK = RATE 1 0—NO SYN STRIP 1—SYN STRIP	SYNC/ASYNC CLOCK SELECT 000 - IX CLOCK 001 - RATE 1 CLOCK (32X) 010 - RATE 2 CLOCK (32X) 011 - RATE 3 CLOCK (32X) 100 - RATE 4 CLOCK (32X) 101 - RATE 4 CLOCK (64X) 110 - RATE 4 CLOCK (128X) 111 - RATE 4 CLOCK (256X)

NOTE 1. As a result of the WD1931's inverted data bus, to set a bit in above registers, the respective data bus line is to be set to low (V_{IL}).

(See Note 2)

STATUS REGISTER

BIT 7	6	5	4	3	2	1	0
• DATA SET CHANGE (DSC)	• DATA SET READY (DSR)	• CARRIER DETECTOR (CD)	• FRAMING ERROR/ SYN DETECT (FE/SD)	• DLE DETECT/ PARITY ERROR (DLE/PE)	• OVERRUN ERROR (OE)	• DATA REQUEST INPUT (DRQI)	• DATA REQUEST OUTPUT (DRQO)

NOTE 2. As a result of the WD1931's inverted data bus, when reading above registers, a data bus line set to low (V_{IL}), indicates the respective bit in the addressed register is set (logical 1).

REGISTER ADDRESS

LO = V_{IL} at pins

HI = V_{OH} at pins

Reg	$\overline{A1}$	$\overline{A0}$	Read	Write
0	LO	LO	Control Register 1	Control Register 1
1	LO	HI	Control Register 2	Control Register 2
2	HI	LO	Status Register	SYN & DLE Register
3	HI	HI	Receiver Holding Register	Transmitter Holding Register

DATA SET CHANGE INTERRUPTS

The following interrupts can be generated.

Carrier Detect On

The Carrier Detect On interrupt occurs when the Carrier Detect input ($\overline{CD}$) goes low and $\overline{DTR}$ is on.

Carrier Detect Off

The Carrier Detect Off interrupt occurs when the Carrier Detect input ($\overline{CD}$) goes high and $\overline{DTR}$ is on.

DSR On

The DSR On interrupt occurs when the Data Set Ready input ($\overline{DSR}$) goes low and $\overline{DTR}$ is on.

DSR Off

The DSR Off interrupt occurs when the Data Set Ready input ($\overline{DSR}$) goes high and $\overline{DTR}$ is on.

Ring Indicator On

The Ring Indicator On interrupt occurs when the Ring Indicator input ($\overline{RI}$) goes low and $\overline{DTR}$ is off.

When an interrupt condition exists, the INTRQ output is set. Reading the Status Register or activating Master Reset ($\overline{MR}$) will reset INTRQ.

DATA BUS CONTROLS

The following Data Bus controls can be generated.

Data Request Output

This control signal occurs when the THR is empty while the transmitter is enabled.

Data Request Input

This control signal occurs when the RHR is full while the receiver is enabled.

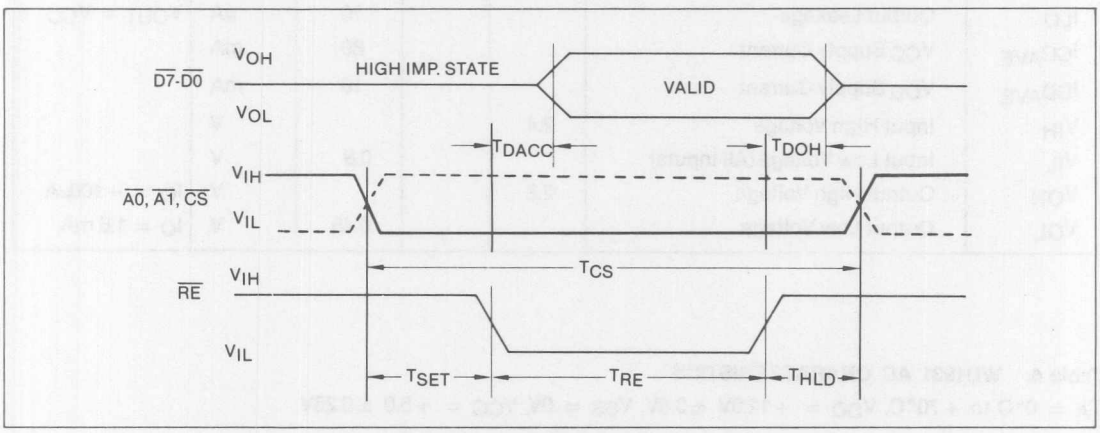


Figure 3. READ TIMING

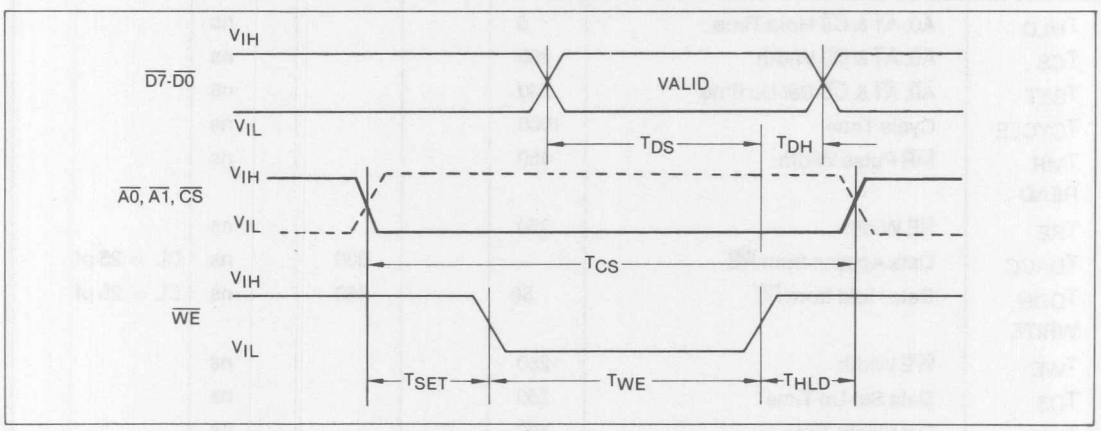


Figure 4. WRITE TIMING

MAXIMUM RATINGS

V_{DD} With Respect to V_{SS} (Ground)		+15 to −0.3V
Max. Voltage To Any Input With Respect to V_{SS}		+20 to −0.3V
Operating Temperature		0°C to +70°C
Power Dissipation		600 mW
Storage Temperature	Ceramic	−65°C to +150°C
	Plastic	−55°C to +125°C

Table 3. WD1931 DC CHARACTERISTICS

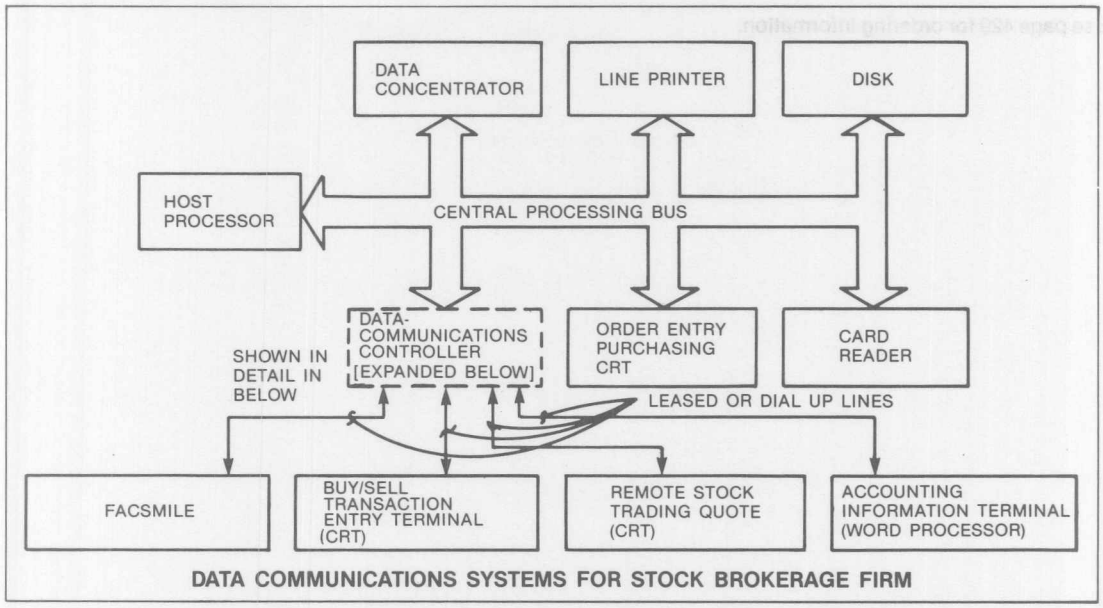
T_A = 0°C to +70°C, V_{DD} = +12.0V ± 0.6V, V_{CC} = +5.0V ± 0.25V, V_{SS} = 0V

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNITS	CONDITIONS
I_{LI}	Input Leakage			10	μA	$V_{IN} = V_{DD}$
I_{LO}	Output Leakage			10	μA	$V_{OUT} = V_{CC}$
I_{CCAVE}	V_{CC} Supply Current			80	mA	
I_{DDAVE}	V_{DD} Supply Current			10	mA	
V_{IH}	Input High Voltage	2.4			V	
V_{IL}	Input Low Voltage (All Inputs)			0.8	V	
V_{OH}	Output High Voltage	2.8			V	$I_O = -100\mu A$
V_{OL}	Output Low Voltage			0.45	V	I_O = 1.6 mA

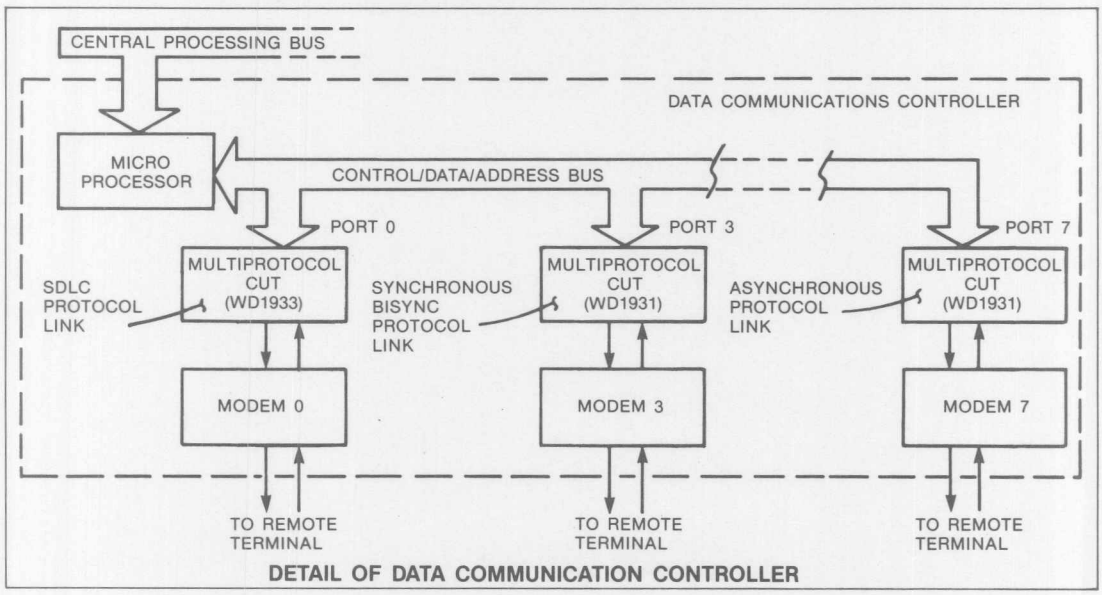
Table 4. WD1931 AC CHARACTERISTICS

T_A = 0°C to +70°C, V_{DD} = +12.0V ±0.6V, V_{SS} = 0V, V_{CC} = +5.0 ±0.25V

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNITS	CONDITIONS
T_{HLD}	$\overline{A0}$, $\overline{A1}$ & $\overline{CS}$ Hold Time	5			ns	
T_{CS}	$\overline{A0}$, $\overline{A1}$ & $\overline{CS}$ Width	495			ns	
T_{SET}	$\overline{A0}$, $\overline{A1}$ & $\overline{CS}$ Set-Up time	240			ns	
T_{CYCLE}	Cycle Time	1000			ns	
T_{MR}	$\overline{MR}$ Pulse Width	450			ns	
READ						
T_{RE}	$\overline{RE}$ Width	250			ns	
T_{DACC}	Data Access from $\overline{RE}$			300	ns	CL = 25 pf
T_{DOH}	Data Hold from $\overline{RE}$	50		150	ns	CL = 25 pf
WRITE						
T_{WE}	$\overline{WE}$ Width	250			ns	
T_{DS}	Data Set-Up Time	250			ns	
T_{DH}	Data Hold Time	100			ns	



DATA COMMUNICATIONS SYSTEMS FOR STOCK BROKERAGE FIRM



DETAIL OF DATA COMMUNICATION CONTROLLER

DIGITAL COMMUNICATIONS SYSTEM

The diagrams above illustrate a typical digital system employing several processing levels and digital protocols. It is flexible enough to satisfy several applications. For example. the host processor and remote terminals could be located respectively in airline reservation offices and ticket counters, travel centers and travel agencies, central bank offices and branch banks, or department stores and individual cash registers. The exploded diagram of the Data-Communications Controller exemplifies the use of one common circuit board design with eight multi-protocol circuits. When the Port requires a character-oriented protocol (synchronous, asynchronous, or synchronous-bisync), the WD1931 is plugged into the appropriate socket. For SDLC, HDLC or ADCCP, the WD193X is used.

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WESTERN DIGITAL
CORPORATION

WD1933/1935
Synchronous Data Link Controller

FEATURES

- HDLC, SDLC, ADCCP AND CCITT X.25 COMPATIBLE
- SDLC LOOP DATA LINK CAPABILITY
- FULL OR HALF DUPLEX OPERATION
- DC TO 2.0 MBITS/SEC DATA RATE
- PROGRAMMABLE/AUTOMATIC FCS (CRC) GENERATION AND CHECKING
- PROGRAMMABLE NRZI ENCODE/DECODE
- FULL SET OF MODEM CONTROL SIGNALS
- DIGITAL PHASE LOCKED LOOP
- FULLY COMPATIBLE WITH MOST CPU'S
- MINIMUM CPU OVERHEAD
- ASYNCHRONOUS/SYNCHRONOUS MULTI-PROTOCOL BOARD CAPABILITY (PIN COMPATIBLE WITH WD 1931)
- FULLY TTL COMPATIBLE
- SINGLE +5V SUPPLY
- ERROR DETECTION: CRC, UNDERRUN, OVERRUN, ABORTED OR INVALID FRAME ERRORS
- STRAIGHT FORWARD CPU INTERRUPTS
- PROGRAMMABLE MODEM CONTROL INTERRUPTS
- DOUBLE BUFFERING OF DATA
- DMA COMPATABILITY
- END OF BLOCK OPTION
- VARIABLE CHARACTER LENGTH (5, 6, 7 OR 8 BITS)
- RESIDUAL CHARACTER CAPABILITY
- ADDRESS COMPARE
- GLOBAL ADDRESS RECOGNITION
- EXTENDABLE ADDRESS FIELD
- EXTENDABLE CONTROL FIELD
- AUTOMATIC ZERO INSERTION AND DELETION
- MAINTENANCE MODE FOR SELF-TESTING

APPLICATIONS

COMPUTER COMMUNICATIONS

TERMINAL COMMUNICATIONS

COMPUTER TO MODEM INTERFACING

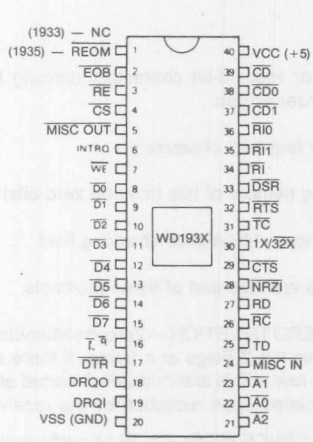


Figure 1. WD193X

PIN DESIGNATION

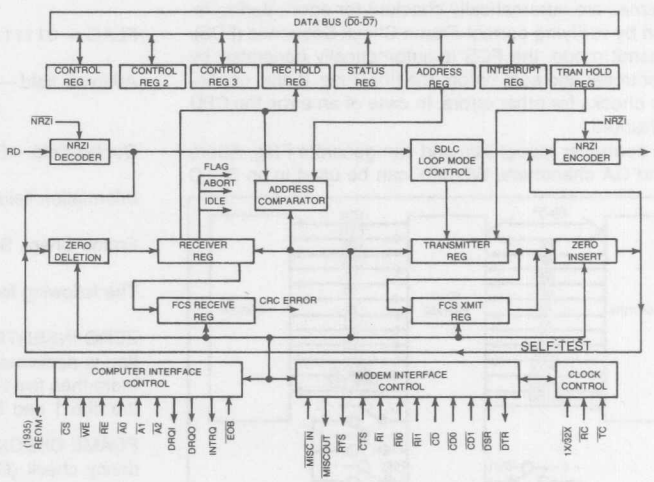


Figure 2. WD193X BLOCK DIAGRAM

LINE CONTROLLERS
FRONT END COMMUNICATIONS
NETWORK PROCESSORS
TELECOMMUNICATION SWITCHING NETWORKS
MESSAGE SWITCHING
PACKET SWITCHING
MULTIPLEXING SYSTEMS
DATA CONCENTRATOR SYSTEMS
SDLC LOOP DATA LINK SYSTEMS
DMA APPLICATIONS
COMMUNICATION TEST EQUIPMENT
LOCAL NETWORKS
MULTIDROP LINE SYSTEMS

The WD193X is a MOS/LSI microcomputer peripheral device which performs the functioning of interfacing a parallel digital system to a synchronous serial data communication channel employing ISO's HDLC, IBM's SDLC or ANSI's ADCCP line protocol. These protocols are referred to as Bit-Oriented Protocols (BOP).

The chip is fabricated in N-channel depletion load MOS technology and is TTL compatible on all inputs and outputs. This controller requires a minimum of CPU software by supporting a comprehensive frame-level instruction set and by hardware implementation of the low level tasks associated with frame assembly/disassembly and data integrity. It can be programmed to encode/decode NRZI data. The internal clock is then derived from the NRZI data using a digital phase locked loop.

The receiver and transmitter logic operates as two total independent sections with a minimum of common logic. The frames are automatically checked for errors during reception by verifying correct Frame Check Sequence (FCS). In transmit mode, the FCS is automatically generated by this controller and sent before the final Flag. It also continuously checks for other errors. In case of an error, the CPU is interrupted.

The controller recognizes and can generate Flag, Abort, Idle and GA characters. WD193X can be used in an SDLC Loop configuration. An End of Block option is supplied to minimize CPU time. A full set of modem control signals are supplied to minimize external hardware.

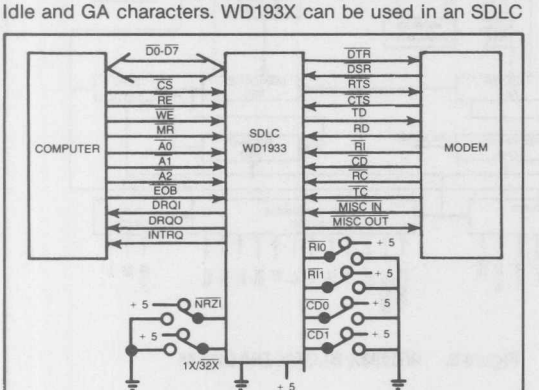


Figure 3. WD193X TYPICAL SYSTEM INTERFACE

A BRIEF DESCRIPTION OF HDLC, SDLC AND ADCCP PROTOCOLS

The WD193X is compatible with HDLC, SDLC and ADCCP standard communication Link Protocols. These are bit-oriented, code independent, and ideal for full duplex communication. A single communication element is called a FRAME, which can be used for both link control and data transfer purposes.

The elements of a frame are the beginning eight bit FLAG (F) consisting of one logical "0," six 1's and a 0, an eight bit ADDRESS-FIELD(A), an eight bit CONTROL-FIELD (C), a variable (N bits) INFORMATION-FIELD, a sixteen bit FRAME-CHECK-SEQUENCE (FCS), and an eight bit end FLAG (F), having the same bit-pattern as the beginning flag.

In HDLC, the address (A) and control (C) characters are extendable (more than one character). An important characteristic of a frame is that its contents are made code transparent by use of a zero bit insertion and deletion technique. Thus, the user can adapt any format or code suitable for his system. The frame is bit-oriented, meaning that, bits not characters in each field have specific meanings. The Frame Check Sequence (FCS) is an error detection scheme similar to the Cyclic Redundancy Checkword (CRC) widely used in magnetic disk storage devices. The frame format is shown in Figure 4.

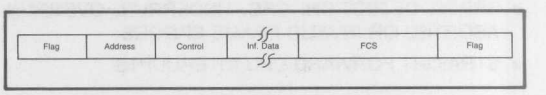


Figure 4. WD193X SDLC/HDLC/ADCCP FRAME FORMAT

Where:

FLAG = 01111110

Address field—One or more 8-bit characters defining the particular station

Control field—One or two 8-bit characters

Information field—Any number of bits (may be zero bits)

Frame Check Sequence—16-bit error checking field

The following features are also part of these protocols.

ZERO INSERTION/ZERO DELETION—Zero insertion/deletion is performed within the 2 Flags of a frame. If there are more than five 1's in a row, a 0 is automatically inserted after the fifth 1 and it is deleted upon reception by the receiver.

FRAME CHECK SEQUENCE (FCS)—A 16 bit cyclic redundancy check (CRC) calculation is performed during transmission of the data in between the 2 flags of the frame. The CRC is then transmitted after the I-field and before the final FLAG. Upon reception the receiver also performs a CRC calculation on the incoming data. If there were no transmission error, the Receiver CRC equals F0 B8 (hex).

DESCRIPTION OF PIN FUNCTIONS

The WD193X is packaged in a 40 pin DIP. The following is a functional description of each pin. A bar over a signal (SIGNAL), means active Low.

Table 1. DESCRIPTION OF WD193X PIN FUNCTIONS

PIN NUMBER	PIN NAME	SYMBOL	FUNCTION
1	No Connect	NC	WD1933 No Connection Allowed
	Received End of Message	$\overline{REOM}$	Received End of Message with no Errors. Output on WD1935.
2	End of Block	$\overline{EOB}$	This input, when low, function as an FCS command. Is independent of $\overline{CS}$.
3	Read Enable	$\overline{RE}$	This input, when low (and $\overline{CS}$ is active), gates the content of addressed register onto the Data bus.
4	Chip Select	$\overline{CS}$	This input, when low, selects the WD193X for a read or write operation to/from the Data bus.
5	Misc Output	$\overline{MISC\ OUT}$	This output is an extra programmable output signal for the convenience of the user. Is controlled by the CR10 bit.
6	Interrupt Request	INTRQ	This output is high whenever any of the interrupt register bits IR7-IR3 are set.
7	Write Enable	$\overline{WE}$	This input when low (and $\overline{CS}$ is active), gates the content of the Data bus into the addressed register.
8–15	Data Bus	$\overline{D0}$–$\overline{D7}$	Bidirectional three-state Data Bus. Bit 7 is MSB.
16	Master Reset	$\overline{MR}$	This input, when low, initializes all the registers, and forces the WD193X into an idle state. The WD193X will remain idle until a command is issued by the CPU.
17	Data Terminal Ready	$\overline{DTR}$	Modem Control Signal. This output when low, indicates to the Data Communication Equipment (DCE) that the WD193X is ready to transmit or receive data.
18	Data Request Output	DRQO	This output, when high, indicates that the Transmitter Holding Register (THR) is empty and ready to receive a data character from the Data bus for a transmit operation.
19	Data Request Input	DRQI	This output, when high, indicates that Receiver Holding Register (RHR) contains a newly received data character, available to be read onto the Data bus.
20	V_{SS}	V_{SS}	Ground
21,22,23	ADDRESS	$\overline{A2}$, $\overline{A0}$, $\overline{A1}$	These inputs are used to address the CPU interface registers for read/write operations.
24	Misc Input	$\overline{MISC\ IN}$	This input is an extra input signal for the convenience of the user. The state is shown by the SR4 bit.
25	Transmitted Data	TD	This output transmits the serial data to the Data Communications Equipment/Channel.
26	Receive Clock	$\overline{RC}$	This input is used to synchronize the received data.
27	Received Data	RD	This input receives the serial data from the Data Communication Equipment/Channel.
28	NRZI	$\overline{NRZI}$	This input, when low, sets the WD193X in NRZI mode.
29	Clear to Send	$\overline{CTS}$	Modem Control Signal. This input when low, indicates that the DCE is ready to accept data from the WD193X.
30	DPLL Select	1X/$\overline{32X}$	This input controls the internal clock. When high (1X clock), the external clock has the same frequency as the internal clock. When low (32X clock), the external clock is 32 times faster than the internal clock and the DPLL Logic is enabled.
31	Transmit Clock	$\overline{TC}$	This input is used to synchronize the transmitted data.

Table 1. DESCRIPTION OF WD193X PIN FUNCTIONS (Continued)

PIN NUMBER	PIN NAME	SYMBOL	FUNCTION
32	Request to Send	$\overline{RTS}$	Modem Control Signal. This output, when low, indicates to the DCE that the WD193X is ready to transmit data.
33	Data Set Ready	$\overline{DSR}$	Modem Control Signal. This input, when low, indicates that the DCE is ready to receive or transmit data.
34	Ring Indicator	$\overline{RI}$	Modem Control Signal. This input, when low, indicates a ringing signal being received on the communication channel.
35,36	Ring Indicator Interrupt Control	$\overline{RI1}$, $\overline{RI0}$	These inputs are used to program Ring Indicator interrupts.
37,38	Carrier Detect Interrupt Control	$\overline{CD1}$, $\overline{CD0}$	These inputs are used to program Carrier Detect Interrupts.
39	Carrier Detect	$\overline{CD}$	Modem Control Signal. This input, when low, indicates there is a carrier signal received by the local DCE from a distant DCE.
40	V_{CC}	V_{CC}	+5VDC

Table 2. WD193X TERMINOLOGY

TERMINOLOGY

TERM	DEFINITION/DESCRIPTION
BOP	Bit-oriented protocols: SDLC, HDLC, and ADCCP
ABORT	11111111 (seven or more contiguous 1's)
GA	Go-ahead pattern. 01111111 (0(LSB) followed by seven 1's)
LSB	First transmitted bit and first received bit. (Least significant bit)
MSB	Last transmitted bit and last received bit. (Most significant bit)
IDLE	11111111 11111111 (15 or more contiguous 1's)
FLAG	01111110. Starts and ends a Frame.
A-FIELD	Address-field in the Frame. Consists of one or more 8-bit characters. Defines the address of a particular station.
C-FIELD	Control field in the Frame. Consists of one or two 8-bit characters.
I-FIELD	Information field in the Frame. Consists of any number of bits.
FCS	Frame Check Sequence. A 16-bit error checking field sequence.
FRAME	A communication element, consisting of a minimum of 32 bits, and delimited by FLAGS.
GLOBAL ADDRESS	An A-field character of eight 1's. When this is compared and matched in the Address comparator, the DRQI will be set, indicating a valid address
RESIDUAL CHARACTER	The last I-field character, consisting of a lesser amount of bits than the other I-field characters in the Frame.
DATA SET	Data Communication Equipment (DCE). May be a modem.
BIT TIME	Length in time of a serial data bit.

HARDWARE ORGANIZATION

The WD193X block diagram is illustrated in Figure 2 and described below.

CPU Interface Registers

All of these registers are addressable and to be read from and/or written into by the CPU via the Data bus. These are 8-bit registers and have to be enabled via Chip Select ($\overline{CS}$) before any data transfer can be done.

CONTROL REGISTER 1, 2, 3 (CR1, 2, 3) Operations are initiated by writing the appropriate commands into these registers. CR1 should be programmed last.

RECEIVER HOLDING REGISTER (RHR) When Data Request Input is set (DRQI=1), contains received assembled character.

ADDRESS REGISTER (AR) Contains the address of this WD1933, which is to be compared to the received address character (A-field).

INTERRUPT REGISTER (IR) Contains the cause of the current interrupt request.

TRANSMITTER HOLDING REGISTER (THR) Is to be loaded with the next in line character to be transmitted, when Data Request Output is set (DRQO=1).

STATUS REGISTER (SR) Contains the overall status of the WD193X plus some information of the last received frame.

Non-Addressable, Internal Registers

These registers are transparent to the user, but is mentioned in these data sheets to help the understanding of the WD193X

TRANSMITTER REGISTER (TR) This 8-bit register functions as a buffer between the THR and the TD output. It is loaded from the THR (if Data Command) with the next character to be transmitted. A FLAG character may also be loaded into this register under program control. This character is automatically shifted out to the Transmit Data output. When the last bit of the current transmitted character has left the TR register, a new character will be loaded into this register, setting DRQO (Data command) or INTRQ (Abort, Flag or FSC command). If at the time when only one bit remains left in the TR register, and the THR is not loaded or a new command is not programmed (Data command), an underrun error will occur.

RECEIVER REGISTER (RR) The received data is, via the Zero-Deletion logic shifted into this 8-bit register. The data is here assembled to a 5, 6, 7 or 8-bit character length and then, under the right conditions, parallel transferred to the RHR register.

FCS RECEIVE REGISTER AND FCS XMIT REGISTER The WD193X contains a 16-bit CRC check register (FCS REC. REG.) and a 16-bit CRC generation register (FCS XMIT REG.). The generating polynomial is:

$$G(X) = X^{16} + X^{12} + X^5 + 1$$

The transmitter and receiver initialize the remainder value to all ones before CRC accumulation starts. The data is multiplied by X^{16} and is divided by G(X). Inserted 0's are not included in the accumulation. Under program control, the complement called the frame check sequence (FCS) is sent with high order bit first.

Various Internal Circuits

ADDRESS COMPARATOR This 8-bit comparator is used to compare the contents of the Address Register with the first address character of the incoming frame. This feature is enabled by a bit in the Command Register. If enabled and there is a match, the received frame is valid and DRQIs are generated for every character received (including the A-field). If enabled and there is not a match or there is no Global Address, the received frame is discarded. If not enabled, all received frames are valid and DRQIs are generated.

ZERO INSERTION The transmitted data stream is continuously monitored by this logic. A zero is automatically inserted following five contiguous 1 bits anywhere between the beginning FLAG and the ending FLAG of a frame. The insertion of the zero bit thus applies to the contents of the Address, Control, Information Data, and the FCS field.

ZERO DELETION The received data stream is continuously monitored by this logic. Upon receiving five contiguous 1 bits, the sixth bit is inspected. If the sixth bit is a 0, it is automatically deleted from the data stream. If the sixth bit is a 1, the seventh bit inspected; if it is a 0, a FLAG is recognized; if it is a 1 an ABORT or GO AHEAD is recognized.

DATA BUS ($\overline{D7}$-$\overline{D0}$) This is an inverted 8-bit bidirectional data bus.

SDLC LOOP-MODE CONTROL This logic supervises the WD193X running in SDLC Loop mode. It monitors the received data for a GO-AHEAD pattern in the case when SDLC LOOP MODE bit (CR22) and ACT TRAN bit (CR16) are set. When GO-AHEAD pattern is received, this logic suspends the repeater function and initiates the transmitter function. For more details, see functional description of SDLC Loop Mode.

NRZI ENCODER/DECODER When this mode is selected, the NRZI Encoder encodes the "normal" transmitted data to NRZI formatted data and the NRZI Decoder decodes the received NRZI data to "normal" data.

A binary 1 for "normal data" is TD = high.

A binary 1 for NRZI data is TD = no change.

A binary 0 for "normal data" is TD = low.

A binary 0 for NRZI data is TD = change of state.

COMPUTER INTERFACE CONTROL This logic interfaces the CPU, to the WD193X. It supervises the read and write functions to the addressable registers, generates data requests and interrupts, decodes and initiates commands, monitors the status of WD193X etc.

MODEM INTERFACE CONTROL This logic interfaces and supervises the modem control signals to/from the WD193X. It provides both dedicated (EIA Standard) and user defined control functions.

CLOCK CONTROL This logic interfaces the transmit and receive clocks to the WD193X. It converts the external clocks to the necessary internal clocks.

FUNCTIONAL DESCRIPTION

SDLC Loop Mode

The diagram below shows an SDLC Loop Data Link System. WD193X can be used in any of these stations.

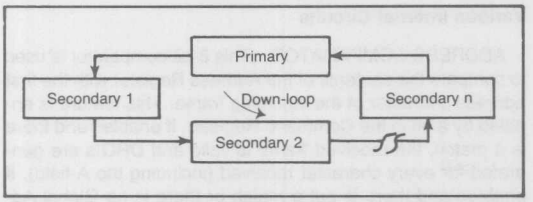


Figure 5. WD193X SDLC LOOP DATA LINK

Each secondary station is normally a repeater in Receive mode. The primary station is the loop controller. Signals sent out on the loop by the primary station are relayed from station to station, then back to the Primary. Any secondary station finding its address in the A-field captures the frame for action at that station. All received frames are relayed to the next station on the loop.

If a secondary station wants to transmit a message, it sets the ACT TRAN bit ($\overline{CTS}$ must be low) and waits for a GO AHEAD (GA) pattern. Until the GA pattern is received, this secondary station continues operating as a repeater. The primary station has the responsibility to generate the first GA pattern which can be accomplished by a flag followed by continuous 1's. The primary station must continue to send 1's until the GA has circulated through the entire loop. The first secondary station with its ACT TRAN bit set detects the GA and changes the last 1 bit of the GA pattern to a 0, thus generating the start flag of the frame it wants to transmit and preventing the GA pattern from propagating down the loop. The repeater function is then suspended by this secondary station and it goes into the transmit mode. When this secondary station completes its transmission frames, it resets the ACT TRAN bit and reverts back to the repeater mode. It repeats the 1's generated by the primary station to form another GA pattern from the final 0 of its ending flag. The GA pattern propagates through the loop until a secondary station down the loop, that wants to transmit (ACT TRAN bit is set), intercepts the GA pattern and starts to transmit as described, or until the primary station receives the idles (continuous 1's), indicating that the GA pattern has circulated through the entire loop. The primary station then generates another GA pattern or terminates its final data frame with continuous 1's.

Repeaters (Secondary stations) delay the received data by 4 bits (NRZ1 = 5 bits) before transmission.

The $\overline{RC}$ and $\overline{TC}$ clocks must be tied together. The internal DPLL will not function in the loop mode.

1X/32X Clock Option

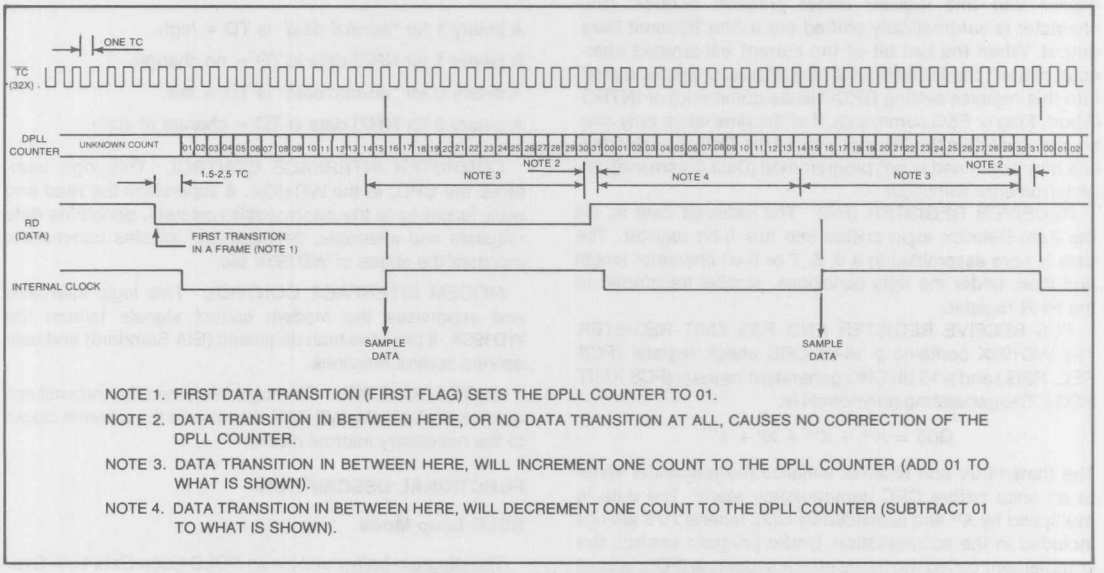
When 1X clock is selected, the data rate equals the external clock (receiver and transmitter).

When 32X clock is selected, the external clock rate is 32 times faster than the data rate.

Digital Phase Locked Loop (DPLL)

This feature is particularly useful in NRZI mode and/or when asynchronous modem is used. The purpose of the DPLL is to synchronize the internal 1X clock to the received data, thus insuring that this data is sampled in the middle of the incoming serial data bit. DPLL is automatically in operation when 32X clock is selected.

The DPLL Logic is initiated at the first received data transition in a frame. Corrections, if needed, are then made for each received data transition. A 32-counter is used for this operation. At the beginning of each frame and at the first received data transition, this 32 counter is reset. From this time on, the counter increments with one count for each external clock pulse. At count 16 the internal 1X clock is forced to change state to high (this transition = sampling time). At count 32, the counter resets itself. This forces the internal 1X clock again to change state back to low.



NOTE 1. FIRST DATA TRANSITION (FIRST FLAG) SETS THE DPLL COUNTER TO 01.

NOTE 2. DATA TRANSITION IN BETWEEN HERE, OR NO DATA TRANSITION AT ALL, CAUSES NO CORRECTION OF THE DPLL COUNTER.

NOTE 3. DATA TRANSITION IN BETWEEN HERE, WILL INCREMENT ONE COUNT TO THE DPLL COUNTER (ADD 01 TO WHAT IS SHOWN).

NOTE 4. DATA TRANSITION IN BETWEEN HERE, WILL DECREMENT ONE COUNT TO THE DPLL COUNTER (SUBTRACT 01 TO WHAT IS SHOWN).

Figure 6. WD193X DPLL TIMING DIAGRAM

At each received data transition, if the internal clock and the received data is out of synchronization, a correction is automatically made by ± 1 external clock period. See DPLL Timing Diagram in Figure 6.

End Of Block (EOB)

This is an FCS command. The main purpose of EOB is to allow the user to initiate FCS and FLAG without the need of using extra computer time. This is particularly practical in DMA applications. At the end of a frame, when the last information data character has already been loaded into the THR and once again DRQO is set, either a regular FCS command is written into CR1 Register, or $\overline{EOB}$ is to be activated. At the end of FCS, when INTRQ is set (XMIT OPCOM), the $\overline{EOB}$ if activated is to be reset again.

Serial Data Synchronization

The serial data is synchronized by the externally supplied Transmit Clock ($\overline{TC}$) and Receive Clock ($\overline{RC}$). When 1X clock is selected, the falling edge of $\overline{TC}$ generates new transmitted data and the rising edge of $\overline{RC}$ is used to sample the received data. When 32X clock is selected, a 32-counter (in the DPLL Logic) is used to synchronize the internal clock. At time 0, when the counter is reset to 0, the new transmitted data is generated. At time 16 (counter = 16) the received data is sampled, insuring that sampling is done in the middle of the received serial data bit. At count 32, the counter is reset to 0 again.

Self Test (Diagnostic) Mode

This feature is a programmable Loop back of data, enabling the user to make a complete test of the WD1933 with a minimum of external circuitry. In this mode, transmitted data to the TD pin, is internally routed to the received data input circuitry, thus allowing a CPU to send a message to itself to verify proper operation of the WD193X. The modem control signals $\overline{DTR}$ and $\overline{RTS}$ are deactivated (off) to insure no interference to/from the Data Communication Equipment (DCE). $\overline{DSR}$ and $\overline{CTS}$ are internally activated for proper input conditions. $\overline{TC}$ and $\overline{RC}$ should be supplied by the same source if 1X clock is selected.

Auto Flag

If this is selected and Data Command is executed, continuous Flags will be sent between frames. This eliminates the need to execute the Flag Command. In DMA applications in particular, this is very practical.

Extended Addressing

This type of addressing means, that there is more than one address character in the A-field. In receive mode, the first address character is compared in the Address Comparator of the WD193X. The other address character/s is to be compared by the CPU. The last address character is recognized by the fact that the LSB (bit 2^0) is a 1.

PROGRAMMING

Controlling Operation

Prior to initiating data transmission or reception, CONTROL REGISTER 1-3 (CR1-3) must be loaded with control information from the CPU. The contents of these registers will configure the WD193X for the user's specific data communication environment. These registers should be loaded during power-on initialization and after a reset operation. They can be changed at any time that the respective transmitter or receiver is deactivated. The CR1-3 dictate what the transmitter will send: the type of character (DATA, ABORT, FLAG or FCS), the number of bits per character, and the number of bits in the residual character. Similarly, they tell the receiver the types of frames to look for: the number of bits per I-field character, whether to perform an address compare, and whether to watch for an extended address. The Control Register also control Data Terminal Ready ($\overline{DTR}$), $\overline{Misc\ Out}$ and the activation of both the transmitter and the receiver. For more detailed information, see Register Formats.

Monitoring Operation

Monitoring is done by use of the Interrupt Register (IR) and Status Register (SR). The IR register indicates when a frame is completed (transmitted or received), if there was an error and if there is a Data Set Change. It also monitors the states of INTRQ, DRQO and DRQI.

The SR register indicates if an error is recognized by IR, what type of error. It also monitors the modem control signals; Ring Indicator ($\overline{RI}$), Carrier Detect ($\overline{CD}$), Data Set Ready ($\overline{DSR}$) and $\overline{Misc\ In}$.

Furthermore, the SR register monitors if the Receiver is idle, and also if in receive mode if the user has programmed the Receiver Character Length to be 8 bits per character, this register indicates the number of residual bits received. For more detailed information, see Register Formats.

Read/Write Control Of CPU Interface Registers

These registers are directly accessible from the CPU bus ($\overline{D7}$-$\overline{D0}$) by a read and/or write operation by the CPU.

The CPU must set up the WD193X register address ($\overline{A2}$-$\overline{A0}$), Chip Select ($\overline{CS}$), Write Enable ($\overline{WE}$) or Read Enable ($\overline{RE}$) before each data bus transfer operation.

During a write operation, the falling edge of $\overline{WE}$ will initiate a WD193X write cycle. The addressed register will then be loaded with the content of the Data Bus ($\overline{D7}$-$\overline{D0}$). During a read operation, the falling edge of $\overline{RE}$ will initiate a WD193X read cycle. The addressed register will then place its content

onto the Data Bus ($\overline{D7}$-$\overline{D0}$). The read/write operation is completed, when $\overline{CS}$ or $\overline{RE}/\overline{WE}$ is brought high.

For more detailed information, timing, etc., see Read/Write Timing diagram.

For read and write operation, the CR1-3 registers normally need no external clock. After reset of CR1-3, $\overline{TC}$ clock is required. The AR and THR registers need no external clock, and can only be written into. The RHR, IR and SR registers need Transmit Clock ($\overline{TC}$) or Receive Clock ($\overline{RC}$) to set various bits, and are read-only.

All these registers will get initialized by a Master Reset. A read operation of RHR resets the DRQI. A write operation to THR, resets the DRQO. A read operation of IR, resets IR bits 0 and 3-7. A read operation of SR, resets SR bits 0-2.

For addressing and external clocks needed, see figure below.

$\overline{CS}$	$\overline{A2}$	$\overline{A1}$	$\overline{A0}$	Read	Write	External Clock
L	H	H	H	CR1	CR1	None*
L	H	H	L	CR2	CR2	None*
L	H	L	H	CR3	CR3	None*
L	H	L	L	RHR	AR	RHR=$\overline{RC}$. AR=None
L	L	H	H	IR	THR	IR=$\overline{TC}$. THR=None
L	L	H	L	SR	—	SR0-3=$\overline{RC}$. SR4-7=None.
H	X	X	X	X	X	

L = V_{IL} at pins
H = V_{IH} at pins
X = Don't care

*2.5 $\overline{TC}$ clock cycles are required after a Master Reset to be able to read and write.

REGISTER FORMATS

Below shows a short form register format.

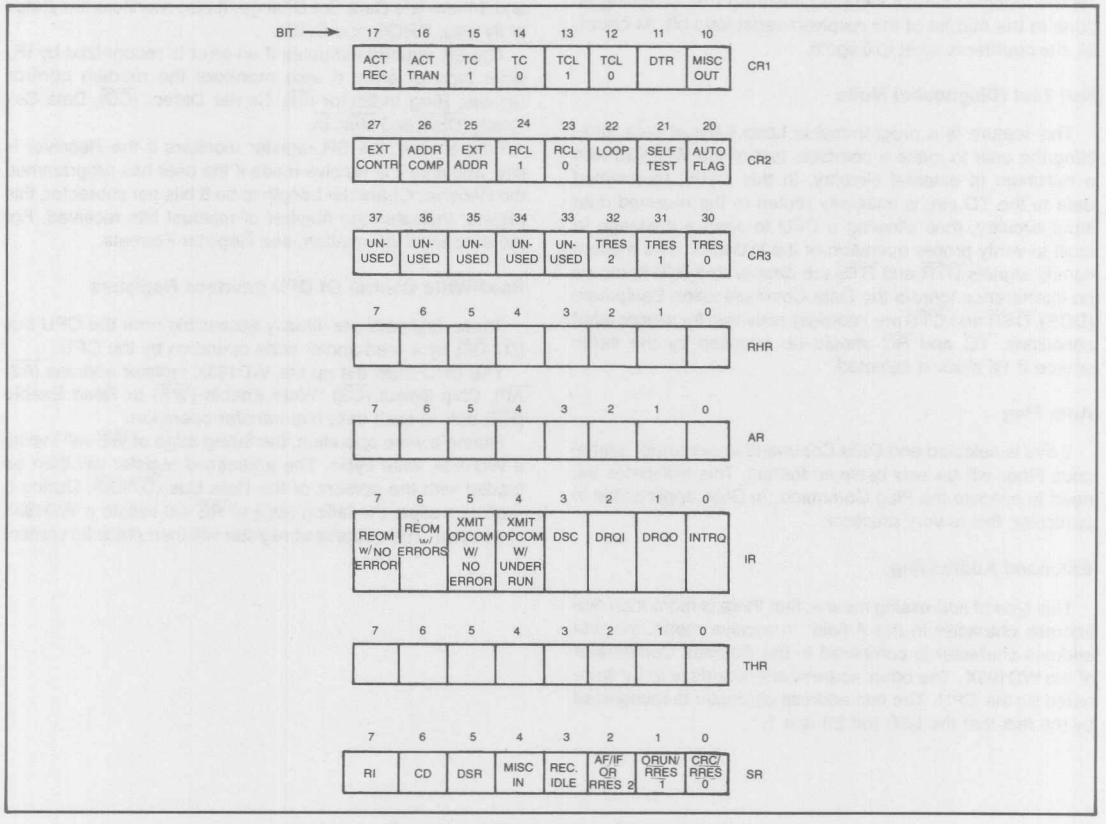


Figure 7. WD193X BIT ASSIGNMENTS

A more detailed description is shown here of each bit location. It should be known, that because the Data Bus Lines ($\overline{D7}$-$\overline{D0}$) has inverted logic, a logic 1 (set) means low state. Also, a modem control signal which is inverted (example $\overline{DTR}$), is in on-state (set) when low.

Control Register 1 (CR1)

When initiating a transmit/receive operation, this should be the last register programmed.

Miscellaneous Output (CR10) This bit controls the Miscellaneous Output signal to the data set. When CR10 is a logical 0, $\overline{Misc\ Out}$ is off, when it is a logical 1, $\overline{Misc\ Out}$ is on.

DTR Command (CR11) This bit controls the data Terminal Ready ($\overline{DTR}$) signal to the data set. When CR11 is a logical 0, $\overline{DTR}$ is off. When CR11 is a logical 1, $\overline{DTR}$ is on. When the Self-Test mode is selected, $\overline{DTR}$ signal is forced to an off state.

Transmitter Character Length (CR13, 12) These bits control the transmitted I-field data character length. The data character may be 5, 6, 7 or 8 bits long.

CR13 (TCL1)	CR12 (TCL0)	Bits Per Character
0	0	8
0	1	7
1	0	6
1	1	5

Transmitter Commands (CR15, 14) These bits control the transmission of DATA (A-field, C-field and I-field), ABORT, FLAG, and FCS (FCS plus FLAG). When these commands are programmed, the previous command currently still in progress, will complete the transmission of its character. When this is done, a new character generated by this new command, will be transmitted.

If DATA is programmed, the new character to be transmitted will be the character loaded (or still to be loaded) in the THR register. If ABORT is programmed, the new character will be eight logical 1's. If FLAG is programmed, the new character will be 01111110. If FCS is programmed, three new characters will be transmitted; first the 16-bit content of the FCS XMIT REGISTER, then a FLAG. One serial data bit time ahead of the first bit (LSB) of this new character (= FLAG character when FCS command) being transmitted, the CPU is signalled that the WD193X is again ready to receive a new command. This signal is an INTRQ (XMIT OPCOM), if the now current command is ABORT, FLAG or FCS. This signal is a DRQO, if the current command is DATA. However, in this latter case (DATA), the user has two choices; 1. Change the command. 2. Keep the DATA command and load a new character into the THR register. For more information, please see the Transmission Timing diagram, Figure 8.

Programming, see figure below.

Activate Transmitter (CR 16) This bit when set, enables the transmitter and sets $\overline{RTS}$ signal. If in SDLC Loop Mode (CR22 = set), the transmitter waits for a Go-Ahead pattern before the transmitter is enabled.

Activate Receiver (CR 17) This bit when set activates the receiver, which begins shifting in frames one character at a time into RR register for inspection.

CONTROL REGISTER 2 (CR2)

Auto Flag (CR20) When set, Flags (without INTRQs) will be continuously transmitted in between frames, when otherwise the transmitter would be in idle state.

Self-Test Mode (CR21) When set, the Transmitter Data Output is internally connected to the Receiver Data input circuitry. The modem control output signals are deactivated (off state). The modem control input signals are internally activated. This mode allows off-line diagnostic.

SDLC Loop Mode (CR22) When set, the WD193X is conditioned to operate in an SDLC Loop Data Link system (see SDLC Loop Mode).

Receiver Character Length (CR24, 23) These bits indicate to the receiver how many bits per character there are to assemble for the I-field. The I-field characters may be 5, 6, 7 or 8 bits long. The unused bits read from RHR will be logical 0.

CR24 (RCL1)	CR23 (RCL0)	Bits Per Character
0	0	8
0	1	7
1	0	6
1	1	5

Extended Address (CR25) When set, this bit indicates to the receiver that there is more than one address character in the A-field. The receiver will expect another address character if the LSB in the current address character is a logical 0. The purpose of this bit: If a non-8-bit I-field character length is expected, the DRQIs will get out of synchronization if the WD193X does not know exactly when the I-field will start. Not used in transmit mode.

Address Compare (CR26) When set, the first address character will be inspected in the Address Comparator. If there is a match with the AR register, or if the address compared is a Global Address (eight 1's) the frame is considered valid, causing DRQIs to be generated. Otherwise, the receiver does not react, and will continue comparing for a new valid address. If not set, all frames are considered valid.

Extended Control (CR27) When set, indicates that there are two control characters per frame. If not set, there is only one control character per frame. The purpose of this bit: If a non-8-bit I-field character length is to be received, the DRQIs will get out of synchronization if the WD193X does not know when the I-field will start. Not used in transmit mode.

CR15 (TC1)	CR14 (TC0)	Command	Character/s Transmitted	Signal to CPU
0	0	DATA	Content of THR	DRQO
0	1	ABORT	1111 1111	INTRQ
1	0	FLAG	0111 1110	INTRQ
1	1	FCS	FCS + 01111110	INTRQ

CR32 (TRES 2)	CR31 (TRES 1)	CR30 (TRES 0)	Residual Char. Length
0	0	0	No residual char. sent
0	0	1	1 bit
0	1	0	2 bits
0	1	1	3 bits
1	0	0	4 bits
1	0	1	5 bits
1	1	0	6 bits
1	1	1	7 bits

CONTROL REGISTER (CR3)

***Transmit Residual Character Length (CR32, 31, 30)** These bits inform the transmitter what bit-length the residual character will be. If no residual character is to be sent, these bits must be set to logical 0.

Unused (CR33-37) These bits are not used, and are always a logical 0.

INTERRUPT REGISTER (IR)

This register contains the information why an interrupt (INTRQ) was generated. An IR register read operation, will reset bits 0, and 3-7.

Loading the THR register, will reset DRQO (bit 1). Reading the RHR register, will reset DRQI (bit 2). A new interrupt will occur if one is pending.

If a new interrupt is generated while the CPU is reading the IR register, this new interrupt will set the respective bit in the IR register one bit time later (this to avoid losing any interrupt). The status of bits 3–7 will accumulate until the IR register is read by CPU.

INTRQ (IR0) When set, indicates an interrupt and that there are one or more bits set in positions 3 through 7 of this register. This bit is a mirror image of INTRQ signal (pin 6).

When pin 6 (INTRQ) is not used for pending interrupts information and only the IR register is read to obtain the status of the interrupt bits (polling method), a minimum of two (2) bits times must be allowed between IR registers "read's" to insure an orderly flow of pending interrupts.

DRQO (IR1) When set, indicates a Data request output. This bit is a mirror image of DRQO signal (pin 18).

DRQI (IR2) When set, indicates a Data Request input. This bit is a mirror image of DRQI signal (pin 19).

Data Set Change (IR3) When set, indicates a change of state of the Data Set (Data Communication Equipment). This is a change of state of $\overline{DSR}$, $\overline{CD}$ or $\overline{RI}$. The type of change of $\overline{CD}$ and $\overline{RI}$ that this bit will react to, is programmed by use of input signals $\overline{CD1}/\overline{CD0}$ and $\overline{RI1}/\overline{RI0}$ and is shown below.

XMIT Operation Complete with Underrun Error (IR4) When set, indicates that the transmitter command has been completed and there was an Underrun error. An Underrun error occurs when the Data Request Output (DRQO) is set, but THR register is not loaded in time.

XMIT Operation with No Error (IR5) When set, indicates that the transmitter command has been completed and there was no error.

Received End of Message With Errors (IR6) When set, indicates that a Received End of Message is detected, and there was an error. Errors include CRC, Overrun, Invalid Frame and Aborted Frame.

The SR Register bits 0–2 will indicate the exact type of error.

Received End Of Message With No Error (IR7) When set, indicates that a Received End of Message is detected, and there was no error.

$\overline{CD1}$	$\overline{CD0}$	Interrupting edge of $\overline{CD}$	$\overline{RI1}$	$\overline{RI0}$	Interrupting edge of $\overline{RI}$
LO	LO	Rising and falling	LO	LO	Rising and falling
LO	HI	Falling	LO	HI	Falling
HI	LO	Rising	HI	LO	Rising
HI	HI	None	HI	HI	None

STATUS REGISTER (SR)

This register contains the status of the receiver and some modem control signals. It also indicates (if REOM w/Errors) exactly what type of errors. If the Receiver Character Length is 8 bits, this register indicates the amount of Residual bits that was received. A read operation will reset bits 0–2.

Received Error/Received Residual Character Length (SR 2–0) If REOM w/NO ERROR (IR7) is set, and the Receiver, Character Length (CR24, 23) is 8 bits, these bits (SR 2-0), indicate the number of residual bits received.

If REOM WITH ERROR (IR 6) is set, these bits indicate the type of error that occurred, as shown in figure below.

Bit Set	Error
SR0	CRC
SR1	Overrun
SR2	Aborted or Invalid frame

Receiver Idle (SR 3) When set, indicates that the receiver is currently IDLE.

Miscellaneous Input (SR4) This is a mirror image of $\overline{\text{MISC}}$ IN signal. When this signal is set, SR4 bit is set.

Data Set Ready (SR5) This is mirror image of $\overline{\text{DSR}}$ signal. When this signal is set, SR5 bit is set.

Carrier Detect (SR6) This is a mirror image of $\overline{\text{CD}}$ signal. When this signal is set, SR6 bit is set.

Ring Indicator (SR7) This is a mirror image of $\overline{\text{RI}}$ signal. When this signal is set, SR7 bit is set.

TRANSMITTER OPERATION

Prior to this operation, the programmable inputs and the transmit mode related register bits need to be programmed according to the user's specific data communications environment. The last bit to be set is always the ACT TRAN (CR16) bit.

Before this, the INTRQ has to be cleared, which can be done by reading the IR register. For more detailed information how to program the WD193X, see Programming.

As an example of how to program the WD193X, let's assume a 24-bit information is to be transmitted. The I-field would then consist of three 8-bit characters with no residual bits. CR3 should then be 00 (Hex).

If Auto Flag is selected, CR20 has to be set, CR21 and CR22 should be logical 0's, as this example is no Self-test and no SDLC Loop Mode.

Bits CR23-CR27 are for reception only (see Receiver Operation). The last register to be programmed is CR1. If MISC OUT is not used, this may be ignored. If a modem is used, DTR (CR11) is to be set. CR13 and CR12 should be logical 0's (8-bit char. length). CR15 and CR14 should be logical 0's (Data Command). ACT TRAN (CR16) bit is to be set. The ACT REC (CR17) is for reception only.

The DTR bit, when set, activates the $\overline{\text{DTR}}$ signal, indicating to the modem to prepare for communication. When the modem is ready, it sends back a Data Set Ready ($\overline{\text{DSR}}$) to the WD1933. This causes the DSC (IR3) bit to set, which in turn activates INTRQ. The IR register is now read. Simultaneously, when the ACT TRAN (CR16) bit is set, this activates the Request to Send ($\overline{\text{RTS}}$) signal, instructing the modem to enter into transmit mode. When the modem is ready to transmit data, it responds by activating the Clear to Send ($\overline{\text{CTS}}$) signal.

The WD193X is now conditioned to transmit. Now DRQO gets set, indicating to the CPU (or DMA) to load the first character (Address) into the THR. When this is done, DRQO will reset. As soon as the WD193X is ready to be loaded with the next character to be transmitted, DRQO is again set. When the THR register is again loaded with a character, DRQO will again reset.

This same sequence continues until the last I-field character to be transmitted is loaded into the THR. If CRC checking is to be used, the next time when DRQO is set, an FCS command has to be programmed. This is accomplished by either setting CR15, 14 to both logical 1's or by activating the $\overline{\text{EOB}}$ signal.

At the end of the FCS being transmitted, INTRQ will set indicating XMIT Operation Complete. The IR register is to be read to find out whether the frame was sent with or without error. Also the FCS Command which was used as described above has to be changed. If CR15, 14 were set, these have to be reset (to Data Command), or if $\overline{\text{EOB}}$ was activated, this signal has to be deactivated. At this same time, the ACT TRAN bit is allowed to be reset, causing the TD output to go idle after the end Flag is sent. If the ACT TRAN bit is kept set, continuous Flags will be sent following the FCS.

If a new frame is to be sent right after this first frame, only one Flag is needed in between frames, meaning the frames have one common Flag character. In this case, the second frame Address character may be loaded at the same time the FCS command is programmed during the first frame. Also, the ACT TRAN bit should be kept set in between frames. Every time DRQO gets set, the user must load the THR register before the last loaded character only has 1.5 bits left to be transmitted. In other words, when DRQO gets set, the user may wait (if 8-bit characters) up to 7.5 serial data bits before loading the THR. If THR is not loaded within this time, an Underrun error will occur.

If Auto Flag is not selected (CR20 = logical 0) the sequence will be a little different than described below. When the first DRQO is set, and after the Address character is loaded into THR, a Flag command is also programmed (CR15, 14 = 10).

This will set an interrupt (INTRQ), which indicates that the IR register must be read. Now, the Data Command is reprogrammed (CR15, 14 =00).

For more information, see Transmission Timing diagram.

ABORT CONDITIONS

The function of prematurely terminating a data link is called an "Abort." The transmitting station aborts by sending eight consecutive 1's. Unintentional Abort caused by 1's in the A-C- or I-field is prevented by zero insertion. Intentional Abort may be sent by programming an Abort command. Abort will also be sent in the case where THR is not loaded in time or FCS command is not programmed in time (= underrun). This means that after the DRQO is set, to avoid Abort; THR must be loaded, $\overline{\text{EOB}}$ activated or FCS command programmed before there is only 1.5 bits left of the last character to be transmitted.

If this is not done, INTRQ (XMIT OPCOM w/underrun) is set and Aborts are transmitted until, either the command is changed or the THR is loaded. If in this same case, Auto

Flag was programmed, one Abort (with INTRQ) would be generated, and thereafter continuous Flags (with no INTRQs) will be sent.

RECEIVER OPERATION

Prior to this operation, the programmable inputs and the receive mode related register bits have to be programmed according to the user's specific data communication environment. Also, the INTRQ has to be cleared. The last bit to be set is always the ACT REC (CR17) bit.

For more detailed information how to program the WD193X see Programming. As an example, let's assume a 26-bit information is to be received, and the I-field is made up by 8-bit characters. The CR3 register is only for transmit mode, and may be ignored here. CR20 and CR 12–16 bits are also for transmit mode only, and therefore may also be ignored. CR21 and CR22 are to be logical 0s (no Self-Test and no SDLC Loop Mode). CR24, 23 are to be logical 0's (8-bit character I-field). If only one A-field and one C-field character is expected, and this WD193X has a specific address, CR25 should be a logical 0, CR26 should be a 1, and CR27 should be a 0. The address to which the A-field should compare should be loaded into the AR register.

The status of the modem is monitored by the SR register, and it may be useful to read it at this time. CR1 is loaded as the last register. CR10 (Misc In) bit is optionable to the user. CR11 (DTR) is to be set if modem is used. CR17 (ACT REC) is now set, starting the input of frame characters into the Receiver Register (RR). When a Flag is detected, the next 8-bit character (address-character), when received, is compared to the character in the AR register. If these match, or if the received character is a Global address, this frame is valid, and the DRQI gets set. If the Address Comparator (CR26) bit is not set, all frames would be considered valid and generate DRQIs. When the RHR register is read, DRQI will be reset. All characters in a valid frame which are input into the RR register will set DRQI, and every time RHR is read by the CPU, DRQI will be reset.

During reception, the receiver also performs a CRC calculation on the incoming data. When the end Flag is received, INTRQ will get set, indicating Received End of Message. If the reception is completed with no error, IR7 (REOM w/no Error) bit will be set. When 8-bit characters are received SR 0-2 bits indicate the number of residual bits, in this case two. If IR6 (REOM w/Error) was set, SR 0-2 bits indicate the type of errors (see Receiver Error Indication).

When all characters including the A-field and the FCS-field are read, and when the REOM interrupt is recognized, it is up to the user to disassemble these mentioned characters from the received data. If non-8-bit characters are received, the amount of residual bits have to be calculated by the CPU after masking out the part of the ending Flag showing up in the last read character.

After end of frame, the receiver begins searching for a new frame.

For more information, see Reception Timing diagram.

RECEIVER ERROR INDICATION

When a frame is received, and REOM w/Error (IR6) is set, the type of error is indicated by the SR bits 0-2.

CRC Error (SR0) If the CRC calculation performed on the incoming data does not equal to F0B8 (HEX), this bit will be set.

Overrun Error (SR1) After DRQI is set, if the RHR is not read within one character minus one bit time, this bit will be set.

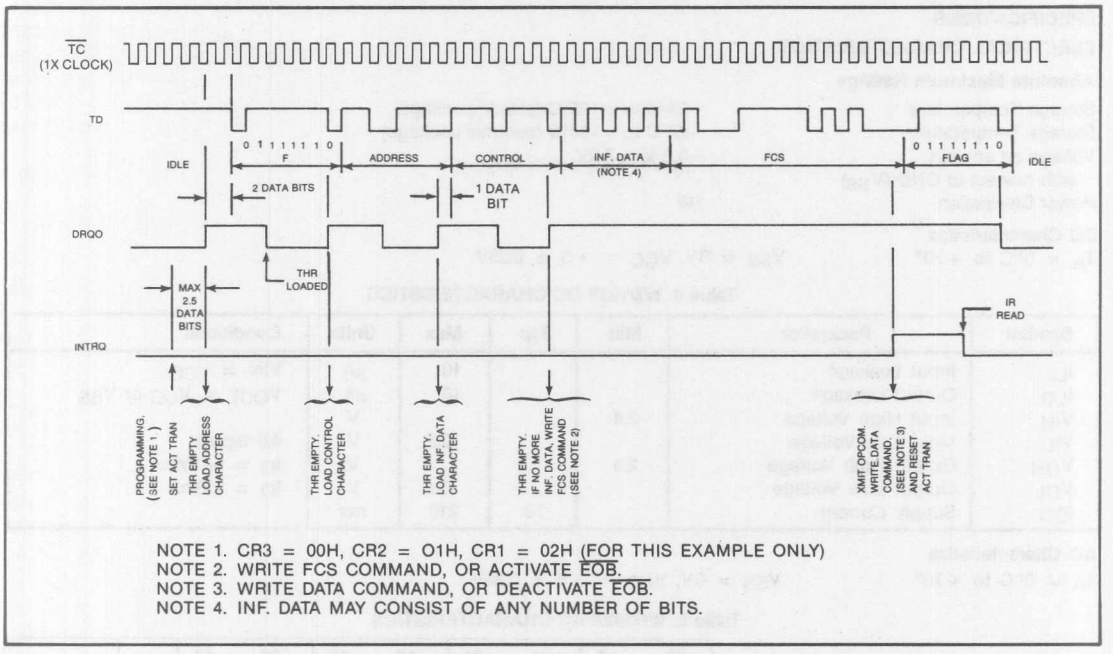
Aborted or Invalid Frame Error (SR2) If the frame is aborted or if in a frame the number of bits between flags are less than the required minimum (see Table 3), this bit will be set.

NOTES

1. TC-command—If two or more contiguous ABORTS or FLAGS are executed, the ACT TRAN (CR16) bit has to be reset before DATA-command can be executed.
2. Master Reset ($\overline{MR}$)—Needs no clock during activation of MR. However, 2.5 clock cycles are required to reset the WD193X after the falling edge of MR.
3. IR-register—Immediately when IR register is read, bit 0 will reset. Bits 3-7 are reset one bit time later.
4. SR-register—Bits 0-2 are reset one bit time after SR register is read.
5. SDLC Loop mode—Go-ahead pattern may be sent by either sending IDLE or ABORT after Flag.
6. $\overline{TC}$ and $\overline{RC}$ clocks are completely independent of each other.
7. It is recommended to verify that the INTRQ signal (pin 6) is set prior to reading the IR register.
8. End Of Block (EOB) — Minimum activated time must be one (1) character time. It can be activated indefinitely using IDDLE or AUTO FLAG (CR20).

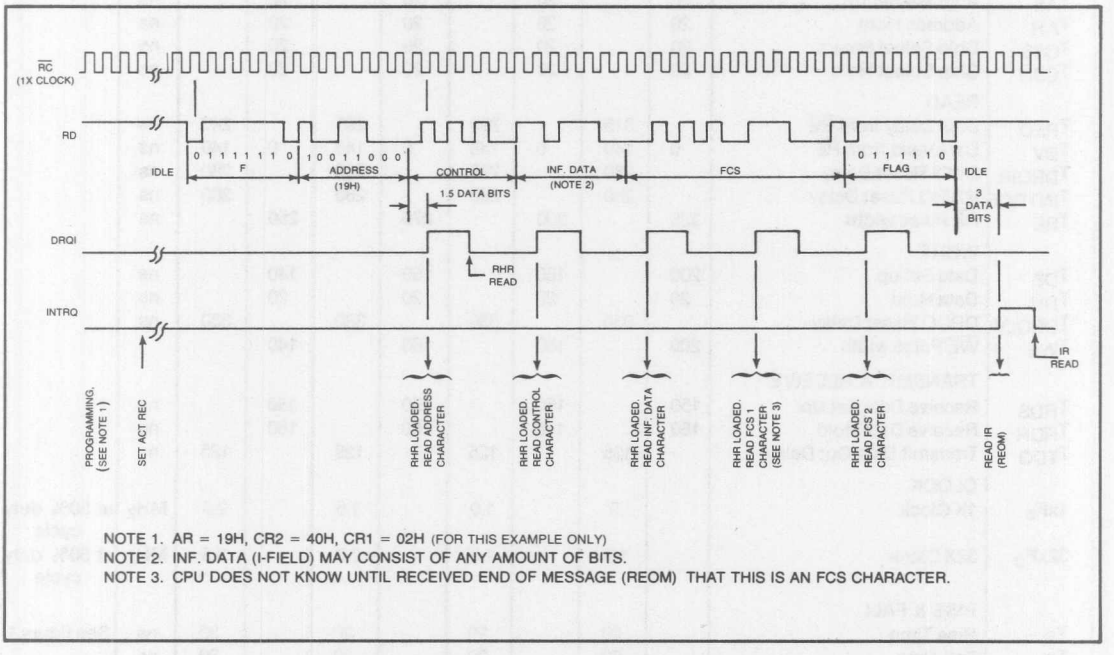
Table 3

	Valid Frame			
Receiver Programmed for	**8 bit char**	**7 bit char**	**6 bit char**	**5 bit char**
1 address, 1 control	≥25 bits	≥23 bits	≥21 bits	≥19 bits
2 addresses, 1 control 1 address, 2 controls	≥25 bits	≥24 bits	≥23 bits	≥22 bits
3 addresses, 1 control 2 addresses, 2 controls	≥25 bits	≥25 bits	≥25 bits	≥25 bits



NOTE 1. CR3 = 00H, CR2 = O1H, CR1 = 02H (FOR THIS EXAMPLE ONLY)
NOTE 2. WRITE FCS COMMAND, OR ACTIVATE $\overline{EOB}$.
NOTE 3. WRITE DATA COMMAND, OR DEACTIVATE $\overline{EOB}$.
NOTE 4. INF. DATA MAY CONSIST OF ANY NUMBER OF BITS.

Figure 8. WD193X TRANSMISSION TIMING DIAGRAM



NOTE 1. AR = 19H, CR2 = 40H, CR1 = 02H (FOR THIS EXAMPLE ONLY)
NOTE 2. INF. DATA (I-FIELD) MAY CONSIST OF ANY AMOUNT OF BITS.
NOTE 3. CPU DOES NOT KNOW UNTIL RECEIVED END OF MESSAGE (REOM) THAT THIS IS AN FCS CHARACTER.

Figure 9. WD193X RECEPTION TIMING DIAGRAM

SPECIFICATIONS

ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings

Storage Temperature	−55°C to +125°C (plastic package)
Storage Temperature	−65°C to +150°C (ceramic package)
Voltage on any pin with respect to GND (V_{SS})	−0.3 to +7.0V
Power Dissipation	1W

DC Characteristics

T_A = 0°C to +70° V_{SS} = 0V, V_{CC} = +5 ± 0.25V

Table 4. WD193X DC CHARACTERISTICS

Symbol	Parameter	Min	Typ	Max	Units	Conditions
I_{LI}	Input Leakage			10	μA	VIN = V_{CC}
I_{LO}	Output Leakage			10	μA	V_{OUT} = V_{CC} or V_{SS}
V_{IH}	Input High Voltage	2.4			V	
V_{IL}	Input Low Voltage			0.8	V	All Inputs
V_{OH}	Output High Voltage	2.4			V	I_O = −100μA
V_{OL}	Output Low Voltage			0.4	V	I_O = 1.6mA
I_{CC}	Supply Current		70	210	ma	

AC Characteristics

T_A = 0°C to +70° V_{SS} = 0V, V_{CC} = +5 ± 0.25V

Table 5. WD193X AC CHARACTERISTICS

		−00, −10		−01, −11		−02, −12		−03, −13			
Symbol	Parameter	Min	Max	Min	Max	Min	Max	Min	Max	Units	Conditions
	READ & WRITE										
T_{AS}	Address Set-Up	20		20		20		20		ns	
T_{AH}	Address Hold	20		20		20		20		ns	
T_{CSS}	Chip Select Set-up	20		20		20		20		ns	
T_{CSH}	Chip Select Hold	20		20		20		20		ns	
	READ										
T_{RED}	Data Delay from $\overline{RE}$		315		290		265		240	ns	
T_{DV}	Data Valid from $\overline{RE}$	0	140	0	140	0	140	0	140	ns	
T_{DRQIR}	DRQI Reset Delay		280		280		280		280	ns	
T_{INTRQR}	INTRQ Reset Delay		280		280		280		280	ns	
T_{RE}	$\overline{RE}$ Pulse width	325		300		275		250		ns	
	WRITE										
T_{DS}	Data Set-up	200		180		160		140		ns	
T_{DH}	Data Hold	20		20		20		20		ns	
T_{DRQOR}	DRQO Reset Delay		330		330		330		330	ns	
T_{WE}	$\overline{WE}$ Pulse width	200		180		160		140			
	TRANSMIT & RECEIVE										
T_{RDS}	Receive Data Set Up	150		150		150		150		ns	
T_{RDH}	Receive Data Hold	150		150		150		150		ns	
T_{TDO}	Transmit Data Out Delay		125		125		125		125	ns	
	CLOCK										
$1xF_C$	1X Clock		.5		1.0		1.5		2.0	MH_Z	at 50% duty cycle
$32xF_C$	32X Clock		1.0		1.5		2.0		2.5	MH_Z	at 50% duty cycle
	RISE & FALL										
T_R	Rise Time		20		20		20		20	ns	See figure 1
T_F	Fall Time		20		20		20		20	ns	

NOTE: All A.C. Timing Measurements made at 0.8V and 2.0V.

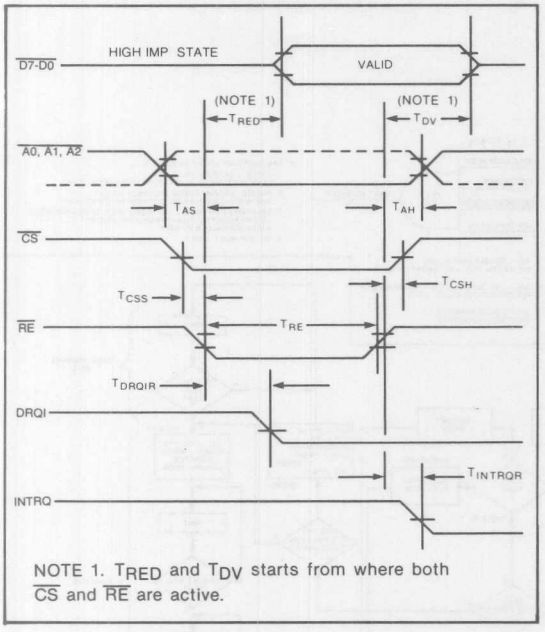


Figure 10. WD193X READ TIMING DIAGRAM

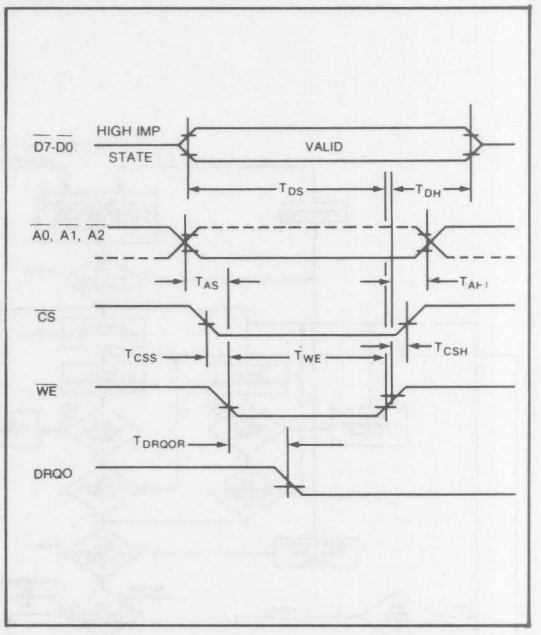


Figure 11. WD193X WRITE TIMING DIAGRAM

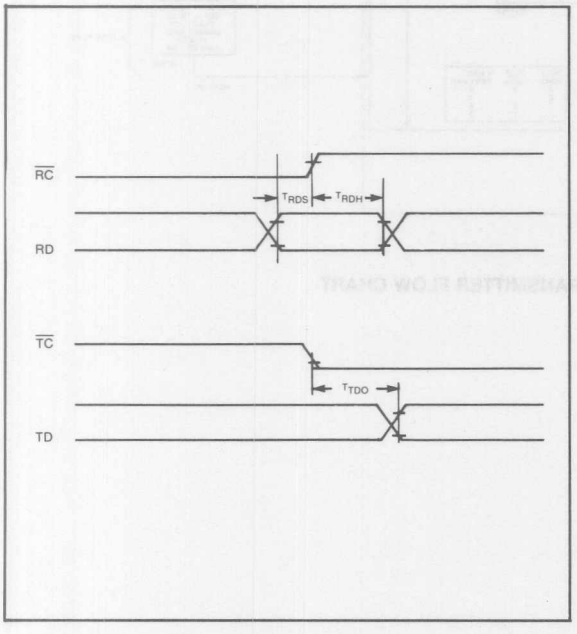


Figure 12. RECEIVER AND TRANSMITTER TIMING

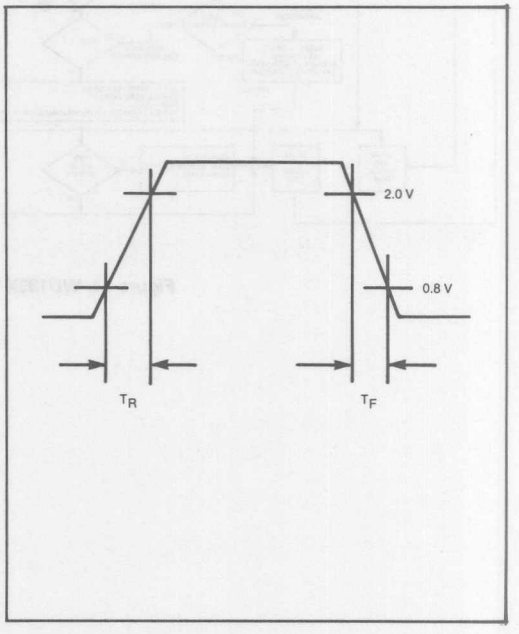


Figure 13. WD193X RISE AND FALL TIMING DIAGRAM

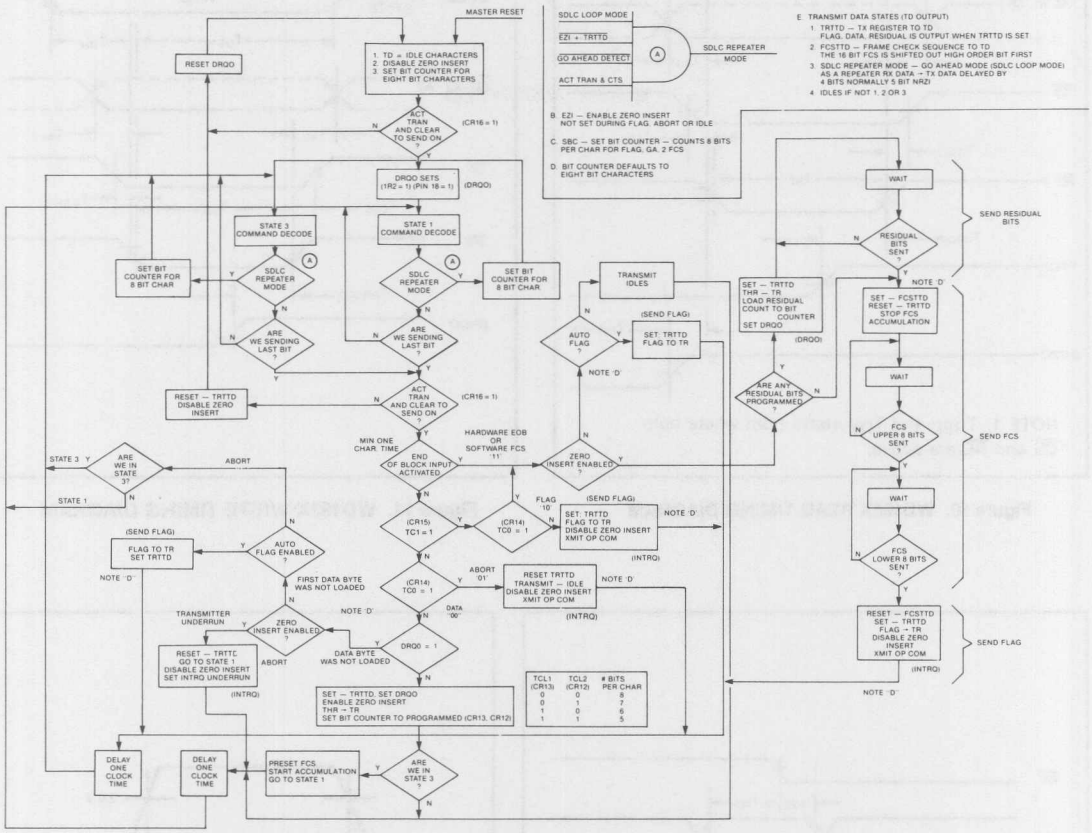


Figure 14. WD193X TRANSMITTER FLOW CHART

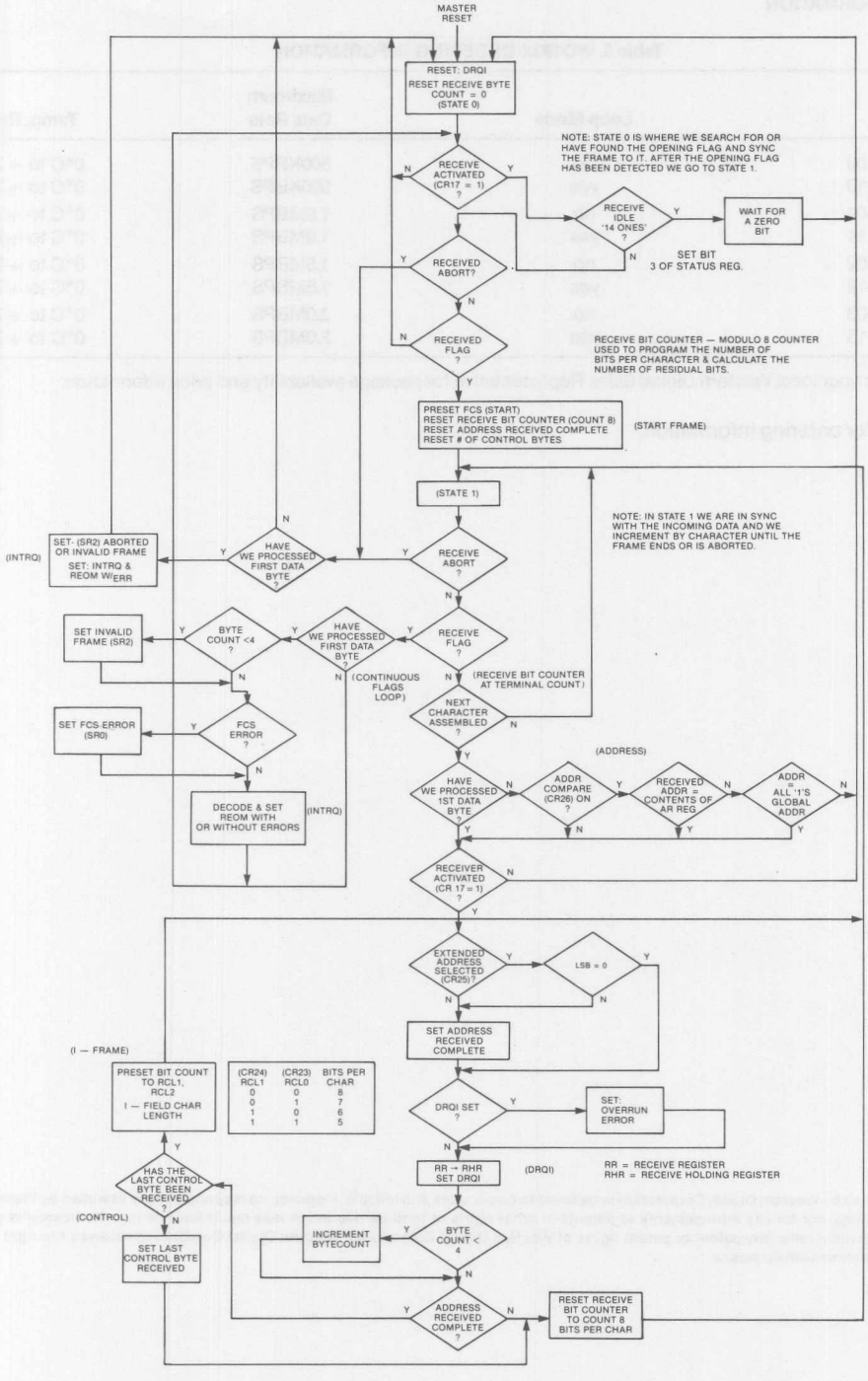


Figure 15. WD193X RECEIVER FLOW CHART

ORDERING INFORMATION

Table 5. WD193X ORDERING INFORMATION

Part No.	Loop Mode	Maximum Data Rate	Temp. Range
WD193X*-00	no	500KBPS	0°C to +70°C
WD193X*-10	yes	500KBPS	0°C to +70°C
WD193X*-01	no	1.0MBPS	0°C to +70°C
WD193X*-11	yes	1.0MBPS	0°C to +70°C
WD193X*-02	no	1.5MBPS	0°C to +70°C
WD193X*-12	yes	1.5MBPS	0°C to +70°C
WD193X*-03	no	2.0MBPS	0°C to +70°C
WD193X*-13	yes	2.0MBPS	0°C to +70°C

* Please contact your local Western Digital Sales Representative for package availability and price information.

See page 429 for ordering information.

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WD1931/WD1933 Compatibility Application Notes

INTRODUCTION

The purpose of this document is to provide the reader with information about the WD1931 and WD1933 devices, and how to take advantage of their compatibility. Various applications examples are given showing flowcharts and timing diagrams. As the devices are designed for use in a very large range of applications, many different features are described and illustrated for the benefit of the reader.

For detailed product information such as A.C. and D.C. parameters, please refer to the respective data sheets.

GENERAL DESCRIPTION

The WD1931 and the WD1933 are MOS/LSI devices which interface a parallel digital system to a serial data communication channel (and vice versa). Both circuits are capable of simplex, half duplex, and full duplex operation.

The WD1931 is designed for character-oriented asynchronous and/or synchronous (BI-SYNC) protocols. The WD1933 is designed for bit-oriented SDLC, HDLC and ADCCP protocols. The devices are programmable and compatible to most 8-bit microcomputers on the market. The pin assignments of these two devices have been chosen to allow the user to implement a one-board multiprotocol design. This board may then be used for any of the above mentioned protocols, by choosing the proper device (WD1931 or WD1933) and connecting some jumpers (see paragraph entitled "Multiprotocol Board Design"). The purpose of these circuits are to convert parallel data from a computer or terminal to a serial data stream at one end of a communication channel. At the other end of the channel, the data is converted back to the original parallel data.

Serial data communications minimizes the number of physical channels required to transfer data and therefore reduces the cost to send data between two (or more) distant points. A microcomputer could perform the same serial/parallel conversion function as these devices, but at much slower speeds. However, using the WD1931 and WD1933 devices to do this function is much more efficient. This makes the computer free to perform other tasks during transmission and reception. The only work that the computer is required to do is to initialize and write data characters to/from the WD1931 or WD1933. These devices will take care of the serialization or deserialization of this data, plus control and timing.

Some control signals on the computer side of the devices are needed for read, write, and control purposes. Additional signals can also be used for special purposes or modes for the convenience of the user. Typically, these other control signals are used to enable communication with a modem or DCE (Data Communications Equipment).

Interrupt outputs are provided to inform the microcomputer when to retrieve from, or to provide data to the holding registers. Also, interrupts can be generated to provide status information such as changes in modem control lines, or that events such as Transmission Complete or Received End of Message have occurred.

SYSTEM APPLICATIONS

WD1931/33 may be used in the following applications:
Switched network
Multipoint network
Non-switched point to point network
Simplex, half-duplex, or full duplex
Asynchronous or synchronous communication
Message switching
Multiplexing systems
Data concentrator systems
Loop data link systems
DMA applications
Parallel to serial data conversion (and vice versa)
Local Networks
Packet Switching
X.25
Multidrop line systems

A typical block diagram of a data link is shown in Figure 1. The communication media used could be a direct communication channel (such as a leased telephone line), a switched telephone line, or one of many other possibilities. Typically these applications would require the use of a modem.

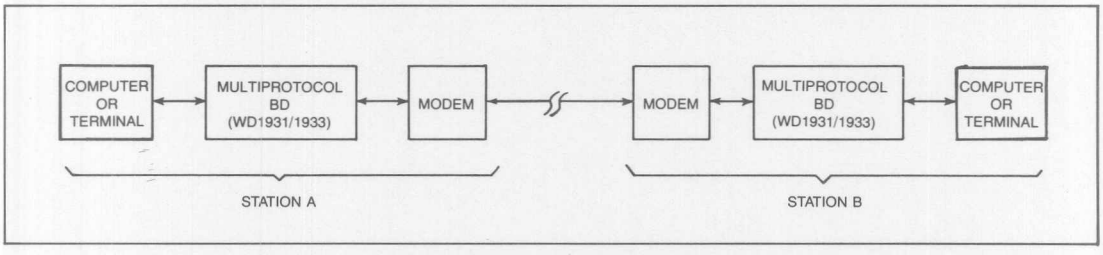


Figure 1. DATA LINK BLOCK DIAGRAM

The applications that these devices could be used in would be a combination of the previously mentioned. A modem would be needed for long distance communication lines. For shorter distance, line drivers/receivers may be sufficient. In some very well controlled environments, such as a laboratory, two devices may be connected without line drivers and receivers.

The WD1931 or WD1933 may be connected directly to a microcomputer bus, but buffers would normally be recommended. Figure 2 shows a typical schematic of an interface between a Z80 microcomputer and a modem. This is called a multiprotocol board, which is described later in this document.

Some examples of various WD1931/WD1933 systems are shown here by use of block diagrams. The station shown in Figure 3 consists of a computer or terminal, a multiprotocol board, and a modem. A station may consist of only the computer or terminal, and one WD1931 or WD1933 device. Whether the modem, line drivers and receivers, or CPU buffers are needed depends on the details of the particular design situation.

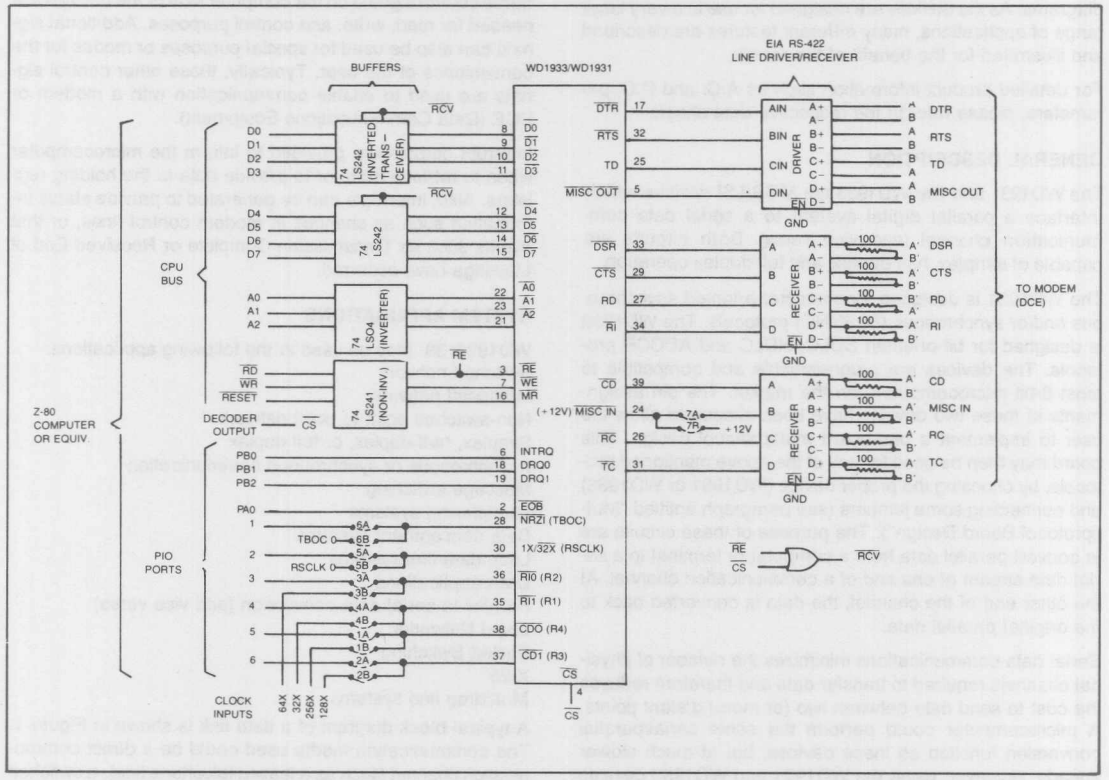


Figure 2. WD1931/1933 AND MICROCOMPUTER. (MULTIPROTOCOL BOARD)

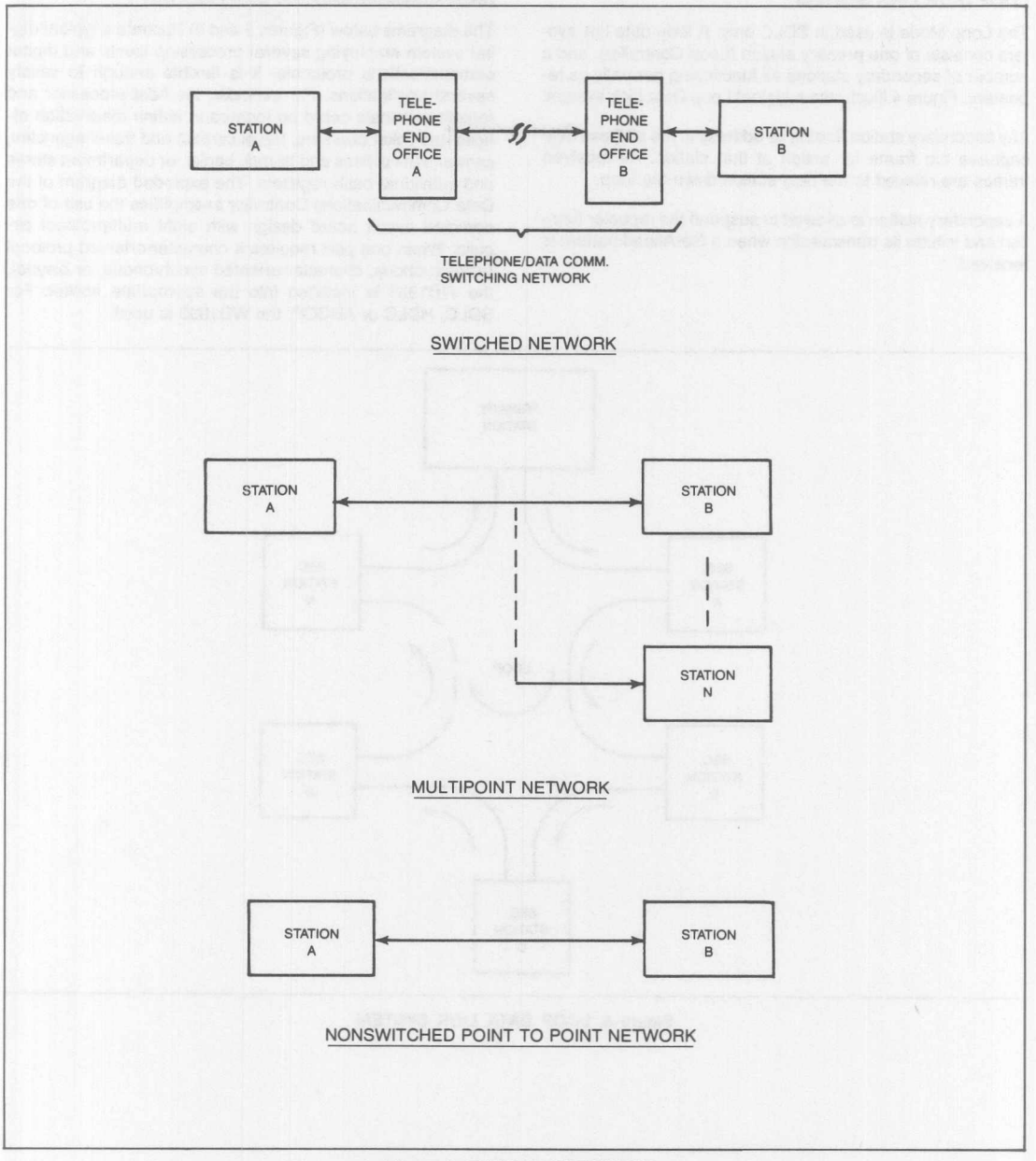


Figure 3. TYPICAL NETWORKS

LOOP DATA LINK SYSTEM

The Loop Mode is used in SDLC only. A loop data link system consists of one primary station (Loop Controller), and a number of secondary stations all functioning normally as repeaters. Figure 4 illustrates a typical Loop Data Link system.

Any secondary station finding its address in the address field captures the frame for action at that station. All received frames are relayed to the next station down the loop.

A secondary station is allowed to suspend the repeater function and initiate its transmission when a Go-Ahead pattern is received.

DATA COMMUNICATIONS EXAMPLE NO. 1

The diagrams below (Figures 5 and 6) illustrate a typical digital system employing several processing levels and digital communications protocols. It is flexible enough to satisfy several applications. For example, the host processor and remote terminals could be located in airline reservation offices and ticket counters, travel centers and travel agencies, central bank offices and branch banks, or department stores and individual cash registers. The exploded diagram of the Data Communications Controller exemplifies the use of one common circuit board design with eight multiprotocol circuits. When one port requires a character-oriented protocol (asynchronous, character oriented synchronous, or bisync), the WD1931 is installed into the appropriate socket. For SDLC, HDLC or ADCCP, the WD1933 is used.

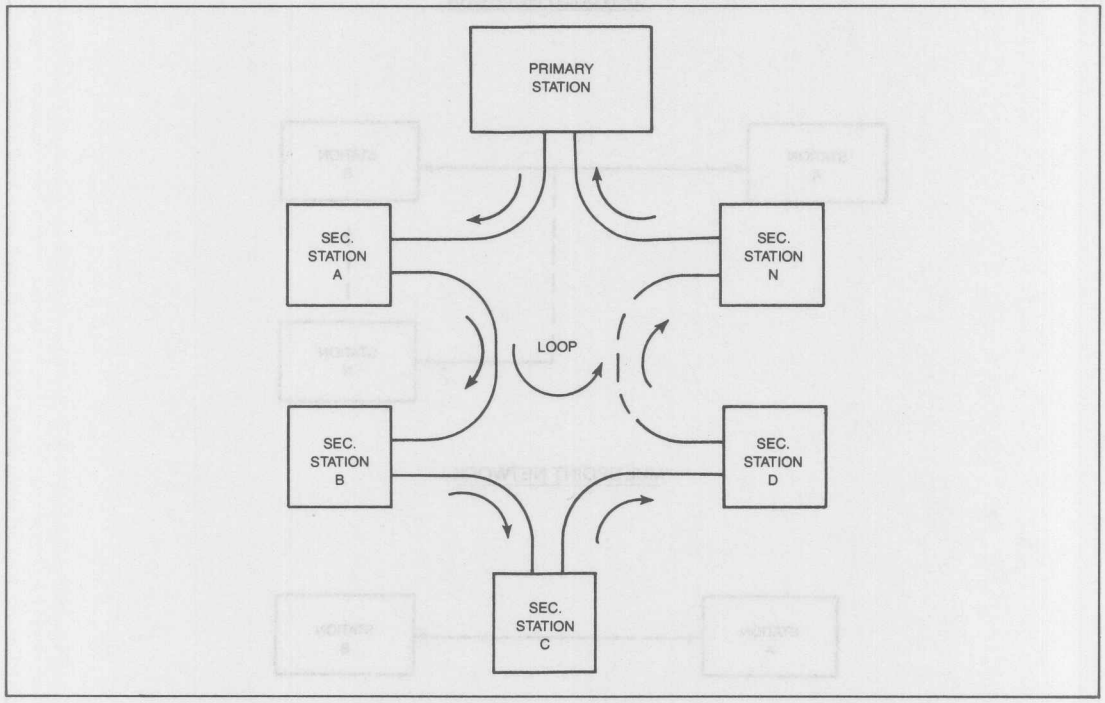


Figure 4. LOOP DATA LINK SYSTEM

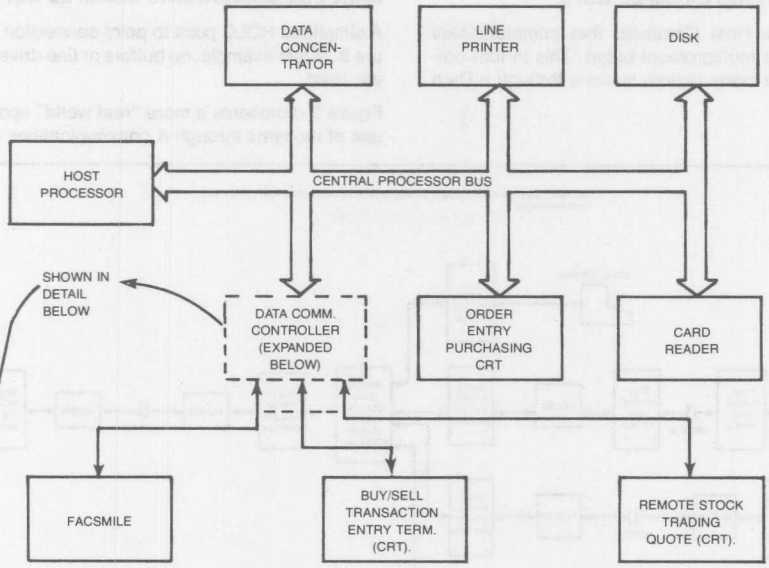


Figure 5. STOCK BROKERAGE SYSTEM

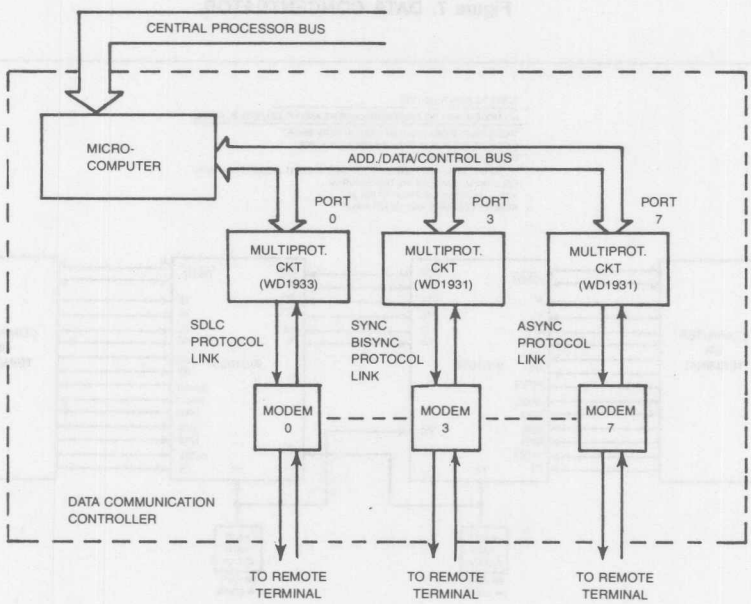


Figure 6. DATA COMMUNICATION CONTROLLER

DATA COMMUNICATIONS EXAMPLE NO. 2

Figure 7 illustrates a Host Computer that communicates through modems to a multiprotocol board. This in turn collects information from many remote stations through a Data Concentrator.

DATA COMMUNICATIONS EXAMPLE NO. 3

A simplified HDLC point to point connection is shown in Figure 8. In this example, no buffers or line drivers and receivers are used.

Figure 9 represents a more "real world" application with the use of modems through a communications channel.

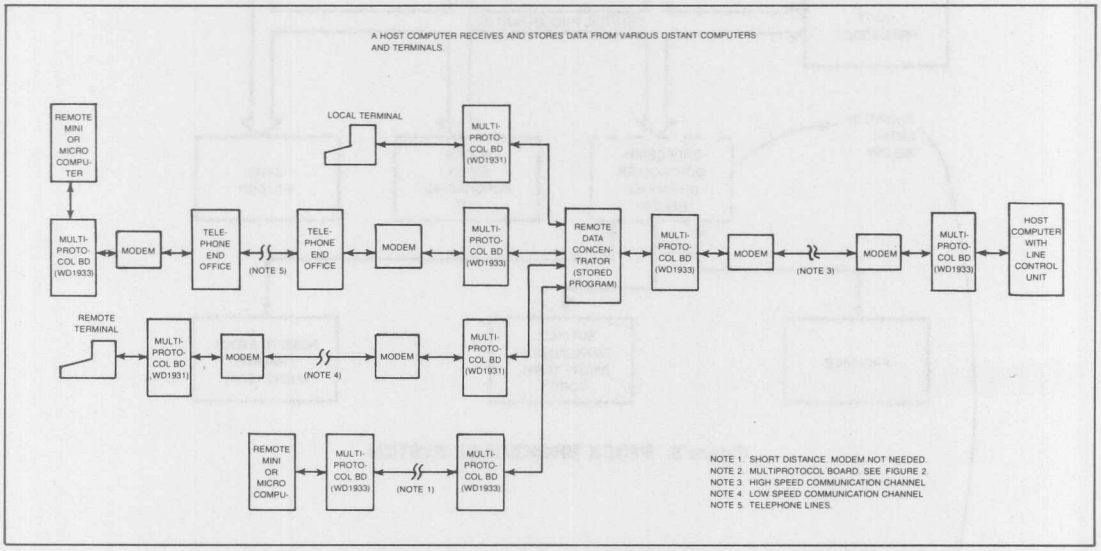


Figure 7. DATA CONCENTRATOR

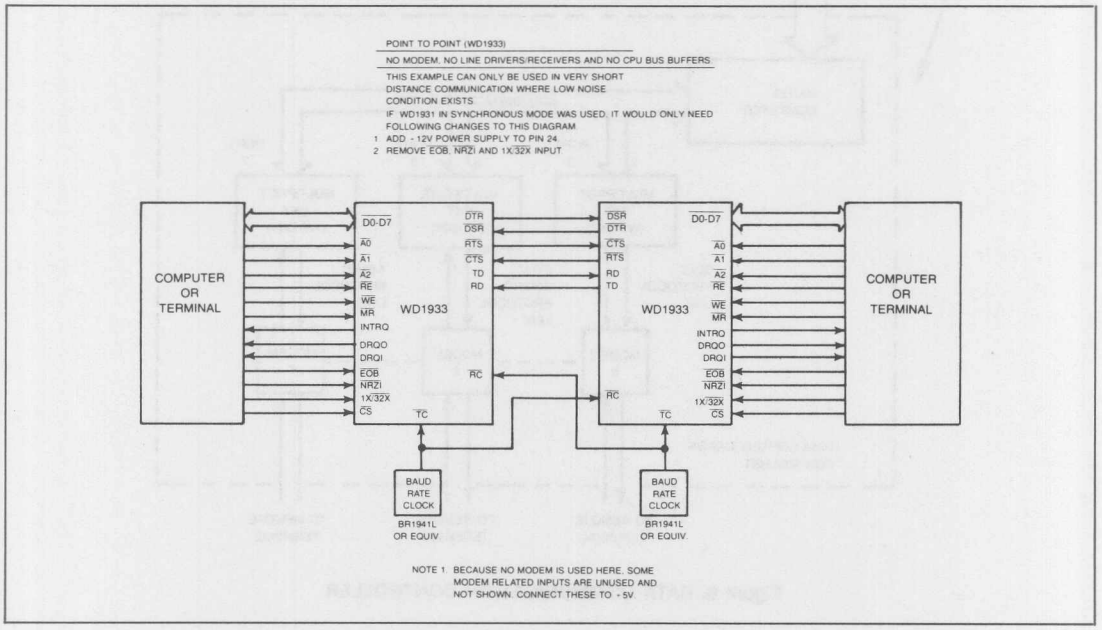


Figure 8. HDLC POINT TO POINT

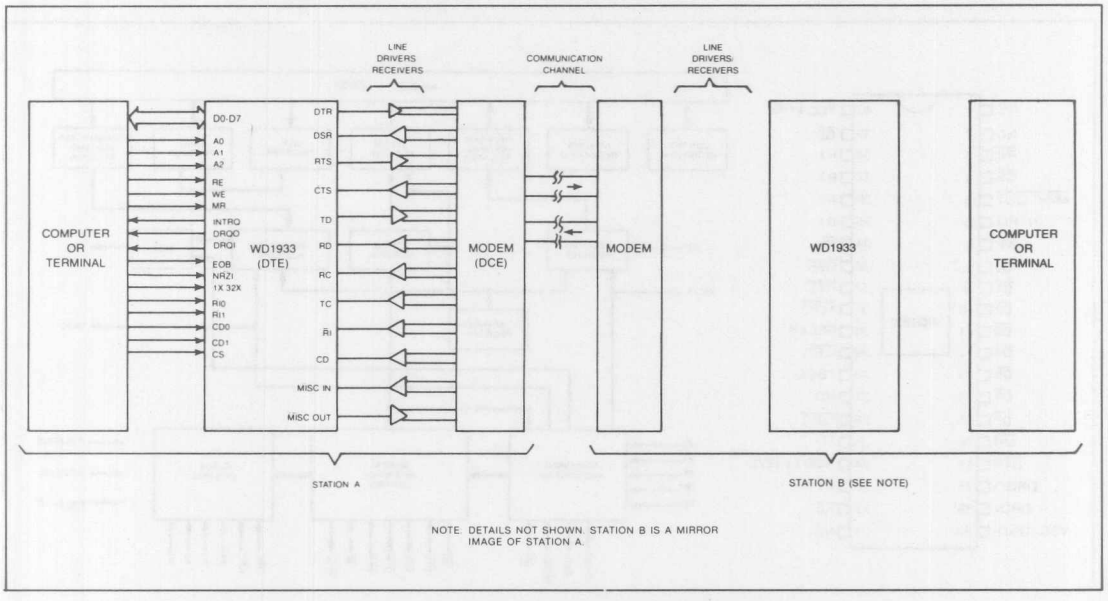


Figure 9. HDLC POINT TO POINT WITH MODEM

WD1931 AND WD1933 TECHNICAL DESCRIPTIONS

The WD1931 and WD1933 devices have been designed to provide a high degree of compatibility and interchangability. The pin-outs are similar, and the register operations are software compatible. This feature allows for the use of either device in a given socket.

WD1931 PIN-OUTS AND BLOCK DIAGRAM

The WD1931 pin assignments and the block diagram are shown in Figure 10.

WD1933 PIN-OUTS AND BLOCK DIAGRAM

The WD1933 pin assignments and the block diagram are shown in Figure 11.

SHORT FORM REGISTER FORMAT AND ADDRESSING

Information concerning operating modes and status conditions are passed to and from the WD1931 or WD1933 device through I/O addressable registers. Each register contains eight bits, where each bit represents a specific function and has its own mnemonics.

The state of each bit is represented by a "1" for TRUE and a "0" for FALSE. This may or may not correlate to a measurable voltage level at a pin, since some pins are TRUE when they are at 0 volts (this is indicated by a bar over the name, or a slash immediately preceeding the name).

The WD1931 registers are shown in Figure 12. Note that some bits are affected by the transmit clock ($\overline{TC}$) rate or the receive clock ($\overline{RC}$) rate.

The WD1933 registers are shown in Figure 13. Note that some bits are affected by the transmit clock ($\overline{TC}$) rate or the receive clock ($\overline{RC}$) rate.

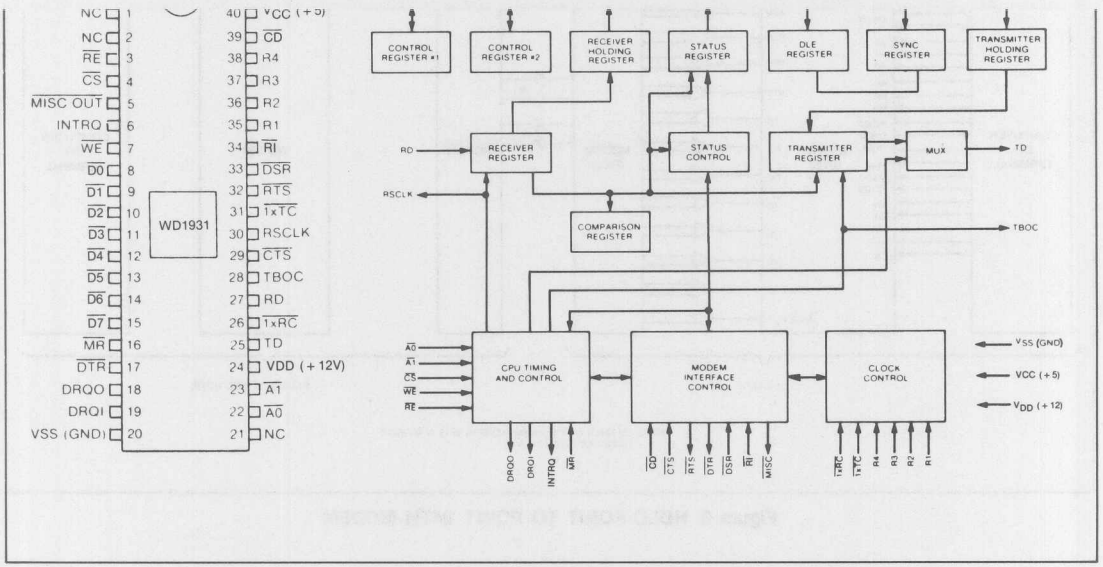


Figure 10. WD1931 PIN CONNECTIONS AND BLOCK DIAGRAM

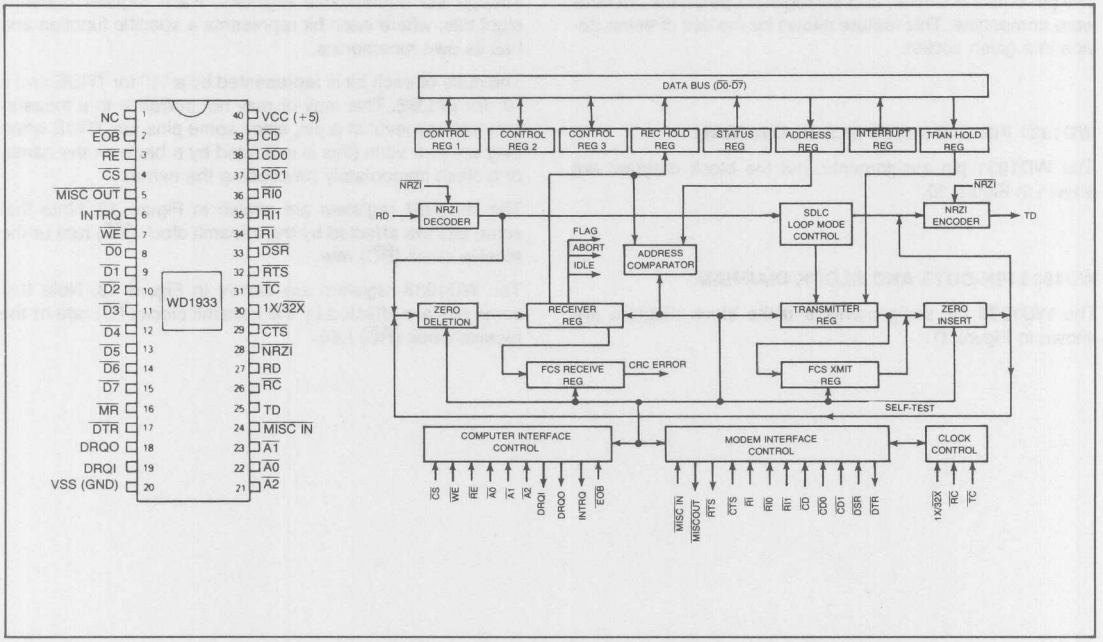
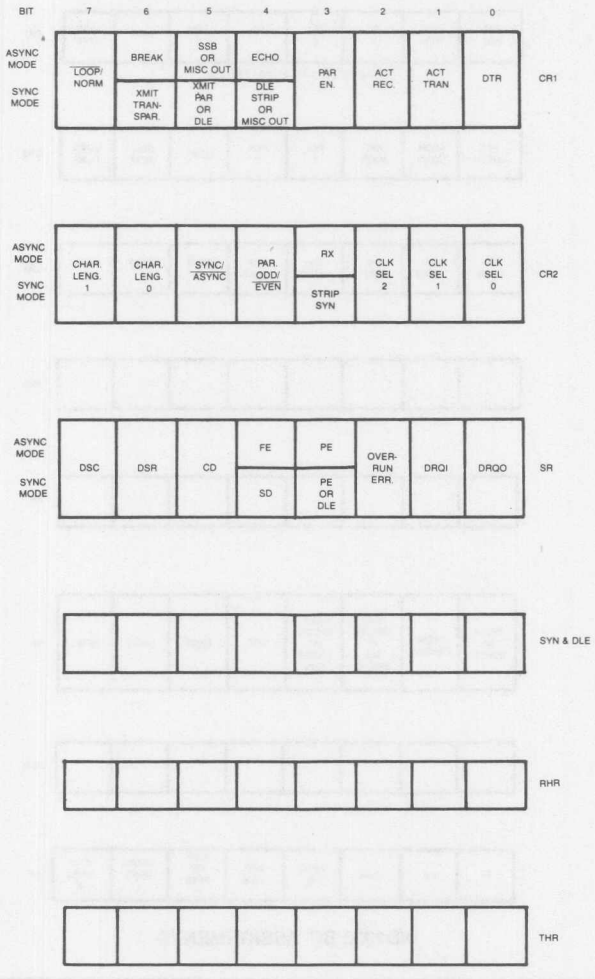


Figure 11. WD1933 PIN CONNECTIONS AND BLOCK DIAGRAM

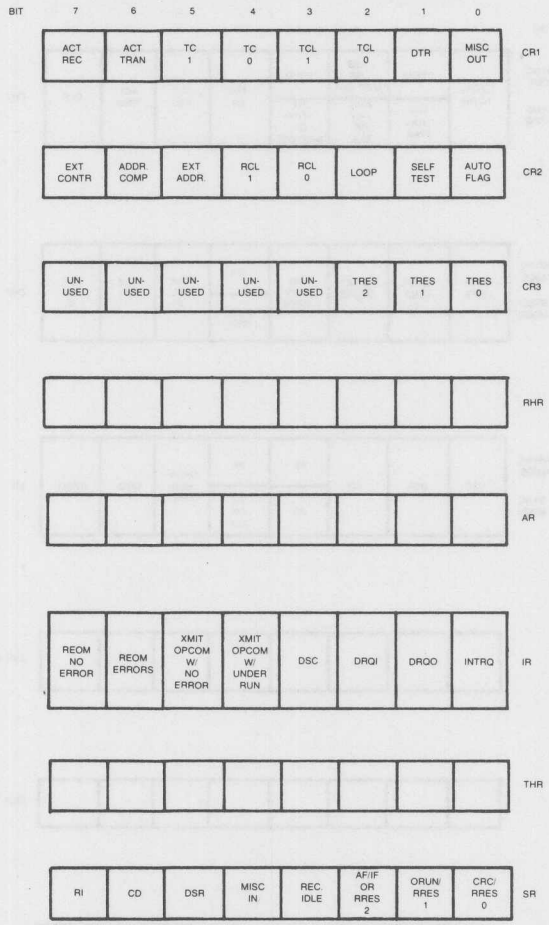


WD1931 BIT ASSIGNMENTS

$\overline{A1}$	$\overline{A0}$	READ	WRITE	CLOCK
LO	LO	CR1	CR1	NONE
LO	HI	CR2	CR2	NONE
HI	LO	SR	SYN & DLE	SR0 = $\overline{TC}$. SR1-4 = $\overline{RC}$. SR5-7, SYN, DLE = NONE
HI	HI	RHR	THR	RHR = $\overline{RC}$. THR = NONE

WD1931 REG. ADDRESSES AND CLOCKS

Figure 12. WD1931 REGISTERS



WD1933 BIT ASSIGNMENTS

$\overline{A2}$	$\overline{A1}$	$\overline{A0}$	READ	WRITE	CLOCK
HI	HI	HI	CR1	CR1	NONE*
HI	HI	LO	CR2	CR2	NONE*
HI	LO	HI	CR3	CR3	NONE*
HI	LO	LO	RHR	AR	RHR = $\overline{RC}$. AR = NONE
LO	HI	HI	IR	THR	IR = $\overline{TC}$. THR = NONE
LO	HI	LO	SR	—	SR0-3 = $\overline{RC}$. SR4-7 = NONE

*After a master reset operation, 2.5 TC clock cycles are required.

WD1933 ADDRESSES AND CLOCKS

Figure 13. WD1933 REGISTERS

MULTIPROTOCOL BOARD DESIGN

The WD1931 and WD1933 pin assignments were chosen so that a circuit board designer may use only one 40-pin socket, but have the choice of using either device on that board. Depending on the application, a few jumper wires may be needed, or perhaps none at all. Figure 2 shows a typical example of a multiprotocol board. This board may be designed with even less components and jumpers, dependent on the particular application it is intended for.

Jumpers 1A-7A are to be connected when WD1933 and all its options are used. Jumpers 1B-7B are to be connected when WD1931 and all its options are used.

For example, if the user does not need the NRZI signal mode, the 1X clock is only used, no Ring or Carrier Detect indication is needed, TBOC, RSCLK and MISC IN are not used, and then no jumpers are needed in the design. In this case, pin 24 may be permanently connected to +12V. Pins 28 and 30 may be connected to +5V via a 10K resistor, and pins 35 through 38 may be connected directly to +5V.

TRANSMISSION EXAMPLE 1 (ONE FRAME)

A typical sequence of events is shown here to transmit a message from computer A to another computer (or terminal) B through a switched network. The message to be sent is a synchronous SDLC protocol frame as shown below in Figure 14. For simplicity, the message sent in this example is very straightforward and short.

Line drivers and receivers are used, permitting transmission to a remote DCE or modem (see schematic in Figure 2). As the SDLC frame is sent, the WD1933 is used. The jumpers required are 1A-7A. Figure 15 illustrates the functional flow, and Figure 16 details the timing of the transmitted frame. Note that the device can be programmed in several different ways to allow for various requirements.

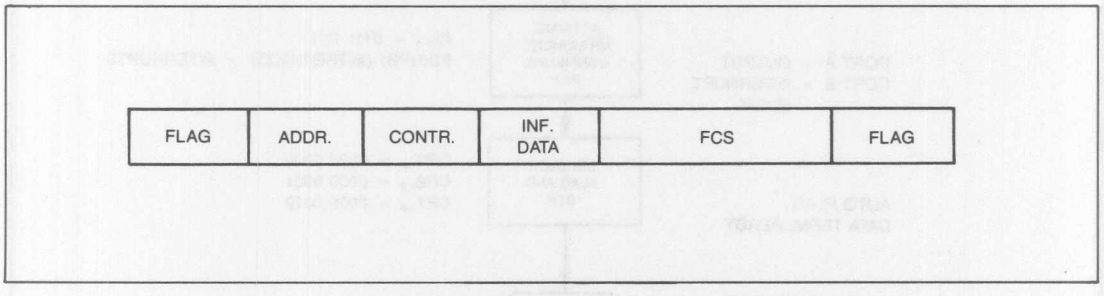


Figure 14. SDLC FRAME FORMAT

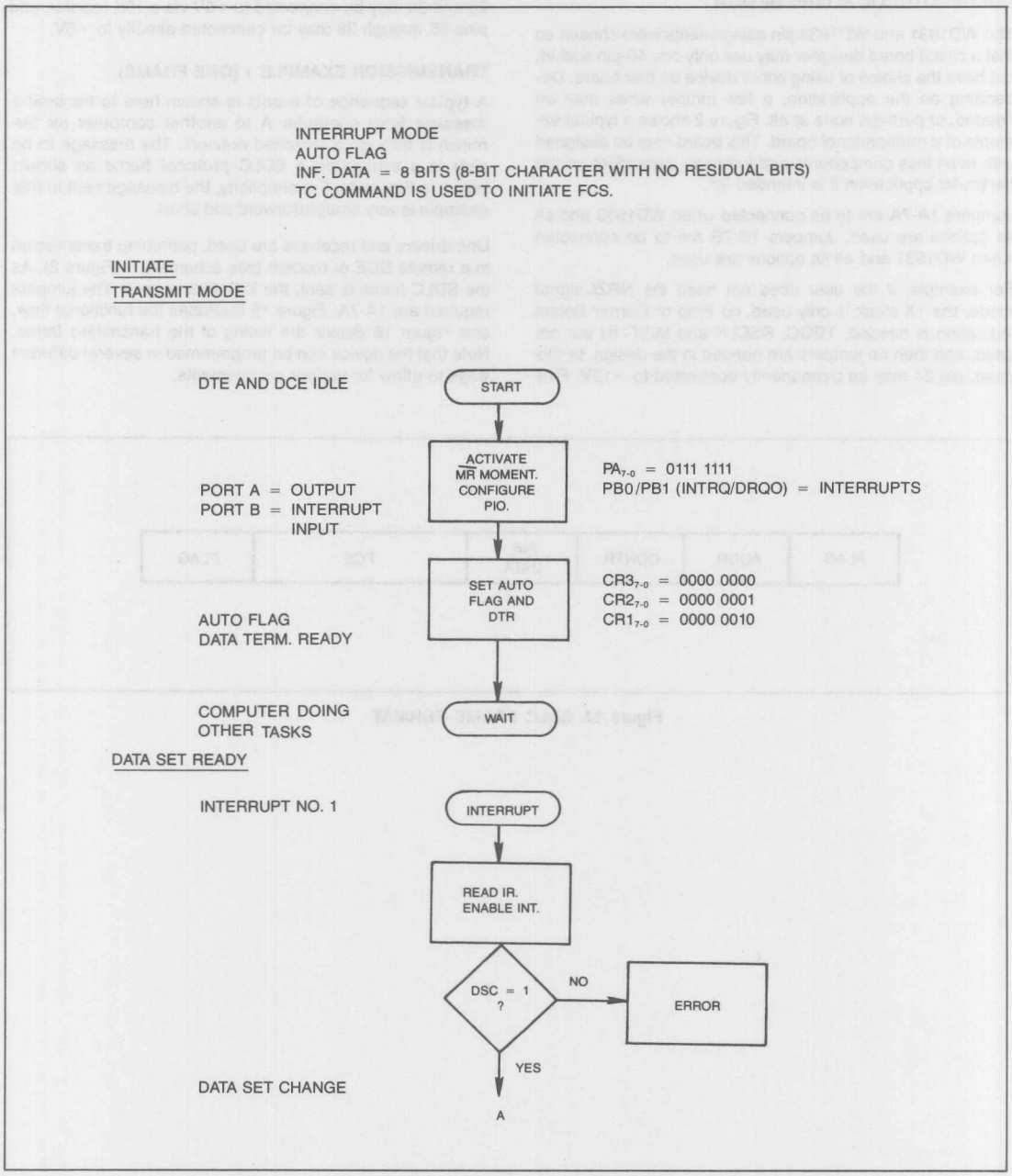


Figure 15. FLOW DIAGRAM OF FRAME TRANSMISSION

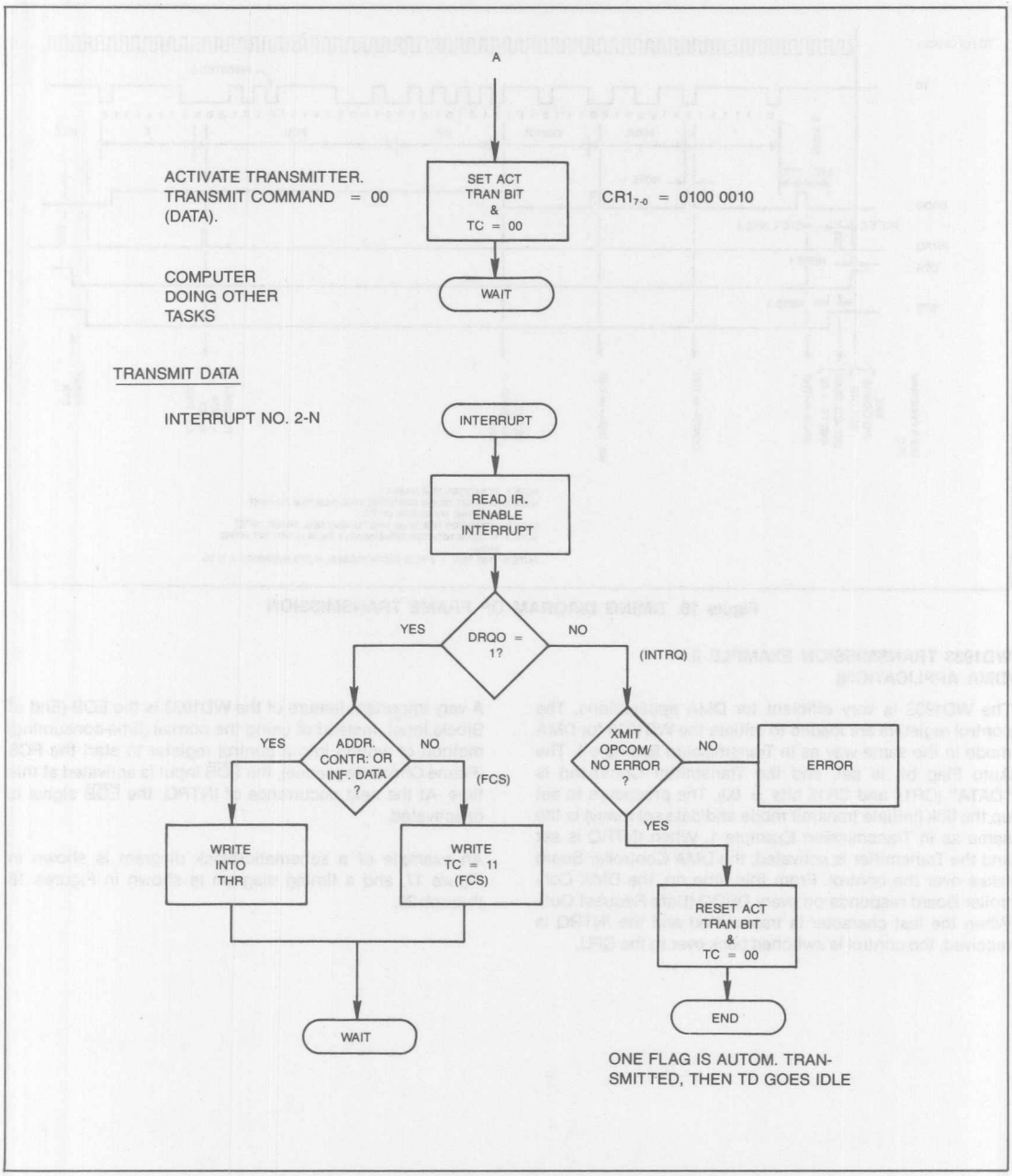


Figure 15. FLOW DIAGRAM OF FRAME TRANSMISSION

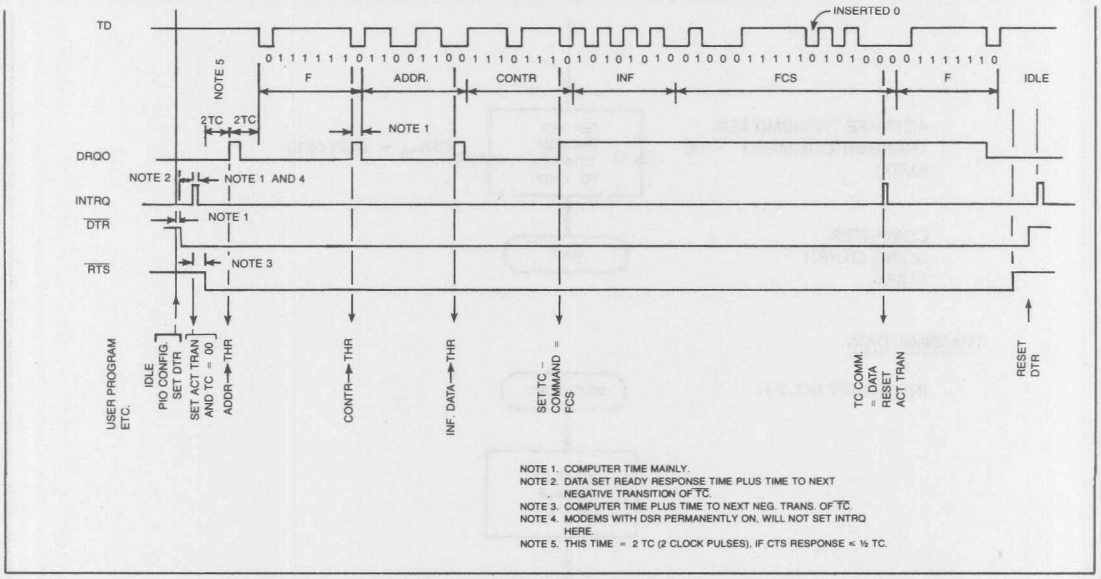


Figure 16. TIMING DIAGRAM OF FRAME TRANSMISSION

WD1933 TRANSMISSION EXAMPLE 2 (DMA APPLICATION)

The WD1933 is very efficient for DMA applications. The control registers are loaded to initiate the WD1933 for DMA mode in the same way as in Transmission Example 1. The Auto Flag bit is set, and the Transmitter Command is "DATA" (CR14 and CR15 bits = 00). The procedure to set up the link (initiate transmit mode and data set ready) is the same as in Transmission Example 1. When INTRQ is set and the Transmitter is activated, the DMA Controller Board takes over the control. From this time on, the DMA Controller Board responds on every DRQO (Data Request Out). When the last character is transmitted and the INTRQ is received, the control is switched back over to the CPU.

A very important feature of the WD1933 is the EOB (End of Block) input. Instead of using the normal (time-consuming) method of writing into a control register to start the FCS (Frame Check Sequence), the $\overline{EOB}$ input is activated at this time. At the next occurrence of INTRQ, the $\overline{EOB}$ signal is deactivated.

An example of a schematic/block diagram is shown in Figure 17, and a timing diagram is shown in Figures 18 through 20.

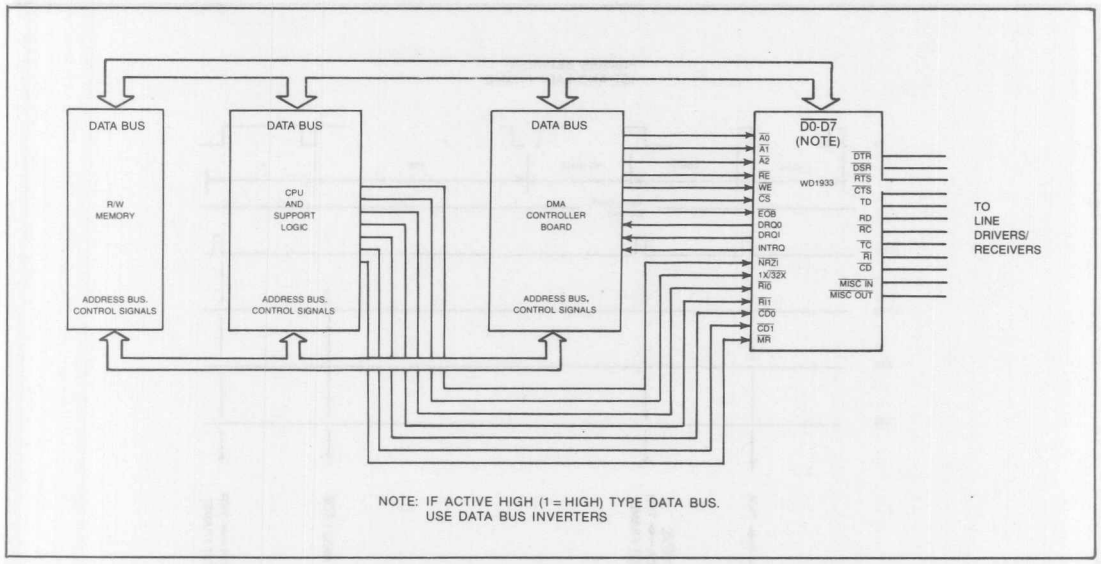


Figure 17. BLOCK DIAGRAM OF DMA APPLICATION

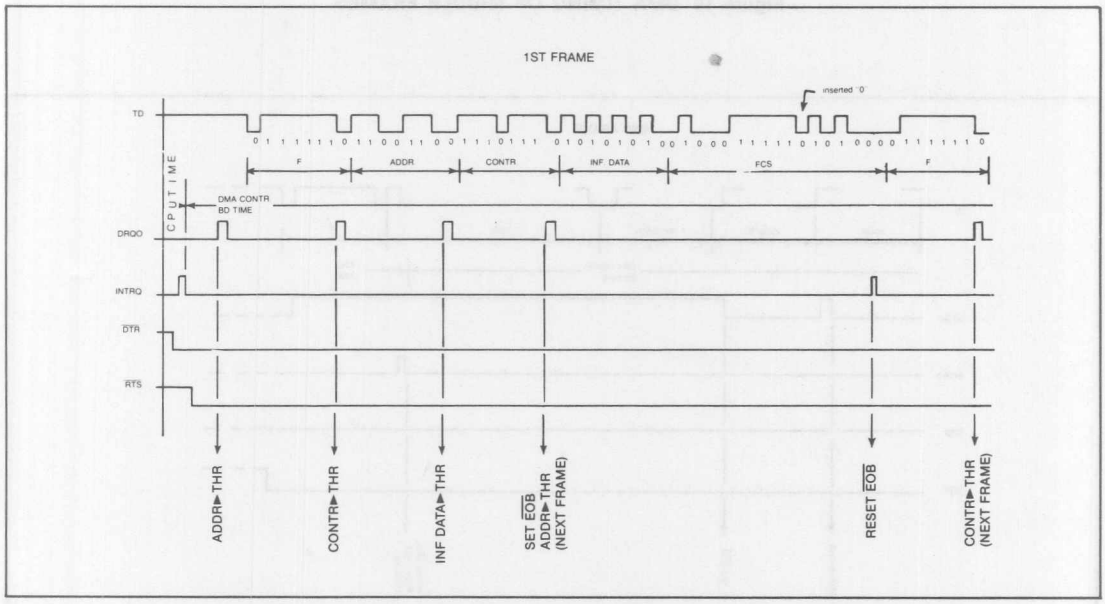


Figure 18. DMA TIMING OF FIRST FRAME

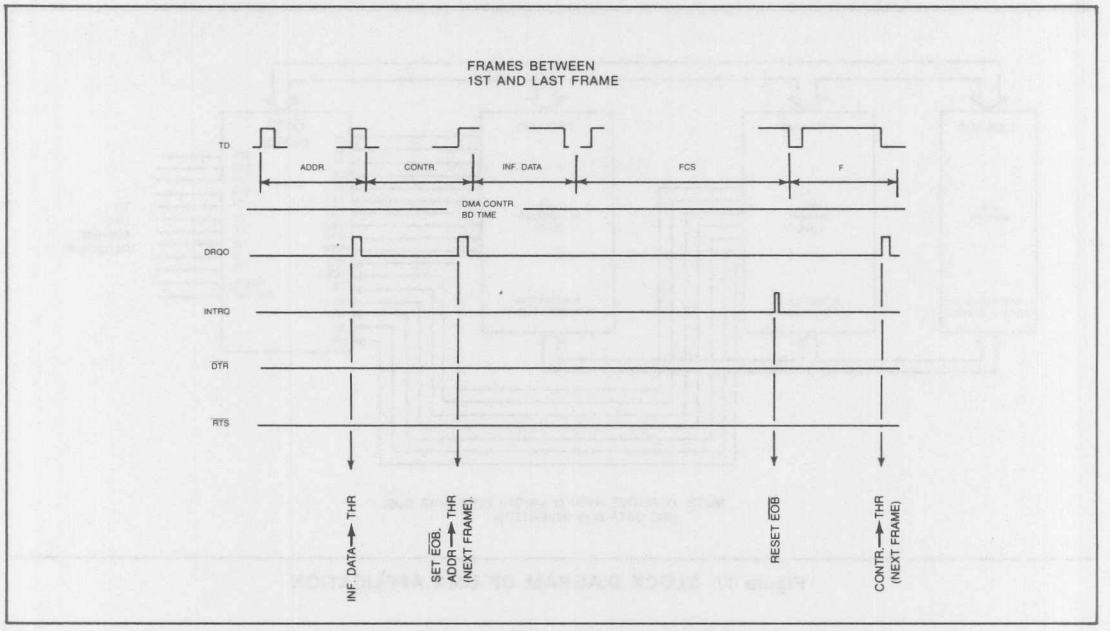


Figure 19. DMA TIMING OF MIDDLE FRAMES

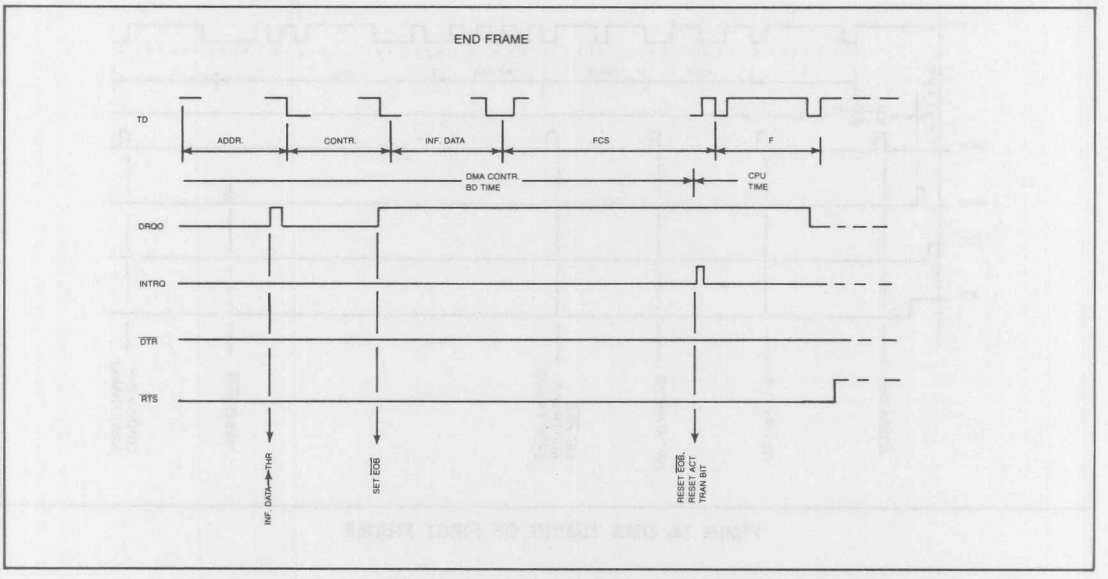


Figure 20. DMA TIMING OF LAST FRAME

WD1933 RECEPTION EXAMPLE 1

A sequence of events is shown in illustrating how to receive a message with the WD1933 device. For simplicity, the same SDLC frame structure is used as in Transmission Example 1. Also, please refer to the same interface circuitry shown in Figure 2.

Figure 21 illustrates the functional flow, and Figure 22 contains the timing information.

WD1933 RECEPTION EXAMPLE 2

This example shows a frame with two ADDRESS characters, two CONTROL characters, one 5-bit INFORMATION DATA character, and two residual bits. This example may not be a typical frame, but it shows how the WD1933 works in a wide range of frame structures.

The first FLAG and FCS are not shown in detail, and are not critical to this example.

Figure 23 illustrates the functional flow, and Figure 24 contains the timing information.

WD1933 LOOP DATA LINK EXAMPLE

This example shows how to program a secondary station to function in SDLC Loop mode. The functional flow is illustrated in Figure 25, and the interface circuit is shown in Figure 2.

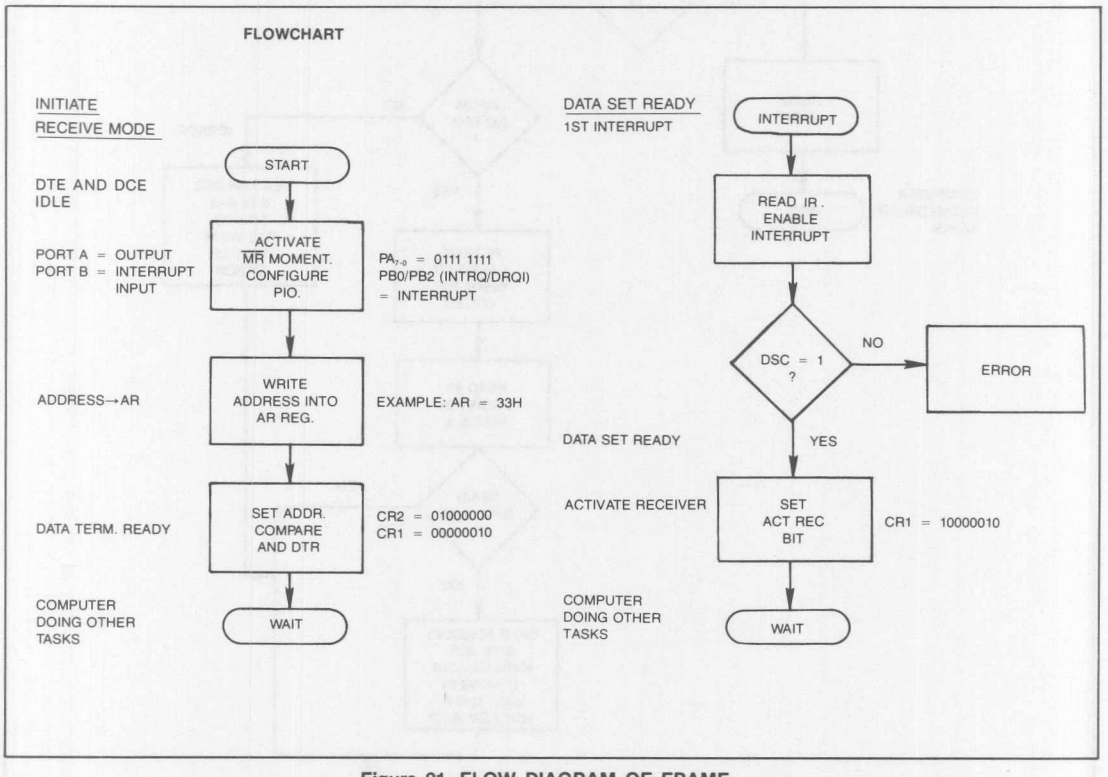


Figure 21. FLOW DIAGRAM OF FRAME RECEPTION (EXAMPLE NO. 1)

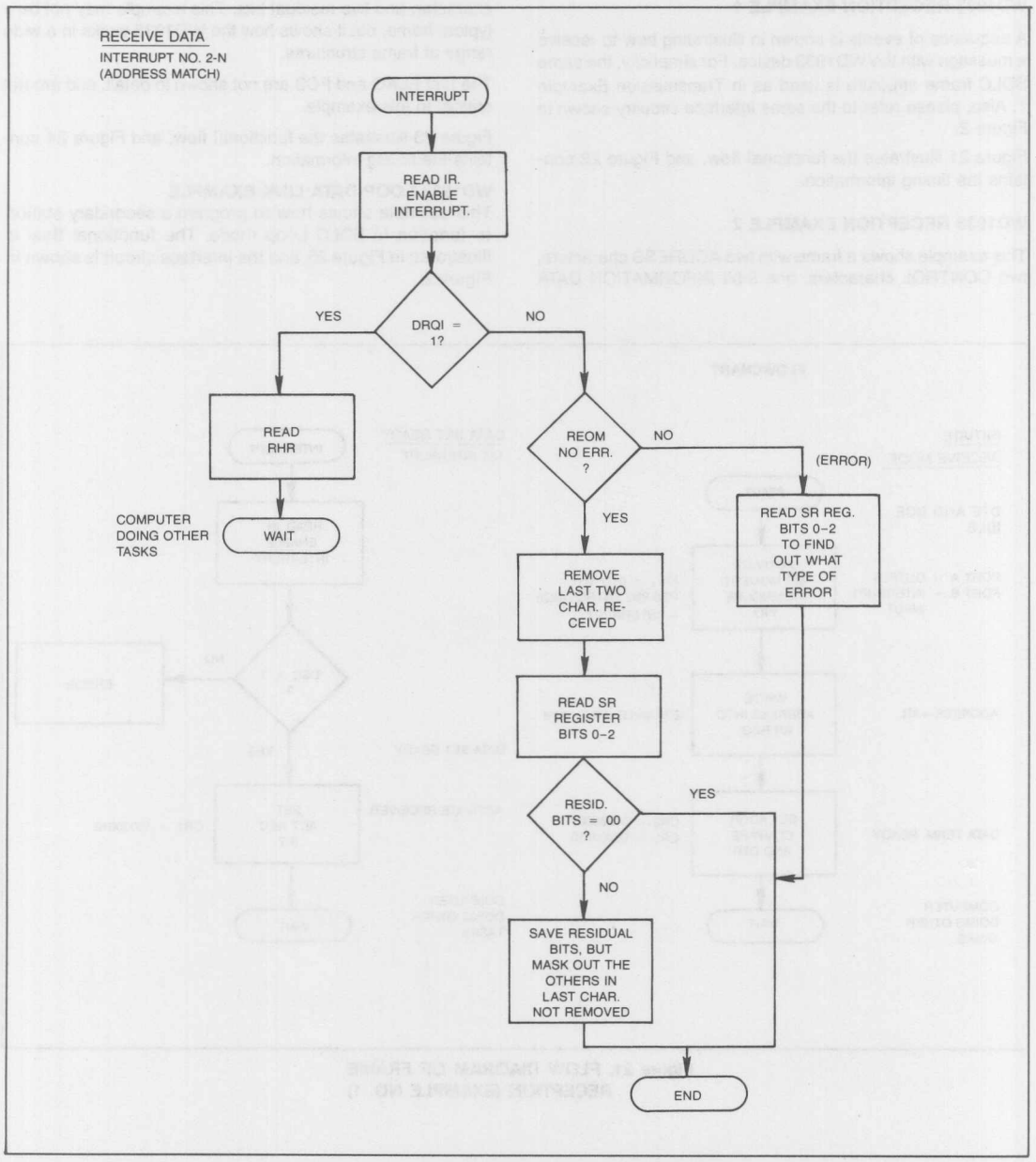


Figure 21. FLOW DIAGRAM OF FRAME RECEPTION

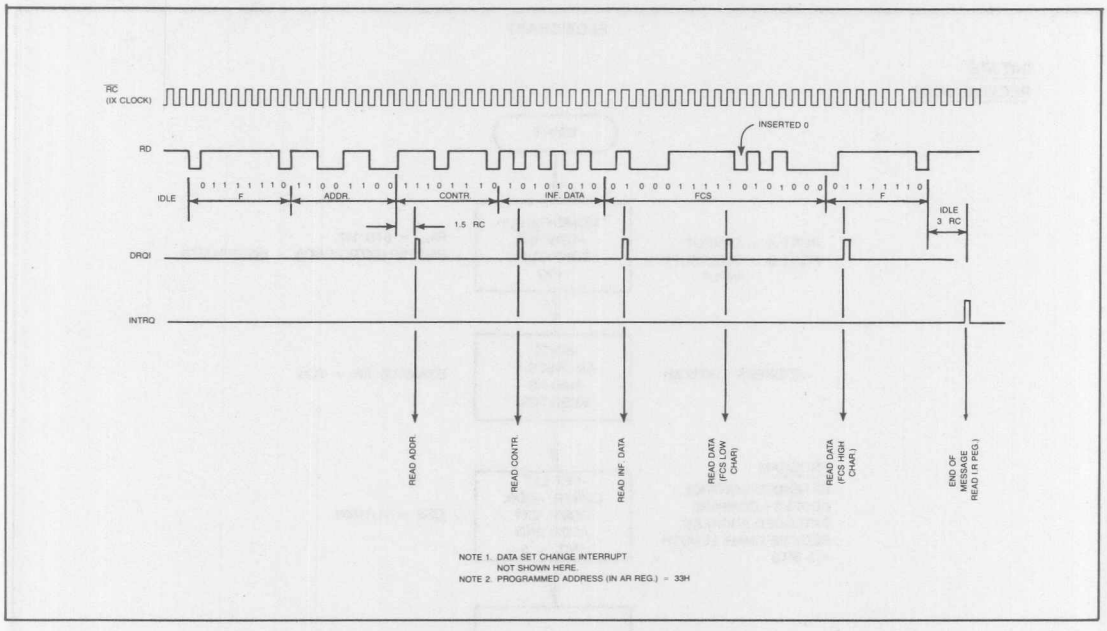


Figure 22. TIMING DIAGRAM OF FRAME RECEPTION (EXAMPLE NO. 1)

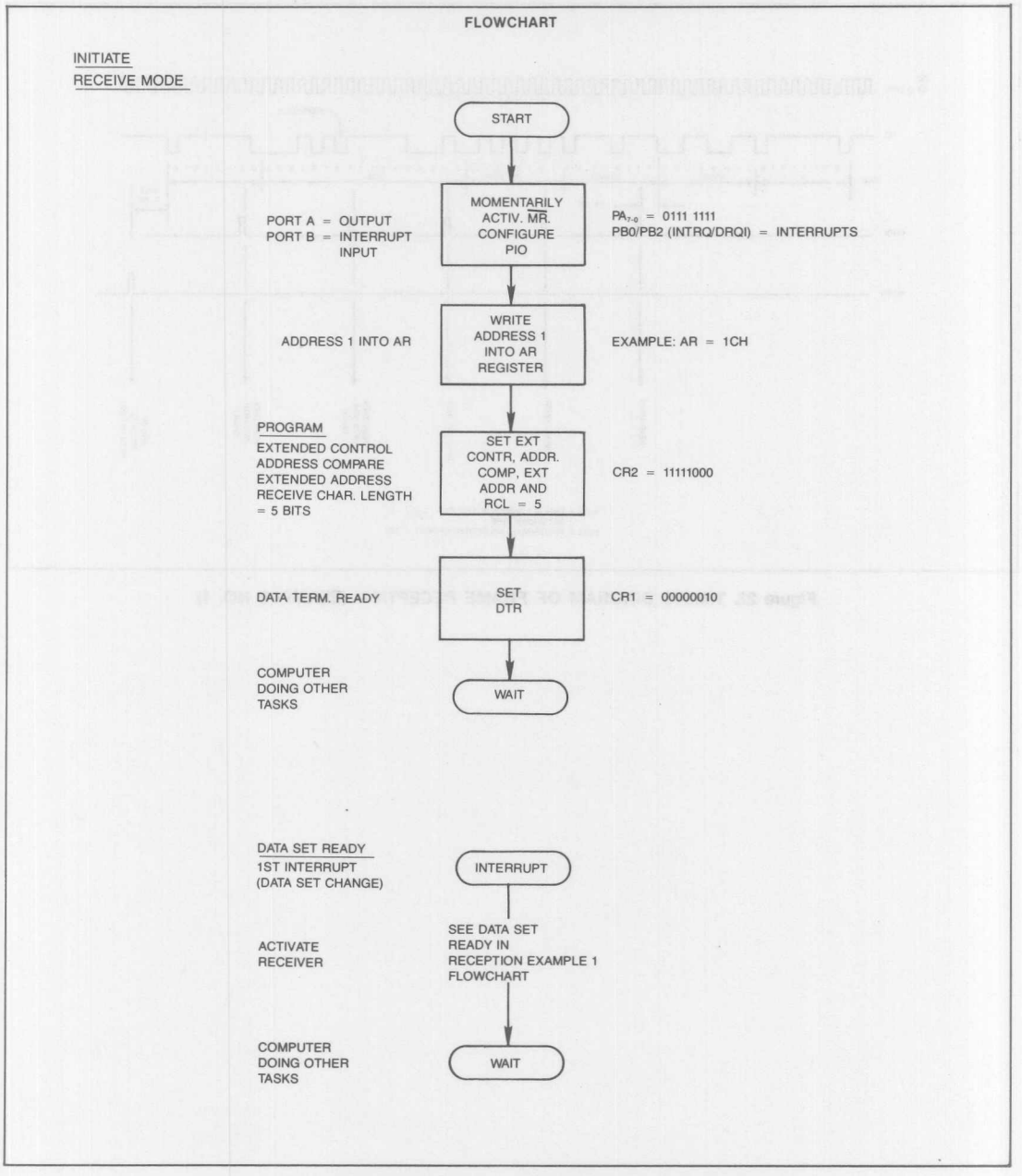


Figure 23. FLOW DIAGRAM OF FRAME RECEPTION (EXAMPLE NO. 2)

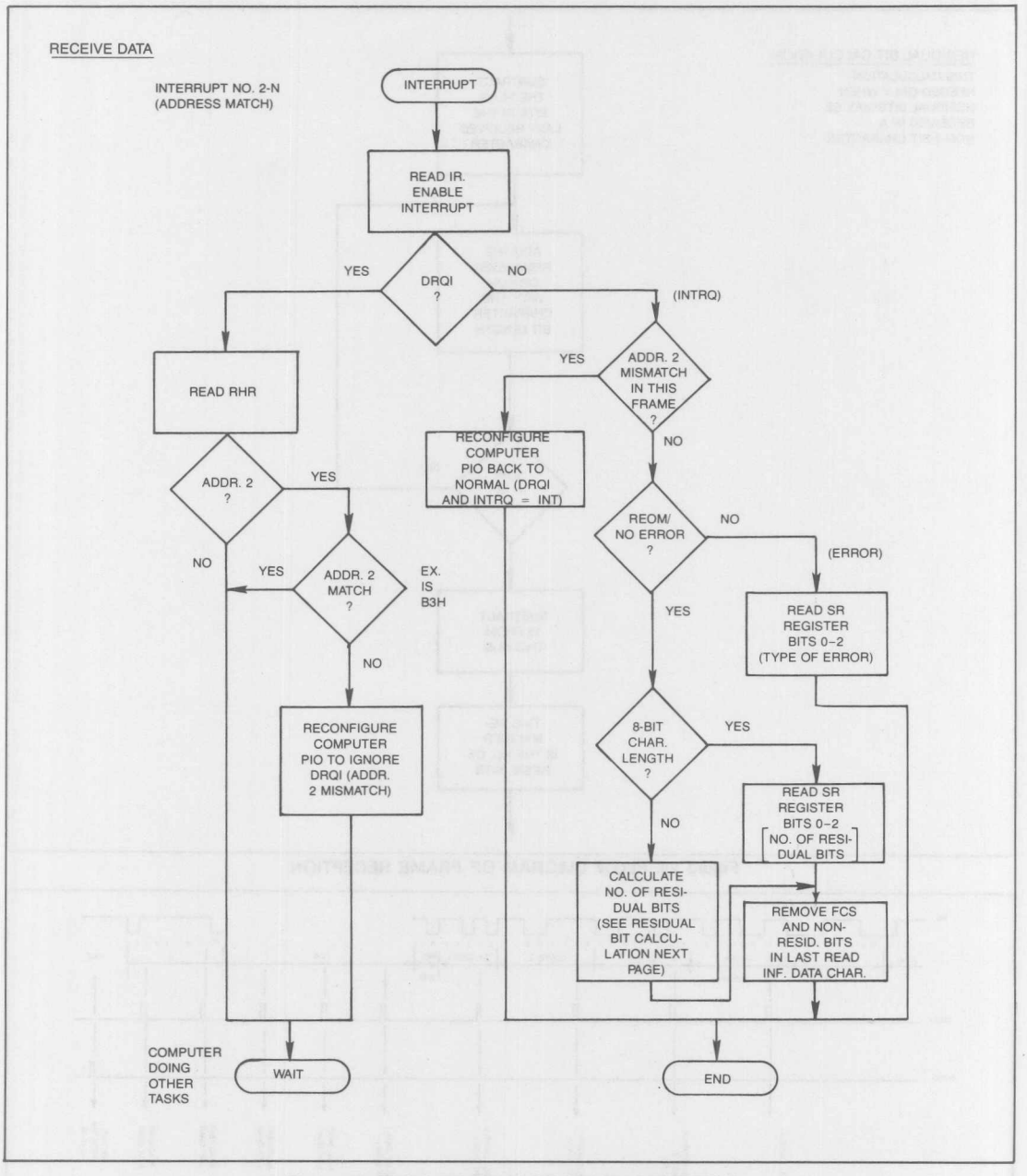


Figure 23. FLOW DIAGRAM OF FRAME RECEPTION

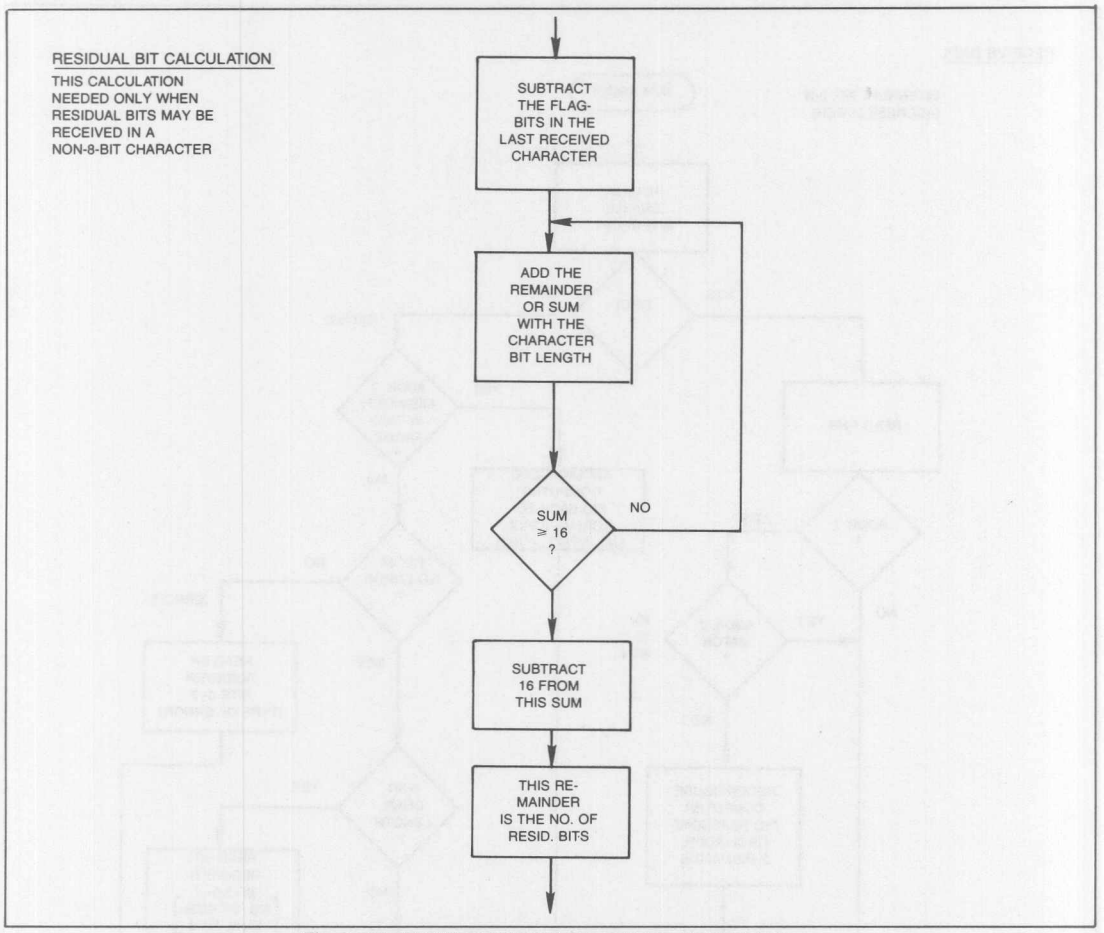


Figure 23. FLOW DIAGRAM OF FRAME RECEPTION

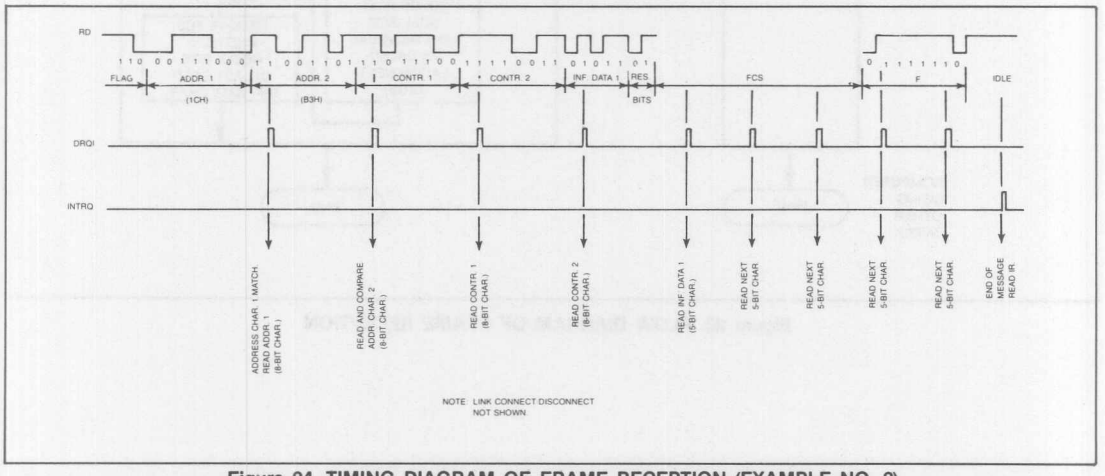


Figure 24. TIMING DIAGRAM OF FRAME RECEPTION (EXAMPLE NO. 2)

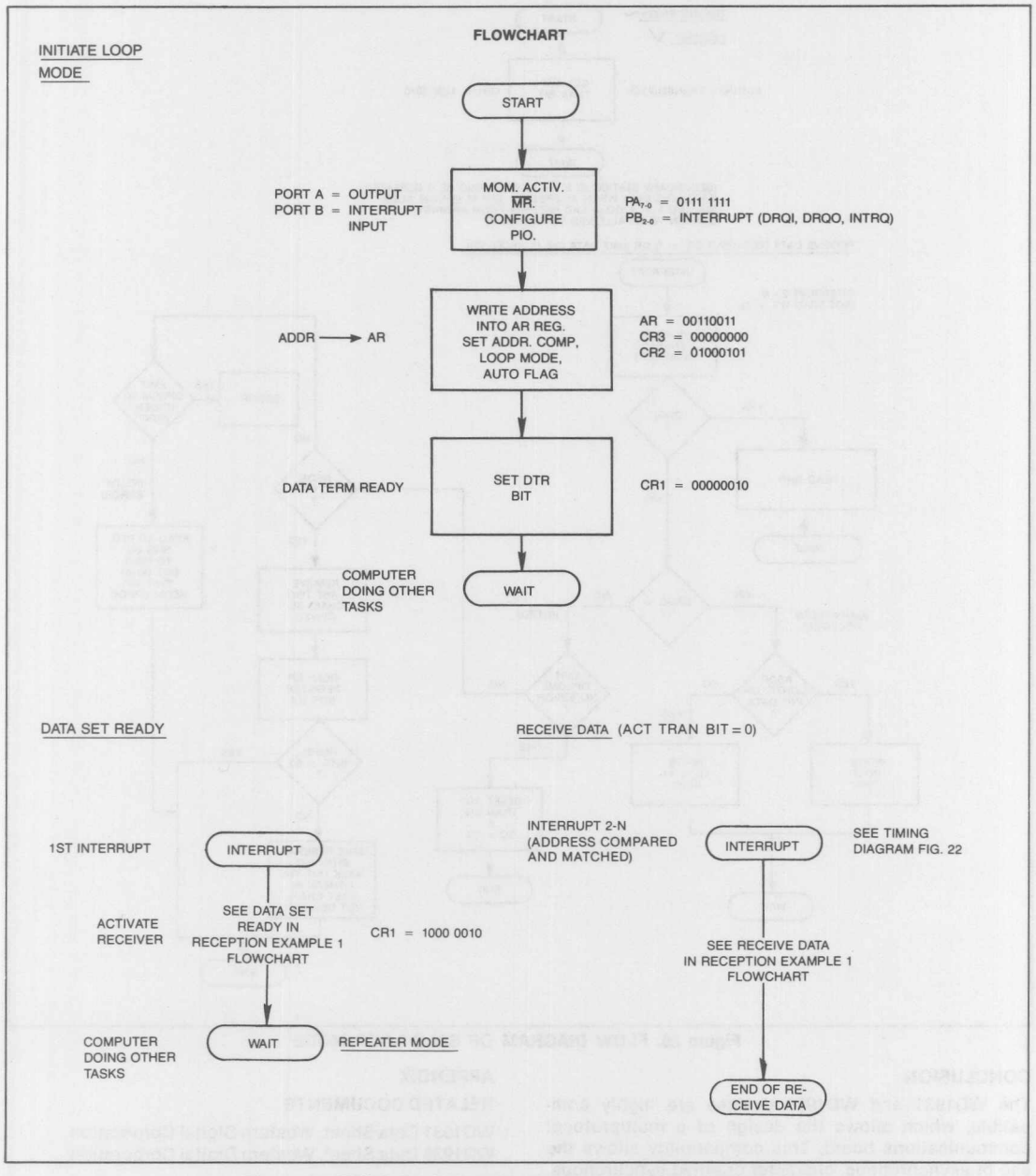


Figure 25. FLOW DIAGRAM OF SDLC LOOP MODE OPERATION

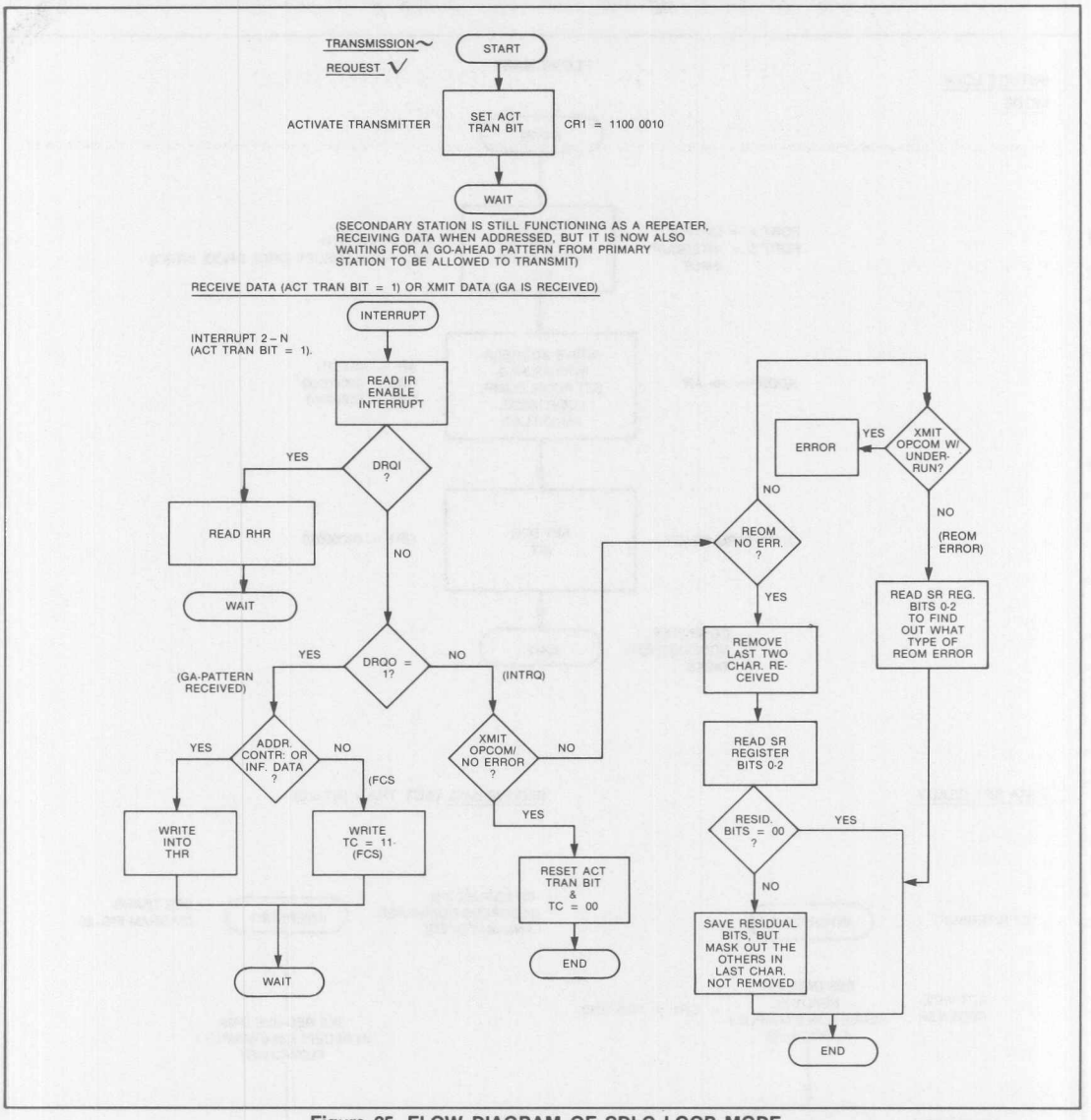


Figure 25. FLOW DIAGRAM OF SDLC LOOP MODE

CONCLUSION

The WD1931 and WD1933 devices are highly compatible, which allows the design of a multiprotocol communications board. This compatibility allows the use of asynchronous, character oriented synchronous, and bit oriented synchronous communications protocols with the same 40 pin socket.

APPENDIX

RELATED DOCUMENTS

WD1931 Data Sheet, Western Digital Corporation
WD1933 Data Sheet, Western Digital Corporation

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WD9914 General Purpose Interface Bus (GPIB) Controller

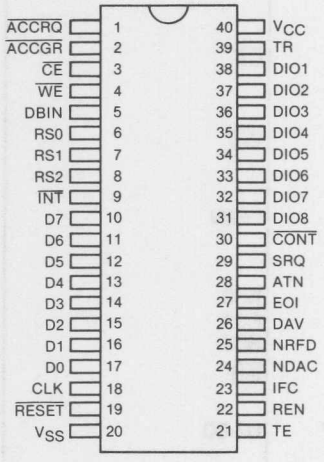
PRELIMINARY

FEATURES

- HANDLES ALL IEEE-488 1975/78 FUNCTIONS
- COMPATIBLE WITH IEEE-488A 1980 SUPPLEMENT
- TALKER AND LISTENER FUNCTION (T, TE, L, LE)
- AUTOMATIC SOURCE AND ACCEPTOR HANDSHAKES (SH, AH)
- CONTROLLER WITH PASS CONTROL
- SYSTEM CONTROLLER CAPABILITIES
- DEVICE TRIGGER AND DEVICE CLEAR CAPABILITIES (DT, DC)
- OPTIONAL AUTOMATICALLY CLEARED 'REQUEST SERVICE BIT'
- PARALLEL AND SERIAL POLL FACILITIES (PP)
- REMOTE/LOCAL FUNCTION WITH LOCAL LOCKOUT (RL)
- SINGLE OR DUAL PRIMARY ADDRESSING
- SECONDARY ADDRESS CAPABILITIES
- DIRECT INTERFACE TO SN75160/161/162 BUS TRANSCEIVERS WITH NO ADDITIONAL LOGIC
- COMPATIBLE WITH MOST MICROPROCESSORS
- DIRECT MEMORY ACCESS FACILITIES
- MEMORY-MAPPED MICROPROCESSOR INTERFACE
- SINGLE +5V SUPPLY
- COMPATIBLE WITH TMS9914A FEATURES

DESCRIPTION

The WD9914 provides an interface between a Microprocessor System and the General Purpose Interface Bus (GPIB) specified in the IEEE-488 1975/78 standards and the IEEE-488A 1980 supplement. The device is controlled and configured through 8-bit memory mapped registers and enables all aspects of the standards to be implemented, including talker, listener and controller.



PIN DESIGNATION

PIN DESCRIPTION

PIN NUMBER	SIGNAL NAME	I/O (TYPE)	DESCRIPTION
1	$\overline{\text{ACCRQ}}$	O(p/p)	ACCESS REQUEST: this pin becomes active (low) to request a direct memory access.
2	$\overline{\text{ACCGR}}$	I	ACCESS GRANTED: when received from the direct memory access control logic this enables the byte onto the data bus. ACCGR must be high when not participating in DMA transfer.
3	$\overline{\text{CE}}$	I	CHIP ENABLE: $\overline{\text{CE}}$ low allows access of read and write registers. If $\overline{\text{CE}}$ is high, D0-D7 are in high impedance unless $\overline{\text{ACCGR}}$ is low.
4	$\overline{\text{WE}}$	I	WRITE ENABLE: when active (low), indicates to the WD9914 that data is being written to one of its registers.
5	DBIN	I	DATA BUS IN: an active (high) state indicates to the WD9914 that a read is about to be carried out by the MPU.
6 7 8	RS0 RS1 RS2	I I I	REGISTER SELECT LINES: determine which register is addressed by the MPU during a read or write operation.
9	$\overline{\text{INT}}$	O(o/d) (no pullup)	INTERRUPT: sent to the MPU to cause a branch to a service routine.
10-17	D7-D0	I/O(p/p)	Data transfer lines on the MPU side of the device.
18	CLK	I	CLOCK Input: 500 kHz to 5 MHz. Need not be synchronous to system clock.
19	$\overline{\text{RESET}}$*	I	INITIALIZES the WD9914 at power-on.
20	V_{SS}		Ground reference voltage.
21	TE	O(p/p)	TALK ENABLE: controls the direction of the transfer of the line transceivers. Logically, it is: ($\overline{\text{CACS}}$ + TACS + EIO.ATN.($\overline{\text{CIDS}}$ + $\overline{\text{CADS}}$). $\overline{\text{SWRST}}$).
22	REN	I/O(o/d)	REMOTE ENABLE: sent by system controller to select control either from the front panel or from the IEEE bus.
23	IFC	I/O(o/d)	INTERFACE CLEAR: sent by the system controller to set the interface system into a known quiescent state. The system controller becomes the controller in charge.
24	NDAC	I/O(p/p)	NOT DATA ACCEPTED: handshake line. Acceptor sets this false (high) when it has latched the data from the I/O lines.
25	NRFD	I/O(p/p)	NOT READY FOR DATA: handshake line. Sent by acceptor to indicate readiness for the next byte.
26	DAV	I/O(p/p)	DATA VALID: handshake line controlled by source to show acceptors when valid data is present to the bus.
27	EOI	I/O(p/p)	END OR IDENTIFY: if ATN is false (high), this indicates the end of a message block. If ATN is true (low), the controller is requesting a parallel poll.

PIN DESCRIPTION

PIN NUMBER	SIGNAL NAME	I/O (TYPE)	DESCRIPTION
28	ATN	I/O(p/p)	ATTENTION: sent by controller in charge. When true (low), interface commands are being sent over the DIO lines. When false (high), these lines carry data.
29	SRQ	I/O(p/p)	SERVICE REQUEST: set true (low) by a device to indicate a need for service.
30	$\overline{\text{CONT}}$	O(p/p)	Indicates if a device is controller in charge. It is used to control direction of SRQ and ATN in pass control systems. Logically, it is (CIDS + CADS).
31	DIO8	I/O(p/p)	DIO8 through DIO1 are the data input/output lines on the GPIB side. These pins connect to the IEEE-488 bus via non-inverting transceivers.
32	DIO7	I/O(p/p)	
33	DIO6	I/O(p/p)	
34	DIO5	I/O(p/p)	
35	DIO4	I/O(p/p)	
36	DIO3	I/O(p/p)	
37	DIO2	I/O(p/p)	
38	DIO1	I/O(p/p)	
39	TR	O(p/p)	TRIGGER: activated when the GET command is received over the interface or the fget command is given by the MPU.
40	V_{CC}		Supply voltage (+5 V nominal).

(p/p) = push/pull output.
(o/d) = open drain output with internal pull up.
*The hardware RESET pin has the following effect on the WD9914:
— Serial and Parallel Poll registers cleared
— All clear/set auxiliary commands cleared except 'swrst'
— 'swrst' auxiliary command set. This holds the WD9914 in known states.

ARCHITECTURE

The block diagram of the internal architecture of the WD9914 is given in Figure 1. As previously stated, there are 13 MPU accessible registers of which 6 are read and 7 are write. These registers handle all communication between the IEEE-488 1975/78 bus and microprocessor.

Each register is accessed by putting the relevant address on lines RS0, RS1 and RS2 and performing a memory read ($\overline{WE}$ = 1 DBIN = 1) or memory write ($\overline{WE}$ = 0 DBIN = 0) operation. The register addresses and use of each bit is shown in Table 1 for the read registers and Table 2 for the write registers. A full description of each register is given in the following paragraphs.

Implementation of the functions described by the state diagrams of the IEEE-488 standard is carried out in the IEEE-488 state diagram block. Information is received from the IEEE bus and from the internal registers and is combined with the current status of the device (for example, Talker Active State, TACS) to produce the control signals to load registers or handle the handshake or bus management lines.

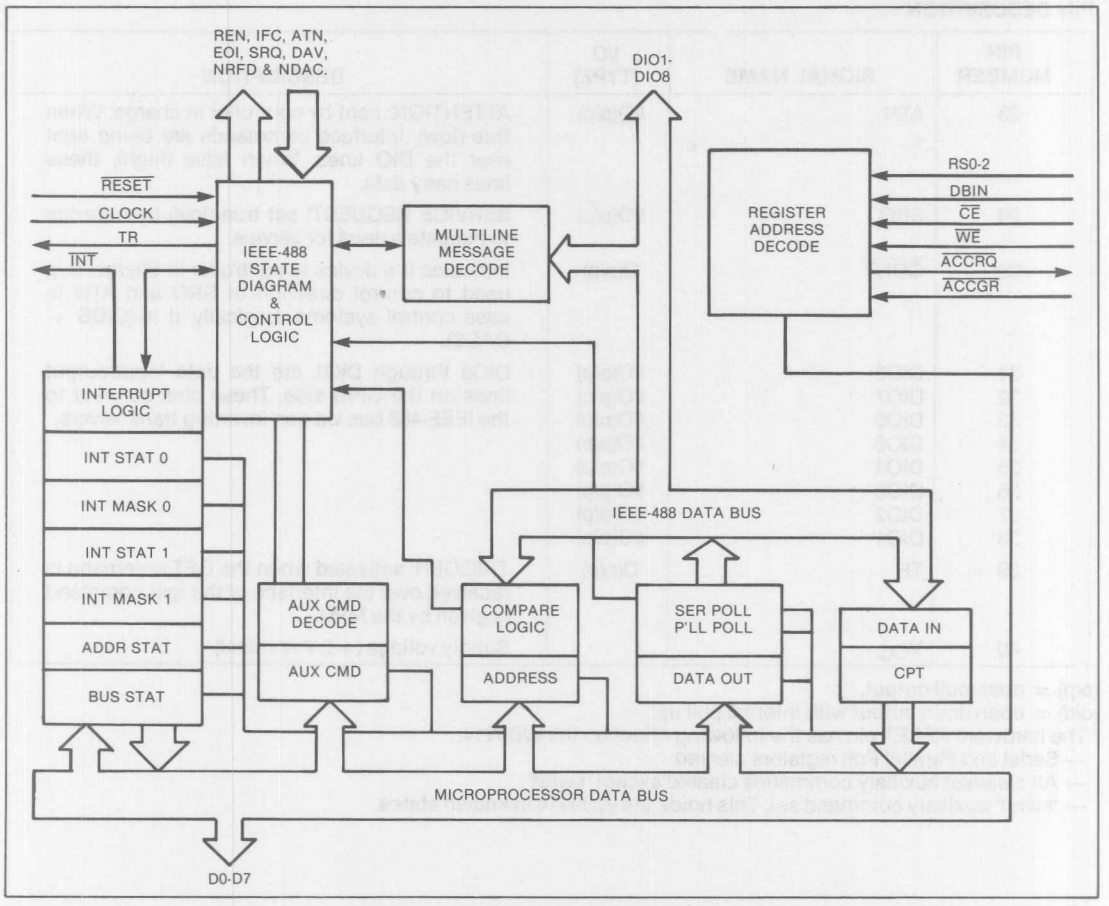


Figure 1. SIMPLIFIED BLOCK DIAGRAM

Table 1. WD9914 READ REGISTERS

ADDRESS				BIT ASSIGNMENT							
RS2	RS1	RS0	REGISTER NAME	D0	D1	D2	D3	D4	D5	D6	D7
0	0	0	Int Status 0	INT0	INT1	BI	BO	END	SPAS	RLC	MAC
0	0	1	Int Status 1	GET	ERR	UNC	APT	DCAS	MA	SRQ	IFC
0	1	0	Address Status	REM	LLO	ATN	LPAS	TPAS	LADS	TADS	ulpa
0	1	1	Bus Status	ATN	DAV	NDAC	NRFD	EOI	SRQ	IFC	REN
1	0	0	*								
1	0	1	*								
1	1	0	Cmd Pass Thru	DIO8	DIO7	DIO6	DIO5	DIO4	DIO3	DIO2	DIO1
1	1	1	Data In	DIO8	DIO7	DIO6	DIO5	DIO4	DIO3	DIO2	DIO1

*The WD9914 host interface data lines will remain in the high impedance state when these register locations are addressed. An Address Switch Register may therefore be included in the address space of the device at these locations.

Table 2. WD9914 WRITE REGISTERS

ADDRESS RS2	RS1	RS0	REGISTER NAME	BIT ASSIGNMENT D0	D1	D2	D3	D4	D5	D6	D7
0	0	0	Int Mask 0			BI	BO	END	SPAS	RLC	MAC
0	0	1	Int Mask 1	GET	ERR	UNC	APT	DCAS	MA	SRQ	IFC
0	1	0	*	xx	xx	xx	xx	xx	xx	xx	xx
0	1	1	Auxiliary Cmd	cs	xx	xx	f4	f3	f2	f1	f0
1	0	0	Address	edpa	dal	dat	A5	A4	A3	A2	A1
1	0	1	Serial Poll	S8	rsvl	S6	S5	S4	S3	S2	S1
1	1	0	Parallel Poll	PP8	PP7	PP6	PP5	PP4	PP3	PP2	PP1
1	1	1	Data Out	DIO8	DIO7	DIO6	DIO5	DIO4	DIO3	DIO2	DIO1

*This address is not decoded by the WD9914. A write to this location will have no effect on the device, as if a write had not occurred.

REGISTERS

Interrupt Mask and Status Registers 0

The Interrupt Mask and Interrupt Status registers operate independently of each other. The status bits will always be set when the appropriate events occur regardless of the state of the corresponding mask bit.

All interrupt bits, with the exception of INT0 and INT1 which are not storage bits, are edge triggered and are set when the appropriate condition becomes true. The storage bits are cleared immediately after the corresponding Interrupt Status Register is read by the host MPU. If an interrupt condition becomes true during this read operation, then the event is stored. The corresponding bit is set when the read operation ends, hence no interrupts are lost. In addition to being cleared by a read operation, the BO interrupt is also cleared by writing to the Data Out Register, and the BI interrupt is cleared by reading the Data In Register.

The interrupt status bits are cleared and held in the O condition while Software Reset (swrst) is set.

The corresponding bit of the Interrupt mask register must be set to a 1 if an interrupt status bit is to cause an external interrupt ($\overline{INT}$ Low) when it is set (i.e., $\overline{INT}$ = $\overline{INT}$ STATUS.INT MASK). The mask register is not cleared by 'swrst' or the Hardware Reset pin ($\overline{RESET}$) and will power on in a random state. It must, therefore, be written to by the host MPU before 'swrst' is cleared to avoid extraneous interrupts.

The INT0 and INT1 bits of the Interrupt Status Register are not true status bits. INT1 will be true if there are any unmasked interrupt status bits set to a 1 in Interrupt Status Register 1. INT0 will be true if any of bits 2-7 of Interrupt Status Register 0 are unmasked and set to a 1. If either INT1 or INT0 is true, then the external interrupt pin ($\overline{INT}$) will be pulled low provided that the Disable All Interrupts feature (dai) has not been set.

The individual bits of Interrupt Status and Interrupt mask Register 0 are described are in the following paragraphs. The conditions which set these bits, shown in parentheses, are given in terms of the state diagrams. Each bit is set on the rising edge of the condition shown.

INTERRUPT MASK/STATUS REGISTER 0

xx	xx	BI	BO	END	SPAS	RLC	MAC	INT	MASK 0
INT0	INT1	BI	BO	END	SPAS	RLC	MAC	INT	STATUS 0
D0	D1	D2	D3	D4	D5	D6	D7		MPU BUS

NOTE: A 0 masks and a 1 unmasks the bits in the interrupt mask registers.

INT1 — This will be a 1 when an unmasked status bit in Interrupt Status Register 1 is set to a 1.

INT0 — This will be a 1 when any of bits 2-7 of Interrupt Status Register 0 is unmasked and set to a 1.

BI — Byte In. A data byte has been received in the Data In register. If the mask bit is not set, then no interrupt is generated but a RFD holdoff will still occur before the next data byte is accepted. If the Shadow Handshake feature is used, then this status bit will not be set. This bit is cleared by reading the Data In Register as well as after Interrupt Status Register 0 has been read. (Set On: ACDS1.LACS)

BO Byte Out. This is set when the Data Out Register is available to send a byte over the GPIB. This byte may be either a command if the device is a controller or data if the device is a talker. It is set when the device becomes an active talker or controller but will not occur if the Data Out register has been loaded with a byte which has not been sent. Subsequently, it will occur after each byte has been sent and the WD9914 returns to SGNS. This bit is cleared by writing to the Data Out Register as well as by reading Interrupt Status Register 0. (Set On: SGNS.CACS + SGNS.TACS.$\overline{SHFS}$)

NOTE:
When a controller addresses itself as a talker and then goes to standby, there will be a momentary transition of the source handshake into SIDS before TACS becomes true and it reenters SGNS. Under these circumstances, the WD9914 is guaranteed to give a BO interrupt on reentering 'SGNS'.

END This indicates that a byte just received by a listener was the last byte in a string, that is, it was received with the EOI line true. It is set at the same time as the BI interrupt. (Set On: (ACDS1.LACS.EOI)

SPAS This indicates that the WD9914 has requested service via rsv1 or rsv2 (in the Serial Poll Register or Auxiliary Command Register) and has been polled in a serial poll. It is set on the false transition of STRS when the serial poll status byte is sent. (Set On: STRS.SPAS.(APRS1 + APRS2)

RLC Remote/Local Change. This is set by any transition between local and remote states in the Remote/Local function. (Set On: (LOCS-REMS) + (REMS-LOCS) + (LWLS-RWLS) + (RWLS-LWLS)

MAC My Address Change. This indicates that a command has been received from the GPIB which has resulted in the addressed state of the WD9914 to change. It will not occur if secondary addressing is being used, nor indicate that the WD9914 has been readdressed on its other primary address. (Set On: ACDS1. (MTA.TA$\overline{DSUNT}$ + OTA.$\overline{TADS}$ + MLA.LADS + UN.$\overline{LADS}$)

Interrupt Mask and Status Registers 1

The operation of Interrupt Mask and Status Register 1 is similar to that of Interrupt Mask and Status Register 0 except that all bits are true storage bits. The status bits are cleared only following the register being read and by 'swrst'.

There is one distinct group of interrupts in this register: GET, UNC, APT, DCAS, MA. These are all set in response to commands received over the bus and if unmasked, a Data Accepted (DAC) holdoff will occur when the interrupt in question is set. It may be released with a 'dacr' auxiliary command. This is further discussed in Section 3.2.

The mask bit of the APT Interrupt is further used in the talker and listener functions. When the interrupt is unmasked, the talker and listener functions of the WD9914 implement the extended talker and extended listener functions of IEEE-488. Otherwise these functions implement the talker and listener functions of IEEE-488.

The individual bits of Interrupt Status and Interrupt Mask Register 1 are described below. The conditions which set these bits, shown in parentheses, are given in terms of the state diagrams.

INTERRUPT MASK/STATUS REGISTER 1

GET	ERR	UNC	APT	CDAS	MA	SRQ	IFC	INT	MASK 1
GET	ERR	UNC	APT	DCAS	MA	SRQ	IFC	INT	STATUS 1
D0	D1	D2	D3	D4	D5	D6	D7	MPU	BUS

GET This is set if a Group Execute Trigger command is received. A DAC holdoff occurs if the interrupt is unmasked. The TR pin becomes high when this command is received and persists high for the duration of a DAC holdoff if one occurs. If the interrupt is masked, the TR pin becomes high for approximately five clock cycles. (Set On: GET.LADS.ACDS1)

ERR Error. This is set if the source handshake becomes active and finds that the NDAC and NRFD lines are both high. This indicates that, for whatever reason, there are no acceptors on the bus. (Set On: SERS)

UNC Unrecognized Command. This is set if a command has been received which has no meaning to the WD9914. Unrecognized addressed commands will only cause this interrupt if the device is LADS except for TCT which will only interrupt in TADS. Secondary commands will only cause this interrupt if the 'pts' auxiliary command has been set previously. A DAC holdoff will occur if this interrupt is unmasked which effectively enables the command pass through feature. Unrecognized commands may be inspected in the Command Pass Through Register before this holdoff is released. (Set On: ACDS1. (UCG.$\overline{LLO}$. $\overline{SPE}$.

$\overline{SPD.DCL}$ + ACG.$\overline{GET.GTL.SCD.TCT.LADS}$ + TCT.TADS + SCG.pts)

APT — Address Pass Through. Unmasking this interrupt enables secondary addressing. It is set if a secondary command is received provided that the last primary command received was a primary talk or listen address of the WD9914. A DAC holdoff will occur and the secondary address may be read from the Command Pass Through Register. The holdoff may be released by a 'dacr' auxiliary command and the 'cs' bit of the Auxiliary Command Register is used to indicate that a valid (cs = 1) or an invalid (cs = 0) secondary has been identified by the host MPU. (Set On: ACDS1.SCG.(LPAS + TPAS)

DCAS — Device Clear Active State. This is set when a device clear command (DCL) is received or when a selected device clear (SDC) is received with the WD9914 in LADS. This will cause a DAC holdoff if unmasked. (Set On: ACDS1.(DCL + SDC.LADS)

SRQ — Service Request. This is provided for the benefit of the controller which should execute a serial poll in response to this interrupt. It is set when the SRQ line becomes true. (Set On: SRQ.($\overline{CIDS}$ + $\overline{CADS}$)

MA — My Address. This is set when the WD9914 recognizes its primary talk or listen address. A DAC holdoff will occur if this is unmasked. (Set On: (MLA + MTA).$\overline{SPMS.aptmk}$)

IFC — Interface Clear. This is provided for the benefit of devices which are not the System Controller. It is set when the IFC line becomes true and indicates that the WD9914 has been returned to an idle state. If the device is the System Controller, then the IFC interrupt is not set. (Set On: IFCIN)

Address Status Register

REM	LLO	ATN	LPAS	TPAS	LADS	TADS	ulpa
D0	D1	D2	D3	D4	D5	D6	D7

MPU BUS

REM — The device is in the remote state
LLO — Local lockout is in operation
ATN — The attention line is low (true) on the bus
LPAS — WD9914 is in the listener primary addressed state
TPAS — WD9914 is the talker primary addressed state
LADS (or LACS) — The device is addressed to listen
TADS (or TACS) — The device is addressed to talk
ulpa — This bit shows the LSB of the last address recognized by the WD9914.

Address Register

edpa	dal	dat	A5	A4	A3	A2	A1
D0	D1	D2	D3	D4	D5	D6	D7

edpa — Enable dual primary addressing mode
dal — Disable listener function
dat — Disable talker function
A5-A1 — Primary address of the WD9914.

Bits A5-A1 of this register contain the primary address of the device (denoted AAAAA in Table 19). IEEE-488 1975/78 does not allow a device to be assigned the value 11111 for bits A5-A1. When 'swrst' is true at power-up or if set by the host MPU, the WD9914 is held in an idle state. During this time the host MPU may load the primary address of the device into these bits. Often this will be read from an Address Switch Register.

The 'edpa' bit is used to enable the dual addressing mode of the WD9914. It causes the LSB of the address to be ignored by the address comparator giving two consecutive primary addresses for the device. The address by which the WD9914 was selected is indicated by the 'ulpa' bit of the Address Status Register.

The Address Register is not cleared by 'swrst' or hardware reset.

Auxiliary Command Register

cs	xx	xx	F4	F3	F2	F1	F0
D0	D1	D2	D3	D4	D5	D6	D7

f4-f0 — Auxiliary command select (see Table 3)
cs — Clear or set the feature (where applicable)

Auxiliary commands are used to enable and disable most of the selectable features of the WD9914 and to initiate many of the actions of the device. The desired feature is selected by writing a byte to this register with the appropriate value in bits f4-f0. These values are given in Table 3.

The 'cs' bit is used in most cases when the feature selected by f4-f0 is of the clear/set type. The feature is enabled if 'cs' = '1' and disabled if 'cs' = '0'. The holdoff on all data (hdfa) feature is an example of such a feature. Other auxiliary commands initiate an action of the WD9914, such as release RFD holdoff (rhdf). In most cases, the 'cs' bit is unused and ignored by these commands.

All the clear/set auxiliary commands are cleared by the hardware RESET pin except 'swrst,' which is set true by RESET.

The force group execute trigger (fget) and return to local (rtl) auxiliary commands have a clear/set mode of operation and a pulsed mode of operation. They behave as normal clear/set features, but if they are written with 'cs' = '0' when they have not been previously set, then they will pulse true. Using the 'fget' command in this manner will produce a pulse of approximately 1 μs at the TR pin (with a 5 MHz clock). The 'rtl' command used in this way will cause a return to one of the local states (assuming local lockout is not in force) but the WD9914 may reenter the remote state next time the listen address occurs.

Table 3. AUXILIARY COMMANDS

c/s	f4	f3	f2	f1	f0	MNEMONIC	FEATURES
0/1	0	0	0	0	0	swrst	Software reset
0/1	0	0	0	0	1	dacr	Release DAC holdoff
na	0	0	0	1	0	rhdf	Release RFD holdoff
0/1	0	0	0	1	1	hdfa	Holdoff on all data
0/1	0	0	1	0	0	hdfe	Holdoff on EOI only
na	0	0	1	0	1	nbaf	New byte available false
0/1	0	0	1	1	0	fget	Force group execute trigger
0/1	0	0	1	1	1	rti	Return to local
na	0	1	0	0	0	feoi	Send EOI with next byte
0/1	0	1	0	0	1	lon	Listen only
0/1	0	1	0	1	0	ton	Talk only
na	0	1	0	1	1	gts	Go to standby
na	0	1	1	0	0	tca	Take control asynchronously
na	0	1	1	0	1	tcs	Take control synchronously
0/1	0	1	1	1	0	rpp	Request parallel poll
0/1	0	1	1	1	1	sic	Send interface clear
0/1	1	0	0	0	0	sre	Send remote enable
na	1	0	0	0	1	rqc	Request control
na	1	0	0	1	0	rlc	Release control
0/1	1	0	0	1	1	dai	Diable all interrupts
na	1	0	1	0	0	pts	Pass through next secondary
0/1	1	0	1	0	1	stdl	Short TI settling time
0/1	1	0	1	1	0	shdw	Shadow handshake
0/1	1	0	1	1	1	vstdl	Very short T1 delay
0/1	1	1	0	0	0	rsv2	Request Service Bit 2

DESCRIPTION OF AUXILIARY COMMANDS

Software Reset (swrst) 0/1xx00000

Setting this command causes the WD9914 to be returned to a known idle state during which it will not take part in any activity on the GPIB. This auxiliary command is set by the power-on RESET and the chip should be configured while 'swrst' is set. Configuration should include writing the address of the device into the Address Register, writing mask values into the Interrupt Mask Registers and selecting the desired features in the Auxiliary Command Register and Address Register. After this, 'swrst' may be cleared at which point the device becomes logicaly existent on the GPIB. The Serial Poll Register and Parallel Poll Registers may also be written in this period but this

is not necessary if there is no status to report as both of these are cleared by the power-on RESET pin. Table 4 lists the various states and other conditions forced by 'swrst'.

Table 4. SOFTWARE RESET CONDITIONS

MNEMONIC	DESCRIPTION
SIDS	Source idle state
AIDS	Acceptor idle state
TIDS	Talker idle state
TPAS	Talker primary idle state
LIDS	Listener idle state
LPAS	Listener primary state
NPRS	Negative poll response state
LOCS	Local state
CIDS	Controller idle state
SPIS	Serial poll idle state
PPSS	Parallel poll standby state
ADHS	DAC holdoff state
AEHS	RFD holdoff on end state
SHFS	Source holdoff state
ENIS	END idle state

NOTES: 1. See Section 3 for definition of above.
2. All interrupt status bits are held in a 0 state, but interrupt mask bits are not affected.

Release DAC Holdoff (dacr)0/1xx00001

The Data Accepted (DAC) holdoff allows time for the host microprocessor to respond to unrecognized commands, secondary addresses, and device trigger or device clear commands. The holdoff is released by the MPU when the required action has been taken. Normally the command is loaded with the clear/set bit at zero; however, when used with the address pass through feature CS is set to one if the secondary address was valid or to zero if invalid see APT interrupt.

Release RFD Holdoff (rhdf)naxx00010

Any Ready For Data (RFD) holdoff caused by a 'hdfa' or 'hdfe' is released.

Holdoff on All Data (hdfa)0/1xx00011

A Ready For Data (RFD) holdoff is caused on every data byte until the command is loaded with CS set to zero. The handshake must be completed after each byte has been received by the MPU using the 'rhdf' command.

Holdoff on End (hdfe)0/1xx00100

A RFD holdoff will occur when an end of data string message (EOI tru with ATN false) is received over the interface. This holdoff must be released using 'rhdf'.

Set New Byte Available False (nbaf)naxx00101

If a talker is interrupted before the byte just stored in the data out register is sent over the interface, this byte will normally be transmitted as soon as the ATN line returns to the false state. If, as a result of the interrupt, this byte is no longer required, its transmission may be suppressed using the 'nbaf' command.

Force Group Execute Trigger (fget)0/1xx00110

The state of the TR output from the WD9914 is affected when this command is executed. If the CS bit is zero, the line is pulsed high for approximately 5 clock cycles (1 μs at 5 MHz). If CS is one, the TR line goes high until 'fget' is sent with CS equal to zero. No interrupts or handshakes are initiated.

Return to Local (rtl)0/1xx00111

Provided the local lockout (LLO) has not been enabled, the remote/local status bit is reset, and an interrupt is generated (if enabled to inform the host microprocessor that it should respond to the front panel controls. If the CS bit is set to one the 'rtl' command must be cleared (CS = 0) before the device is able to return to remote control. If CS is set to zero, the device may return to remote without first clearing 'rtl'.

Force End or Identify (feoi)naxx01000

This command causes the EOI message to be sent with the next data byte. The EOI line is then reset.

Listen Only (lon)0/1xx01001

The listener state is activated until the command is sent with CS set to 0 or until deactivated by a bus command.

Talk Only (ton)0/1xx01010

The talker state is activated until the command is sent with CS set to 0 or until deactivated by a bus command.

NOTE:
'ton' and 'lon' are included for use in systems without a controller. However, where the WD9914 is being used as a controller, it utilizes the 'lon' and 'ton' functions to set itself up as a listener or talker, respectively. Care must therefore be taken to ensure these functions are reset if sending UNL or OTA.

Go to Standby (gts)naxx01011

Issued by the controller in charge to set the ATN line false.

Take Control Synchronously (tcs)naxx01101

Control is again taken by the controller in charge, and ATN is asserted. If the controller is not a true listener, the shadow handshake command must be used to monitor the handshake lines so that the WD9914 is synchronous with the talker/listeners and only sends ATN true at the end of byte transfer. This ensures that no data is lost or corrupted.

Request Parallel Poll (rpp)0/1xx01110

This is executed by the controller in charge to send the parallel poll command over the interface (the WD9914 must be in the Controller Active State so that the Attention line is asserted). The poll is completed by reading the Command Pass Through Register to obtain the status bits, then sending 'rpp' with the CS bit at zero.

Take Control Asynchronously (tca)naxx01100

This command is used by the controller in charge to set the attention line true and to gain control of the interface. The command is executed immediately and data corruption or loss may occur if a talker/listener is in the process of transferring a data byte.

Send Interface clear (sic)0/1xx01111

The IFC line is set true when this command is sent with CS set to one. This must only be sent by the system controller and should be reset (CS = 0) after the IEEE minimum time for IFC has elapsed (100 μs). The system controller is put into the controller active state.

Send Remote Enable (sre)0/1xx10000

Issued by the system controller to set the REN line true and send the remote enable message over the interface, REN is set false by sending 'sre' with CS at zero.

Request Control (rqc)naxx10001

When the TCT command has been recognized via the unidentified command pass through, this command is sent by the MPU. The WD9914 waits for the ATN line to go false and then enters the controller active state (CACS).

Release Control (ric)naxx10010

This command is used after TCT has been sent and handshake completed to release the ATN line and pass control to another device.

Disable All Interrupts (dai)0/1xx10011

The $\overline{\text{INT}}$ line is disabled, but the interrupt registers and any holdoffs selected are not affected.

Pass Through Next Secondary (pts)naxx10100

This feature may be used to carry out a remote configuration of a parallel poll. The parallel poll configure command (PPC) is passed through the WD9914 as an unrecognized addressed command and is identified by the MPU. The 'pts' command is loaded, and the next byte received by the WD9914 is passed through via the Command Pass Through Register. This would be the parallel poll enable (PPE), which is read by the microprocessor.

Set T1 Delay (std1)1xx10101

The T1 delay time can be set to 6 clock cycles (1.2 μs at 5 MHz) if this command is sent with the CS bit at one. The TI delay time is 11 clock cycles (2.2 μs at 5 MHz) following a power-on reset or if the command is sent with CS set to zero.

Shadow Handshake (shdw)0/1xx10110

This feature enables the controller in charge to carry out the listener handshake without participating in a data transfer. The Data Accepted line (DAC) is pulled true a maximum of 3 clock cycles after Data Valid (DAV) is received, and Not Ready For Data (NRFD) is allowed to go false as soon as DAV is removed.

The shadow handshake function allows the 'tcs' command to be synchronized with the Acceptor Not Ready State (ANRS) so that ATN can be re-asserted without causing the loss or corruption of data byte. The END interrupt can also be received and causes a RFD holdoff to be generated.

Very Short T1 Delay (vstd1)0/1xx10111

If this feature is enabled, the GPIB settling time (T1) will be reduced to 3 clock cycles (600 ns at 5 MHz) on the second and subsequent data bytes when ATN is false. Otherwise, the GPIB settling time is determined by the std1 feature.

Request Service Bit 2 (rsv2)0/1xx11000

The rsv2 bit performs the same function as the rsv1 bit but provides a means of requesting service which is independent of the Serial Poll Register.

This allows minor updates to be made to the Serial Poll Register without affecting the state of the request service.

In addition, rsv2 is cleared when the serial poll status byte is sent to the controller during a serial poll. It is therefore used in situations where a service request is simply a request from an instrument for the controller to poll its status. As soon as this happens, rsv2 is cleared since the reason for requesting service has been satisfied. This eliminates the burden of clearing the bit from the host MPU but also guarantees that rsv2 is cleared before another serial poll can occur. If this were not so, there would be a possibility of a second status byte being sent with the RQS message true, which could result in confusion for the controller. (rsv2 is cleared on: SPAS.(APRS1 + APRS2).STRS).

Bus Status Register

ATN	DAV	NDAC	NRFD	EOI	SRQ	IFC	REN	
D0	D1	D2	D3	D4	D5	D6	D7	MPU BUS

The host MPU may examine the status of the GPIB management lines at the time of reading.

The IFC bit of this register does not indicate a true value if the device is a system controller using the 'sic' auxiliary command.

Serial Poll Register

S8	rsv1	S6	S5	S4	S3	S2	S1	
DIO8	DIO7	DIO6	DIO5	DIO4	DIO3	DIO2	DIO1	GPIB
D0	D1	D2	D3	D4	D5	D6	D7	MPU BUS

S8, S6-S0 Device status
rsv1 Request service bit 1

Bits S8, S6-S1 of this register are sent out over the GPIB when the device is addressed during a serial poll. They are cleared by a hardware reset but not by 'swrst' and may therefore be set up during configuration of the chip. These bits are fully double buffered and if the register is written to while the device is addressed during a serial poll (serial poll active state, SPAS), the value written is saved, and these bits are updated when SPAS is terminated.

The rsv1 bit provides an input to the service request function of the WD9914 and is used to instruct this to request that the controller service the device. When rsv1 is set true, the SRQ line is pulled true on the GPIB, and the controller typically responds by setting up a serial poll to obtain the status of all instruments on the bus that may require service. When the WD9914 is addressed to send its status byte, SRQ is set false, and the status byte is sent with the RQS message true on DIO7. The rsv1 bit must then be cleared and set true again if service is to be requested a second time. The SPAS interrupt is set immediately following the status byte being sent.

The rev1 bit is also cleared by the hardware reset pin but not by 'swrst'. It is not double-buffered but the service request function comprehends changes in the state of rsv1 while the device is in SPAS. The Serial Poll Register may therefore be written to any time.

Command Pass Through Register

DIO8	DIO7	DIO6	DIO5	DIO4	DIO3	DIO2	DIO1	GPIB
D0	D1	D2	D3	D4	D5	D6	D7	MPU BUS

This provides a means of directly inspecting the GPIB data lines (DIO(8-1)). It has no storage and should only be used when the data lines are known to be in a steady state such as will occur during a DAC holdoff or in CPWS during a parallel poll. It is used to read unrecognized commands and secondaries following a UNC interrupt or to read secondary addresses following an APT interrupt. In addition, an active controller uses this register to read the results of a parallel poll at least 2μs after setting the 'rpp' auxiliary command.

Parallel Poll Register

PP8	PP7	PP6	PP5	PP4	PP3	PP2	PP1	
DIO8	DIO7	DIO6	DIO5	DIO4	DIO3	DIO2	DIO1	GPIB
D0	D1	D2	D3	D4	D5	D6	D7	MPU BUS

When a controller initiates a parallel poll, the contents of this register are presented to the GPIB data lines. If all bits of the register are cleared, then none of the lines DIO(8-1) will be pulled low during a parallel poll which corresponds to the Parallel Poll Idle State (PPIS) of IEEE-488. If it is desired to participate in a parallel poll, then the bit corresponding to the desired parallel poll response is set to a 1.

The Parallel Poll Register is fully double buffered. If it is written to during a parallel poll, the new value is held until the parallel poll ends, at which point the register is updated. This permits the host MPU to update the parallel poll response completely asynchronously to the GPIB.

If this register is cleared by the hardware RESET pin but not by 'swrst,' it may be loaded while the chip is being configured with 'swrst' set.

Data In Register

DIO8	DIO7	DIO6	DIO5	DIO4	DIO3	DIO2	DIO1	GPIB
D0	D1	D2	D3	D4	D5	D6	D7	MPU BUS

This register is used to hold data received by the WD9914 when it is a listener. It is loaded during Accept Data State (ACDS1) and, following this, an RFD holdoff will occur. This will normally be released when the byte is read by the host MPU, but if the Holdoff On All Data (hdfa) feature is selected, this holdoff must be released by the 'rhdf' auxiliary command.

If the Holdoff On End (hdfe) feature is selected, the RFD holdoff will be released by reading the Data In Register. But if the EOI line is true when the byte is received, reading the data byte will not release the holdoff and rhdf must be used.

As the Data In Register is loaded, the BI interrupt is set. The END interrupt is set simultaneously if the byte is accompanied by a true EOI line.

Data Out Register

DIO8	DIO7	DIO6	DIO5	DIO4	DIO3	DIO2	DIO1	GPIB
D0	D1	D2	D3	D4	D5	D6	D7	MPU BUS

The Data Out register is used by a controller or talker for sending interface messages and device dependent messages. When the WD9914 enters the Talker Active State (TACS) or the Controller Active State (CACS), the contents of the Data Out Register are presented to the GPIB data lines (DIO(8-1)), and the byte is sent over the bus under the control of the Source Handshake. Each time a byte is written, the source handshake is enabled, and the byte is sent. If the handshake is interrupted before the byte can be sent, then it will be sent next time the Source Handshake becomes active unless a new byte available false (nbaf) auxiliary command is written. This has the effect of clearing an unsent byte from the Data Out Register, and although the register itself is not cleared the WD9914 behaves as if it had not been loaded.

Each time the source handshake becomes active and there is no unsent byte in the Data Out Register, a BO interrupt will occur informing the host MPU that the Data Out Register is available for use.

The Data In Register and Data Out Register operate independently. The Data Out Register is not double buffered, and its contents are output directly to the data lines of the GPIB.

DIRECT MEMORY ACCESS

The WD9914 can operate in DMA using the $\overline{\text{ACCRQ}}$ (DMA request) and $\overline{\text{ACCGR}}$ (DMA grant) DMA handshake lines. The operation is automatic within the WD9914 and needs no 'mpu' configuration.

The $\overline{\text{ACCRQ}}$ signal is set by (BO.$\overline{\text{CACS}}$ + BI) and can therefore not be used by a controller while ATN is asserted. It is reset by 'swrst' readin data in register, writing to the data out register and $\overline{\text{ACCGR}}$. It is not cleared by reading interrupt status register 0.

If using DMA, the internal CE and addressing is disabled by the $\overline{\text{ACCGR}}$ signal going low and $\overline{\text{ACCGR}}$ will automatically address either the data in register (DBIN = 0) or the data out register (DBIN = 1).

NOTE:
The sense of DBIN is inverted for DMA operation.

At the end of a DMA read from memory sequence, the $\overline{\text{ACCRQ}}$ will be left low (also BO bit set). It may be necessary for the 'mpu' to clear this in some circumstances, e.g., starting DMA write to memory sequence.

In DMA it is recommended that the MA interrupt be unmasked to prevent errors due to interrupted data streams.

If DMA is not being utilized, the $\overline{\text{ACCGR}}$ signal must be held high. In this case, the $\overline{\text{ACCRQ}}$ signal can be used as a separate interrupt line for BO and BI. This allows faster 'mpu' transfers to take place as it is not necessary to read the interrupt register to find the cause of the interrupt. Figure 2 shows a typical DMA configuration.

TERMINAL ASSIGNMENTS AND FUNCTIONS

The IEEE-488 standard uses the negative logic convention for the GPIB lines. The FALSE state (0) is represented by a high voltage (>2.0 V); the TRUE state (1) is represented by a low voltage (>0.8 V). The GPIB terminations of the WD9914 are in agreement with this convention. For example, if Data Valid is true (1), the DAV line is pulled low by the device. These terminations are connected to the bus via noninverting buffers to obtain the correct signal polarity.

Note that the terminations on the microprocessor side of the device are in positive logic (true state (1) = high voltage : false state (0) = low voltage). This is in agreement with the logic convention used by most microprocessors. Thus if:

DO(MSB) D7(LSB)

0	1	1	0	1	0	0	1

is written into the data out register, it will appear as:

DIO8(MSB) DIO1(LSB)

HIGH	LOW	LOW	HIGH	LOW	HIGH	HIGH	LOW

on the IEE-488 D10 lines.

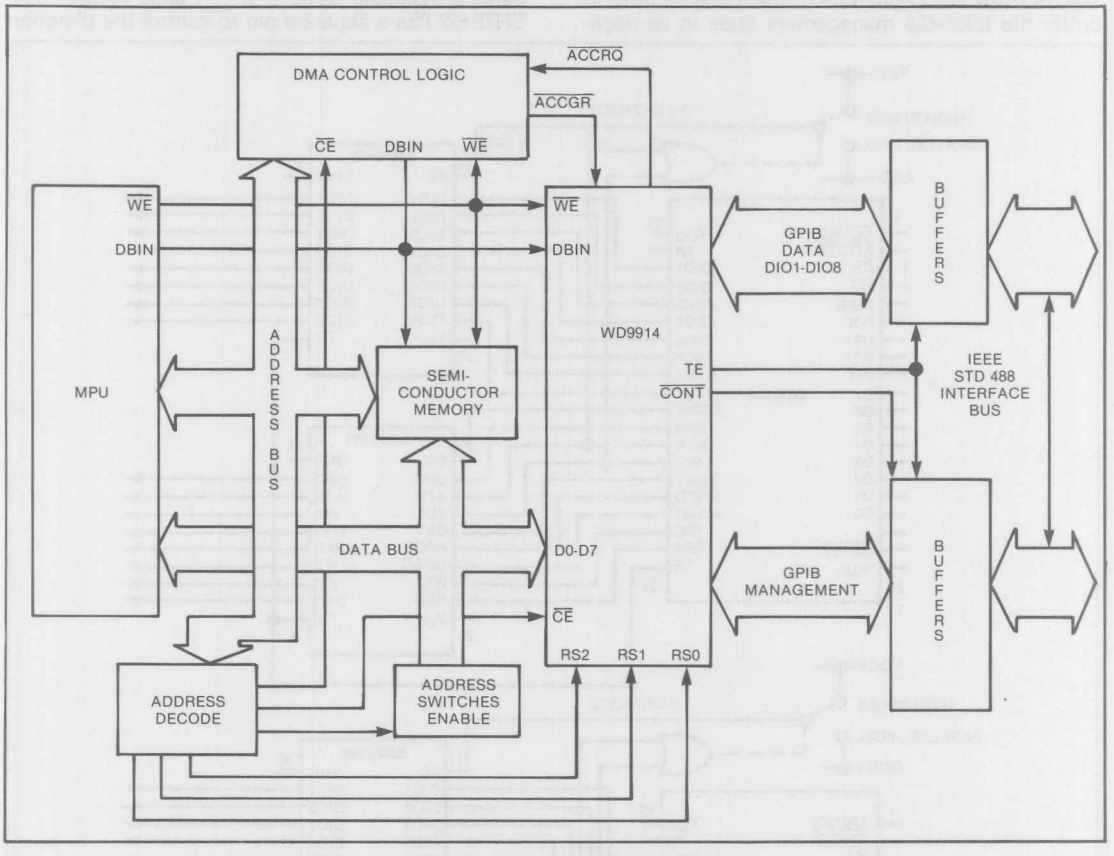


Figure 2. DMA CONFIGURATION

TRANSCEIVER CONNECTIONS

There are three linear transceivers designed to work with the WD9914: The SN75160, SN75161, and SN75162. Data sheets for these are included as Appendix C. Figure 3 shows the possible transceiver connections. Note that there is a corresponding pinout between the WD9914 and the transceivers. This allows the whole GPIB interface to be laid out in a very small area of printed circuit board.

The SN75160 is a 20 pin device used to buffer the IEEE-488 data lines (DIO(8-1)) in all applications. The direction of the buffers is controlled by the Talk Enable (TE) output of WD9914. This active high signal becomes true whenever there is an interface function of the WD9914 not sending the NUL message on DIO(8-1), that is, when the device is in TACS, CACS, SPAS, or PPAS. The Pull-Up Enable (PE) input of the SN75160 is an active high input which selects whether the 'DIO(8-1)' lines are driven by open collector or push/pull buffers. A push/pull buffer is required if faster data rates are required and the 'stdl' and/or the 'vstdl' features are used. Open collectors must be used if parallel polling is being used in a particular GPIB environment. If only one of these features is desired the PE input may be hardwired otherwise it must be derived from ATN and EIO, as shown in Figure 3.

The SN75161 is a 20-pin device used to buffer the IEEE-488 management lines. It may be used for a talker/listener device or for a controller which does not pass control. The direction of the handshake line buffers NRFD, NDAC, DAV are again controlled by the TE signal. However, the SRQ, ATN, REN, and IFC buffers are controlled by the DC input of the SN75161, which connects to the Controller Active ($\overline{\text{CONT}}$) output of the WD9914. $\overline{\text{CONT}}$ becomes low whenever the WD9914 is an active controller, that is, when it is not in CIDS or CADS. The SN75161 also includes the logic necessary to control the direction of the EOI buffer. This is dependent on the TE signal when ATN is false (high) and the DC signal when ATN is true (low).

The SN75162 is a 22-pin device which may be used to buffer the IEEE-488 management lines in all applications including devices which pass control. The SN75162 has a separate pin to control the direction

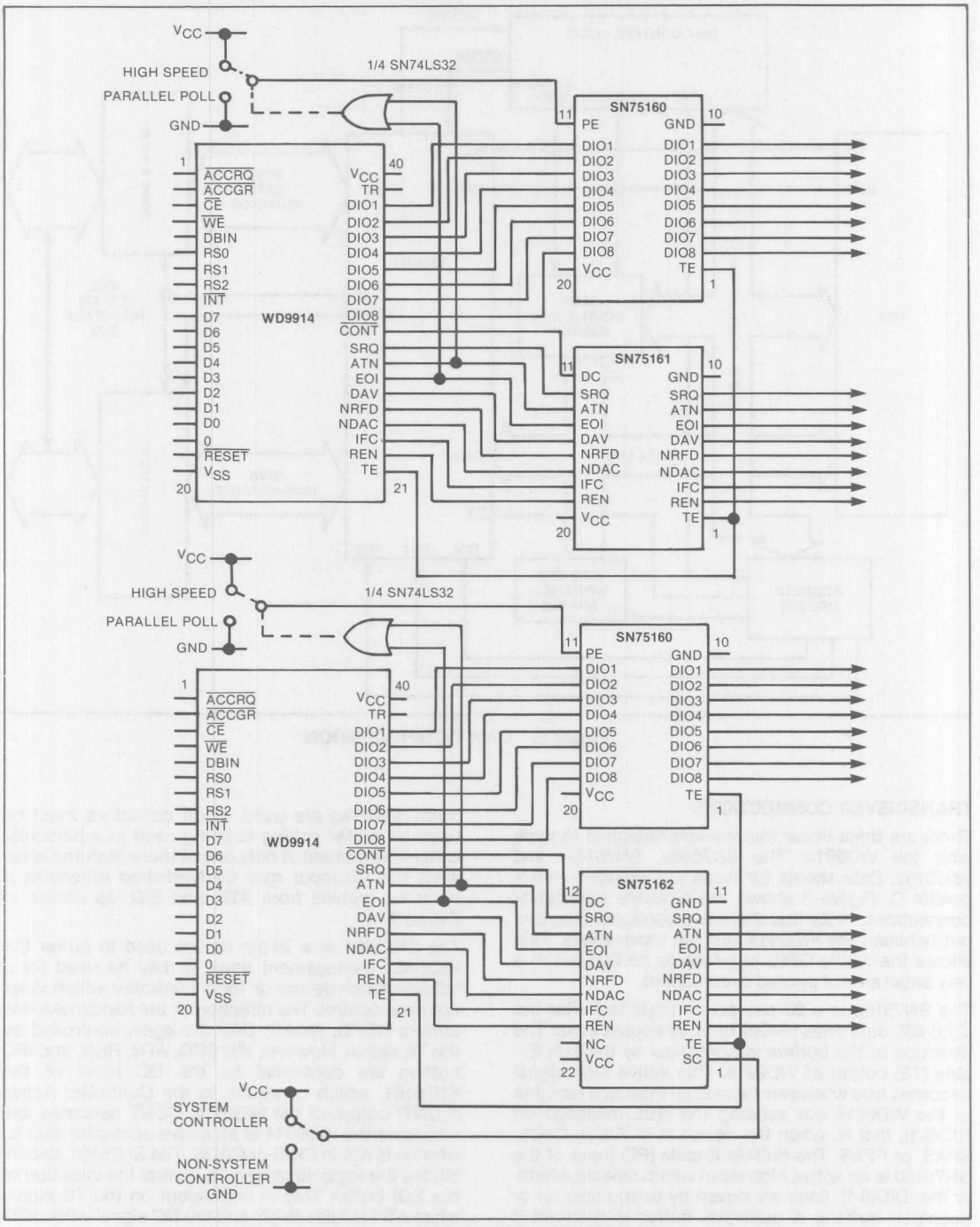


Figure 3. TRANSCEIVER CONNECTIONS

of the REN and IFC buffers, but is otherwise identical to the SN75161 in all other respects. This input is the System Controller input (SC) which may be hardwired or switchable to determine whether or not the instrument in question is a system controller or not. Note that a device which has its buffers configured as a non-system controller should never use the 'sic' and 'sre' auxiliary commands.

STATE DIAGRAM IMPLEMENTATION

This section presents the state diagrams for the WD9914.

Where equivalent, the names of WD9914 states are the same as those of IEEE-488. In some cases, IEEE-488 states have been divided, for example, ACDS of the IEEE-488 has been split into ACDS1 and ACDS2. The convention of lower case characters for local messages and upper case for remote messages and interface states is retained.

State diagrams with remote message outputs are supplemented with tables. T is used to represent a true output and F a false output. Parentheses denote a passive output; otherwise, it is active. The outputs shown are the values presented to the bus and assume the use of the SN75160 and SN75161 or SN75162 transceivers or their logical equivalents. The symbol (NUL) associated with DIO(1-8) indicates that each of these lines is sent passive false by the function in question.

NOTE:
An arrow into a state with no state as its origin represents a transition from every other state on the diagram. Note, however, that this does not imply that all exit conditions from the destination state are overridden. If such an entry condition is true and, simultaneously, an exit condition is true then this represents an illegal situation and should be avoided. Such situations will not occur in normal operation of the device.

No maximum timings are discussed. The WD9914 with its recommended transceivers meets all IEE-488 maximum timing requirements. If the WD9914 is used with other transceivers, then it must be ensured that these requirements are still met.

AUXILIARY COMMANDS

There are two basic types of commands implemented in the auxiliary command regiater: immediate execute and clear/set.

The clear/set commands are used to enable and disable the various features of the WD9914. The particular feature is selected by the code on f0-f4 and it is set or cleared according to the value on the cs bit. For the purposes of the state diagrams, the mnemonic of a clear/set command simply represents its current state.

The immediate execute auxiliary commands remain active for the duration of a strobe signal after the auxiliary command register has been written to. This is represented in the form of a state diagram in Figure 5. Note that writes to the auxiliary command register must be spaced by at least five clock cycles. For the purposes of the remaining state diagrams, the immediate execute commands are represented as the mnemonic gated by the auxiliary command strobe state (AXSS).

The clear/set bit of the auxiliary command register is used by several of the immediate execute commands, for example, 'dacr' uses it to differentiate between valid and not valid secondary addresses when releasing a DAC holdoff on a secondary address. The 'lon' and 'ton' auxiliary commands are also considered immediate execute.

The 'fget' and 'rtl' auxiliary commands are both immediate execute and clear/set. They may be cleared or set in the normal way, but if they are cleared when they are already in the false state, they will pulse true for the duration of AXSS. In the following state diagrams, however, these are simply included in their clear/set form.

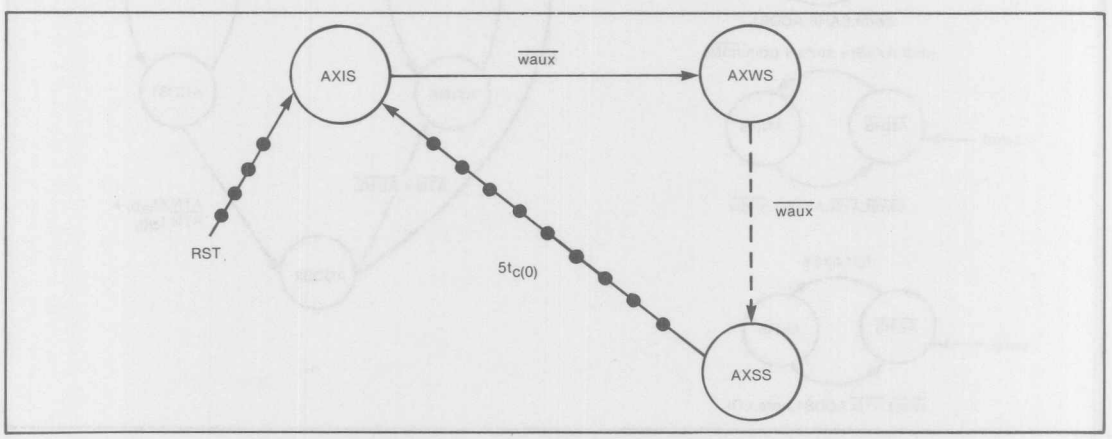


Figure 4. WD9914 AUXILIARY COMMAND STATE DIAGRAM

Table 5. AUXILIARY COMMAND STATE DIAGRAM MNEMONICS

MESSAGES			STATES		
waux	=	write to auxiliary command register	AXIS	=	auxiliary command register idle state
$t_{c(0)}$	=	clock cycle time	AXWS	=	auxiliary command write state
			AXSS	=	auxiliary command strobe state

ACCEPTOR HANDSHAKE

The WD9914 acceptor handshake is shown in Figure 5. The main variation from IEEE-488 to note is that the device remains in AIDS while the controller function is in CACS. The WD9914, therefore, does not monitor the commands which it sends over the bus and this places some restrictions on the user.

The accept data state of IEEE-488 (ACDS) is divided into two states. The first, (ACDS1) is used to strobe data into the Data In Register or to sequence the decoding of commands from the bus. All interrupts generated by the acceptor handshake (GET, MA, MAC, DCAS, APT, UCG, BI, and END) are generated by this state. The second (ACDS2) is used as a holding state where the device will remain in the event of a DAC holdoff.

Certain of the commands will cause interrupts in ACDS1 and, if the interrupts are unmasked, a DAC holdoff will occur. The interrupts concerned are GET, MA, DCAS, UCG, and APT. This is represented in the state diagram by the signal SAHF which becomes true when one of the above interrupts is set if it is unmasked. It persists for the duration of ACDS1. This event is stored by causing the ADHS to become active which inhibits the transition from ACDS2 to AWNS. ADHS is cleared by 'dacr.' Table 19 shows the response of the WD9914 to the various bus commands.

If a GET command is received in ACDS1, then the TR pin will be set high. This high condition persists throughout ACDS1 and ACDS2, which means that if a DAC holdoff occurs, the TR pin will remain high until the holdoff is released by a 'dacr' auxiliary command.

Two additional state diagrams are included to record

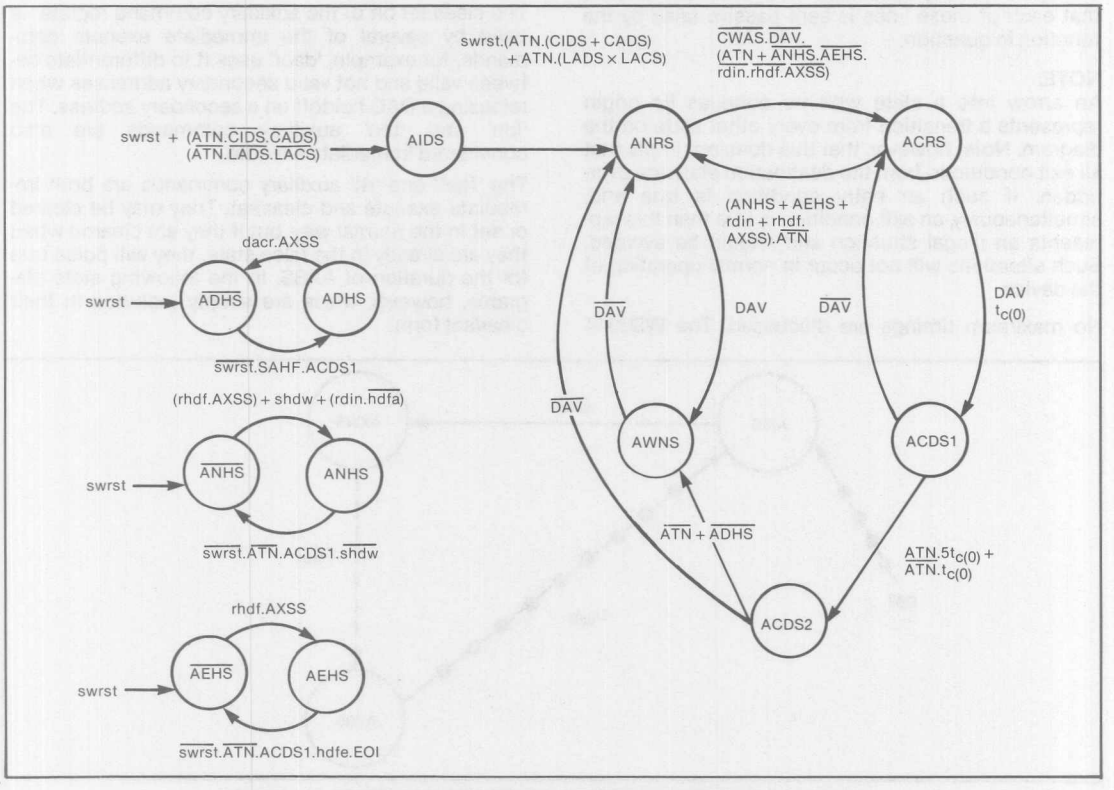


Figure 5. WD9914 ACCEPTOR HANDSHAKE STATE DIAGRAM

the type of data received in ACDS1 when ATN is false. ANHS indicates that a data byte has been received and that an RFD holdoff should be caused before the next data byte is accepted. The holdoff may be released by reading the Data In Register unless the 'hdfa' feature is enabled in which case 'rhdf' must be used. AEHS shows that the last data byte was accepted with the EOI message true and the 'hdfe' feature set. This will cause an RFD holdoff which can only be released by 'rhdf.'

Table 6. ACCEPTOR HANDSHAKE MNEMONICS

MESSAGES			STATES		
swrst	=	software reset	AIDS	=	acceptor idle state
dacr	=	DAC release	ANRS	=	acceptor not ready state
rhdf	=	release RFD holdoff	ACRS	=	acceptor ready state
shdw	=	shadow handshake	ACDS1	=	accept data state 1
rdin	=	read data in register	ACDS2	=	accept data state 2
hdfe	=	enable RFD holdoff after END messages received	AWNS	=	acceptor wait for new cycle state
hdfa	=	enable RFD holdoff on all data	ADHS	=	accept data holdoff state
ATN	=	attention	ANHS	=	acceptor not ready holdoff state
DAV	=	data valid	AEHS	=	acceptor not ready holdoff after 'END'
EOI	=	end or identify state	CWAS	=	controller wait for ANRS state (controller function)
RFD	=	ready for data	AXSS	=	auxiliary command strobe state (auxiliary command register)
DAC	=	data accepted	LADS	=	listener addressed state (listener function)
SAHF	=	set accept data holdoff state	LACS	=	listener active state (listener function)
$t_{c(0)}$	=	clock cycle time	CIDS	=	controller idle state (controller function)
			CADS	=	controller addressed state (controller function)

Table 7. ACCEPTOR HANDSHAKE MESSAGE OUTPUTS

STATE	REMOTE MESSAGES SENT		OTHER ACTIONS	
	RFD	DAC		
AIDS	(T)	(T)		
ANRS	F	F		
ACRS	(T)	F		
ACDS1	F	F	ATN False:	— data entered into Data In Register — BI interrupt generated — end interrupt generated if EOI is true.
			ATN true:	— commands decoded — command related interrupts set — sahf set if command requires a DAC holdoff — TR pin set true if GET message is received — 'pts' feature cleared after UNC interrupt set
ACDS2	F	F	TR	— pin set true if GET command was received in ACDS1
AWNS	F	(T)		

SOURCE HANDSHAKE

The WD9914 source handshake state diagram is shown in Figure 6. IEEE-488 states SIWS and SWNS have been removed. These record the false then true transition of 'nba' (new byte available) as the old data byte is removed and a new data byte is made ready. Instead the WD9914 uses a separate state (SHFS) to record the availability of a data byte in the Data Out Register. This state is exited when a byte is written to the Data Out Register which enables the transition from SGNS to SDYS and the subsequent transmission of the byte. The SHFS is reentered as the byte is sent in STRS, but if the handshake is interrupted before this, then the fact that the byte has not been sent is recorded until the source handshake again becomes active. If, however, the byte in the data out register is to be disregarded, then 'nbaf' may be used to return the device to SHFS.

The status byte in the Serial Poll Register is continually available. The transition from SGNS to SDYS is not dependent on SHFS during a serial poll, that is, while SPAS is active. By separately recording the availability of a byte in the Data Out Register, a talker sending data may be interrupted for a serial poll without risk of a byte being lost.

The additional state SERS is included to detect an error condition on the bus. This will be entered when the source handshake tries to send a byte but finds both the NRFD and NDAC lines false at the same time. This condition will normally indicate for a controller that there are no devices powered up on the bus, or for a talker that there are no devices addressed to listen on the bus.

The state VSTS will be entered after the first data byte of a talker has been sent if the 'vstdl' feature is enabled. This enables a very short bus settling time ($4t_{c(0)}$) for all subsequent bytes until ATN next becomes true. The WD9914 will not use the short bus settling time when it is an active controller.

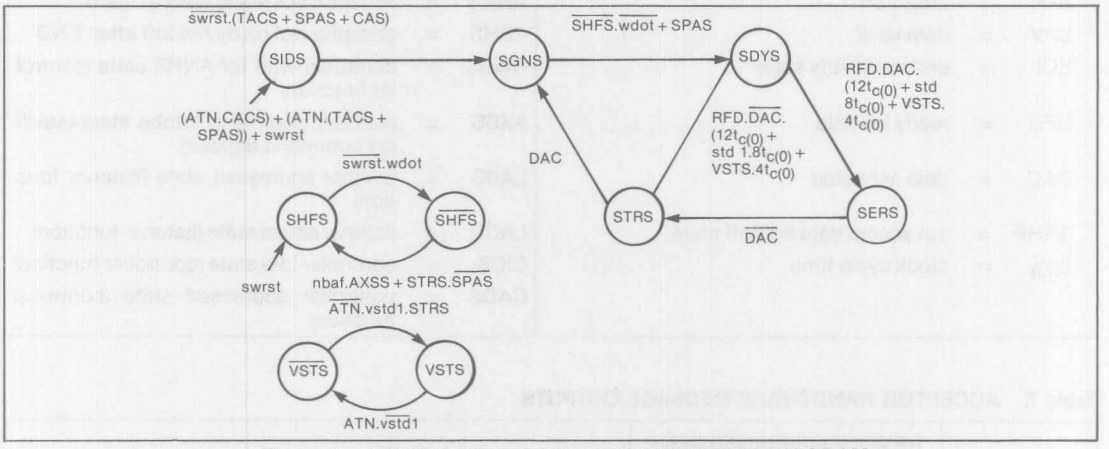


Figure 6. WD9914 SOURCE HANDSHAKE STATE DIAGRAM

Table 8. SOURCE HANDSHAKE MNEMONICS

MESSAGES			STATES		
swrst	=	software reset	SIDS	=	source idle state
nbaf	=	new byte available false	SGNS	=	source generate state
wdot	=	write to the data out register	SDYS	=	source delay state
stdl	=	enable short bus settling time	SERS	=	source error state
vstdl	=	enable very short bus settling time	STRS	=	source transfer state
ATN	=	attention	SHFS	=	source holdoff state
RFD	=	ready for data	VSTS	=	very short bus settling time state
DAC	=	data accepted	TACS	=	talker active state (talker function)
$t_{c(0)}$	=	clock cycle time	CACS	=	controller active state (controller function)
			SPAS	=	serial poll active state (talker function)
			AXSS	=	auxiliary command strobe state (auxiliary command register)

Table 9. SOURCE HANDSHAKE MESSAGE OUTPUTS

STATE	REMOTE MESSAGES SENT DAV	OTHER ACTIONS
SIDS	(F)	BO interrupt and ACCRQ set true if SHFS is false and SPAS is not true
SGNS	F	
SDYS	F	
SERS	F	ERR interrupt set true
STRS	T	

TALKER AND LISTENER FUNCTIONS

Figures 7 and 8 show the WD9914 listener and talker state diagrams, which serve the purpose of the listener and talker or extended listener and extended talker functions of IEEE-488, depending on the state of the APT interrupt mask bit.

The WD9914 does not recognize secondary addresses on-chip and these must be passed through to the host MPU for verification. Secondary addressing is enabled by unmasking the APT interrupt. A secondary address will cause this interrupt if the last primary command received was a primary address of the device, that is, it is in TPAS or LPAS. A DAC holdoff will also occur. The host MPU must respond to the interrupt by reading the secondary from the Command Pass Through Register and identifying it as being valid or not valid. The holdoff may then be released with a 'dacr' auxiliary command, the sense of the 'cs' bit being used to indicate a valid (cs = 1) or not valid (cs = 0) secondary. If a valid secondary address is indicated then the WD9914 will enter TADS or LADS depending on whether it is in TPAS or LPAS.

The 'lon' and 'ton' auxiliary commands together with the clear/set bit (cs) have a direct influence on the appropriate state diagrams. Therefore, although they appear as ordinary clear/set auxiliary commands, they can be effectively cleared by other bus events. For example, if a WD9914 addresses itself as a listener via the 'lon' command it may be returned to LIDS by an UNL command from the bus at a later time.

The 'lon' and 'ton' auxiliary commands are used to implement two features of IEEE-488. First, talk only and listen only are used in situations where there is no active controller on the bus. Note that the 'lon' and 'ton' commands are linked with these features to indicate to the user that these commands are not enabled by CAS as are 'ltn' and 'lun' of IEEE-488.

Second, the 'lon' and 'ton' auxiliary commands are used by an active controller to address itself. IEEE-488 provides for a controller to address itself to listen via the 'ltn' and 'lun' message but there is no corresponding message for the talker. Hence, when a controller addresses itself to talk via 'ton,' it must send its talk address over the bus and similarly, if it sends another talk address over the bus then it must unaddress itself by writing 'ton' false.

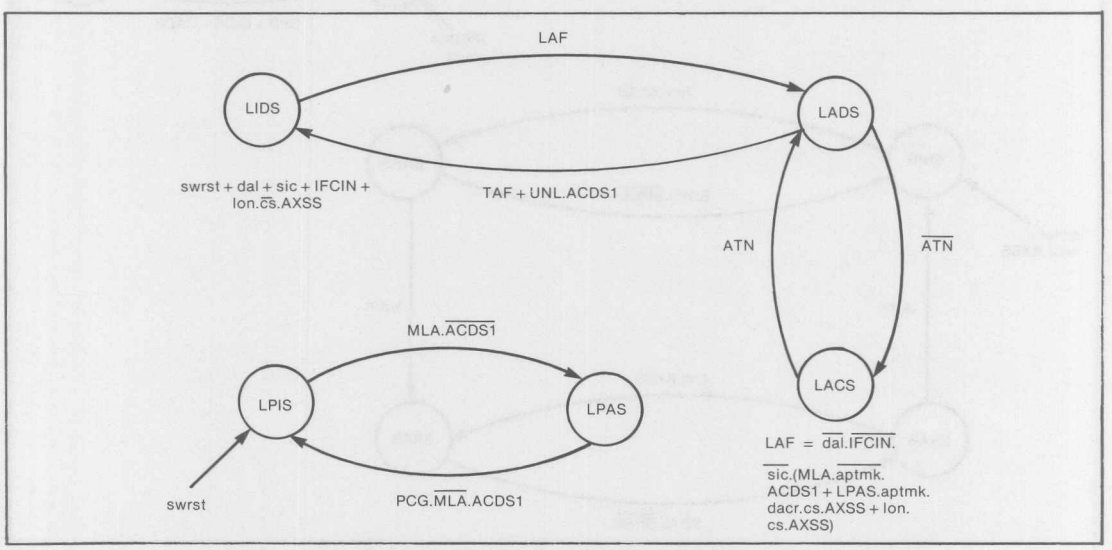


Figure 7. WD9914 LISTENER STATE DIAGRAM

When the WD9914 enters SPAS, the contents of the serial poll register are sampled and presented on DIO(8-1). These will remain unchanged until SPAS is exited. The source handshake will, however, send this status byte as many times as the controller will accept it.

The internal IFC signal of the WD9914 (IFCIN) is suppressed when the device itself is sending IFC in order to simplify implementation of the controller function. Therefore, the send interface clear (sic) auxiliary command is included with IFCIN to return the talker and listener functions to their idle states and allow a system controller to clear its own interface.

A separate state diagram is included to control the sending of the END message of IEEE-488. If the 'feoi' auxiliary command is written followed by loading a byte into the Data Out Register, the WD9914 will enter ERAS, and the EOI line will be asserted as 'DIO(8-1)' begin to change. The function will enter ENAS as soon as the source handshake begins to send this byte, and EOI will be released when the Data Out Register is next loaded. If it is desired to send EOI true with the next byte as well, then 'feoi' may be written before the Data Out Register returns the device to ERAS.

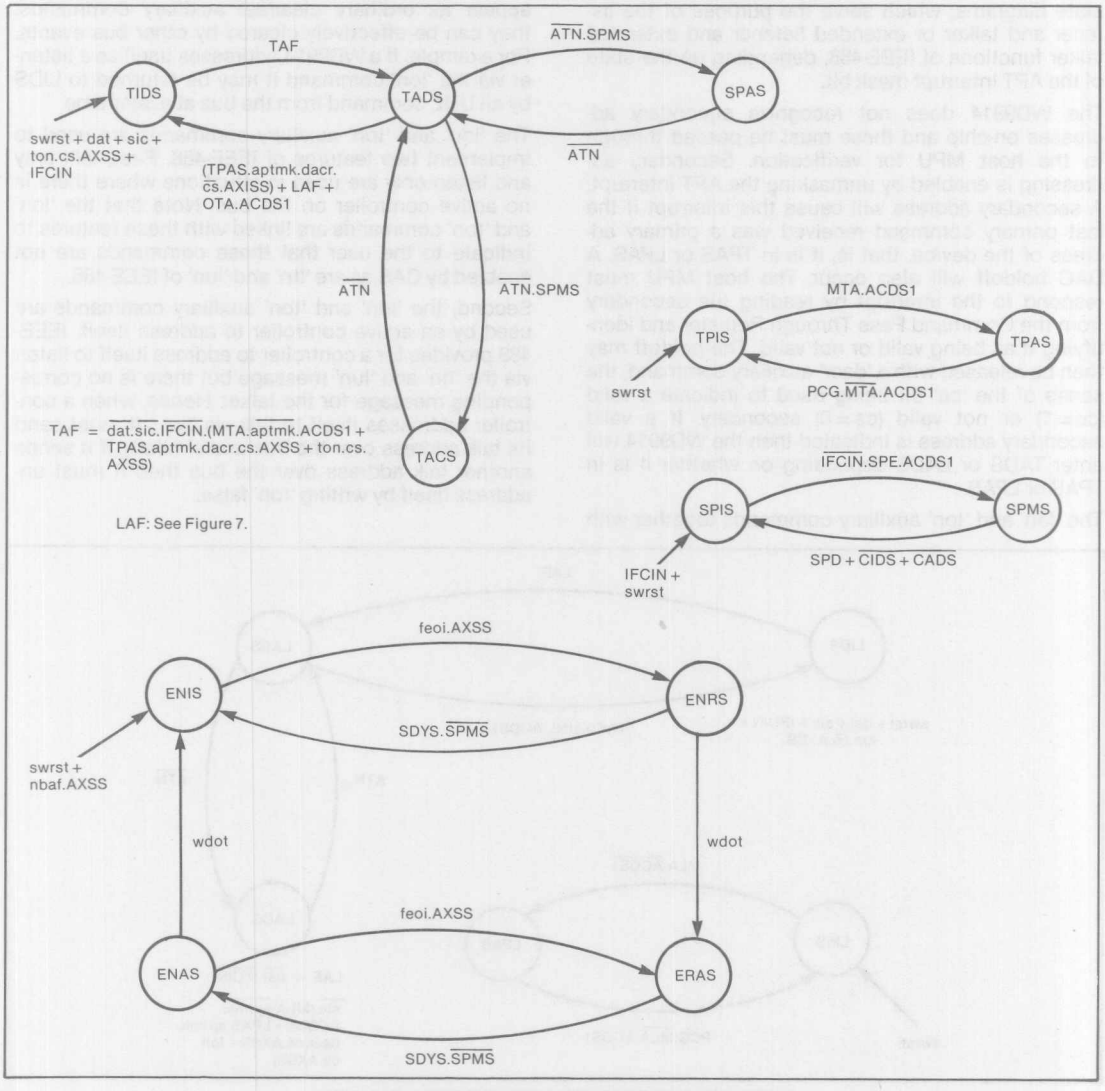


Figure 8. WD9914 TALKER STATE DIAGRAM

Table 10. TALKER AND LISTENER MNEMONICS

MESSAGES			STATES		
swrst	=	software reset	LIDS	=	listener idle state
dal	=	disable listener	LADS	=	listener addressed state
dat	=	disable talker	LACS	=	listener active state
sic	=	send interface clear	LPIS	=	listener primary idle state
lon	=	listen only	LPAS	=	listener primary addressed state
ton	=	talk only	TIDS	=	talker idle state
cs	=	clear/set bit of the auxiliary command register	TADS	=	talker addressed state
dacr	=	release 'DAC' holdoff	TACS	=	talker active state
aptmk	=	address pass through interrupt mask	SPAS	=	serial poll active state
nbaf	=	new byte available false	SPIS	=	serial poll idle state
feoi	=	force 'EOI'	SPMS	=	serial poll mode state
wdot	=	write to the Data Out Register	TPIS	=	talker primary idle state
ATN	=	attention	TPAS	=	talker primary addressed state
IFCIN	=	internal interface clear message (a debounced signal, suppressed by 'sic')	ENIS	=	end idle state
EOI	=	end or identify	ENRS	=	end ready state
PCG	=	primary command group	ERAS	=	end ready and active state
MLA	=	my listen address	ENAS	=	end active state
MTA	=	my talk address	SDYS	=	source delay state (source handshake)
OTA	=	other talk address	CIDS	=	controller idle state (controller function)
SPE	=	serial poll enable	CADS	=	controller addressed state (controller function)
SPD	=	serial poll disable	ACDS1	=	accept data state 1 (acceptor handshake)
UNL	=	unlisten	AXSS	=	auxiliary command strobe state (auxiliary command register)
PCG	=	primary command group			

Table 11. TALKER FUNCTION MESSAGE OUTPUTS

STATE	QUALIFIER	REMOTE MESSAGES SENT		OTHER ACTIONS DIO(8-1)
		RQS	EOI	
TIDS		(F)	(F)	(NUL)
TADS		(F)	(F)	(NUL)
TACS	ENIS.ENRS	(F)	F	DATA OUT REG
TACS	ENAS.ERAS	(F)	T	DATA OUT REG
SPAS	NPRS.SRQS	F	F	SERIAL POLL REG
SPAS	APRS1.APRS2	T	F	SERIAL POLL REG

SERVICE REQUEST FUNCTION

Figure 9 shows the state diagram for the WD9914 service request function. The device has two means of implementing the request service (rsv) local message of IEEE-488: the first, 'rsv1,' is bit 7 of the Serial Poll Register; the second is the auxiliary command 'rsv2.' These are simply ORed together to provide an input to the service request function, and, in any particular application, only one would normally be used, the other being left in its hardware reset state.

The affirmative poll response state (APRS) of IEEE-488 is split into two states on the WD9914 for the following reason: Consider the case where a device has requested service, has been serial polled, and then wishes to request service again. The host MPU must clear the 'rsv' message and then set it true again. Now suppose this temporary false condition happens within one occurrence of SPAS. If the service request function has been implemented exactly as per IEEE-488, it will not be recognized, and SRQ will not be asserted a second time. Therefore, 'rsv' may only be cleared when the device is known not to be in SPAS, which can only happen if it is cleared as a consequence of some pre-arranged action of the controller. This action would normally be a part of the service routine executed by the controller as a response to the request for service. For example, if service was requested by an instrument which had some data to send for processing or to a printing device then 'rsv' could be cleared when it is addressed to talk and send its data over the bus.

For many applications, the fact that the device has been serial polled after requesting service is considered sufficient response from the controller. The 'rsv' local message therefore simply becomes a request for the controller to read its serial poll status byte. It is then desirable to be able to clear and reassert 'rsv' at any time after the serial poll status byte has been polled and the SPAS interrupt set. The WD9914 is able to record a false transition of 'rsv1' or 'rsv2' by moving from APRS1 to APRS2 even if the device is in SPAS. This makes the above approach to serial polling possible.

To further support this approach, the 'rsv2' auxiliary command is automatically cleared when the serial poll status byte is polled, ensuring that 'rsv2' is cleared before a second serial poll can occur. If this were not the case, then the same status byte might be polled twice by the controller with the RQS bit true, which may indicate that two reasons for requiring service have arisen.

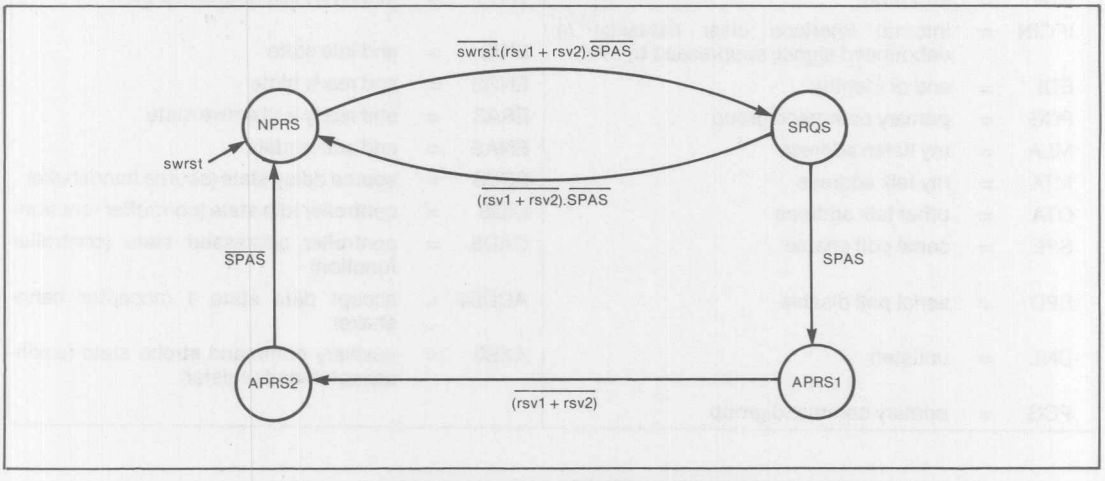


Figure 9. SERVICE REQUEST STATE DIAGRAM

The WD9914 will only send one serial poll status byte during each active period of SPAS. However, it will send this status byte as many times as the controller is prepared to accept it. Therefore, the controller should only read the status byte once per serial poll; otherwise, each time a status byte is sent with the RQS message true, the SPAS interrupt will be generated and 'rsv2' will be cleared.

Table 12. SERVICE REQUEST MNEMONICS

MESSAGES			STATES		
swrst	=	software reset	NPRS	=	negative poll response state
srv1	=	request service 1 (bit 7 of serial poll register)	SRQS	=	service request state
rsv2	=	request service 2 (auxiliary command register)	APRS1	=	affirmative poll state 1
			APRS2	=	affirmative poll state 2
			SPAS	=	serial poll active state (talker function)

Table 13. SERVICE REQUEST MESSAGE OUTPUTS

STATE	REMOTE MESSAGES SENT SRQ	OTHER ACTIONS
NPRS	(F)	
SRQS	T	
APRS1	(F)	— rsv2 cleared if in SPAS and STRS — SPAS interrupt set if in SPAS when STRS is exited
APRS2	(F)	— same as APRS1

REMOTE/LOCAL FUNCTION

The WD9914 remote local state diagram is shown in Figure 10. If differs little from that of IEEE-488.

The complete listener function (LAF) is used to effect the transition from LOCS to REMS or from LWLS to RWLS. This means that if the APT interrupt is masked, the device will enter one of the remote states in response to its listen address, but if secondary addressing is enabled, then this will not happen until 'dacr' is written with 'cs' true in response to a valid secondary address. In addition, the transition to one of the remote states will occur if 'lon' is used to address the device to listen.

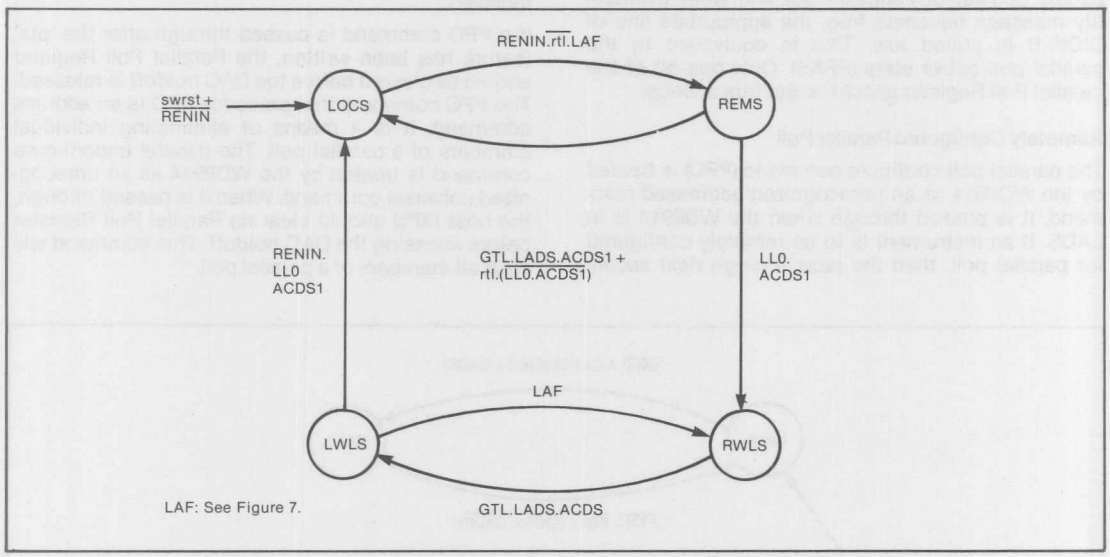


Figure 10. WD9914 REMOTE LOCAL STATE DIAGRAM

Table 14. REMOTE/LOCAL MNEMONICS

MESSAGES			STATES		
swrst	=	software reset	LOCS	=	local state
rtl	=	return to local	REMS	=	remote state
RENIN	=	internal remote enable message (debounced)	RWLS	=	remote with lockout state
GTL	=	go to local	LWLS	=	local with lockout state
LLO	=	local lockout	LADS	=	listener addressed state (listener function)
			ACDS1	=	accept data state 1 (acceptor handshake)

PARALLEL POLL FUNCTION

The parallel poll function of the WD9914 only nominally supports logically-configured parallel poll. With a suitable software package, remotely-configured parallel poll may also be easily implemented. The state diagram is shown in Figure 11.

When the EOI and ATN lines become true simultaneously (the Identify message), the contents of the Parallel Poll Register are output to DIO(8-1). If parallel poll is to be used in a particular bus environment, then the Pull-Up Enable (PE) input of the SN75160 must be held low so that the DIO(8-1) are driven by open collector buffers. Parallel Poll, occurring when the Parallel Poll Register is in the hardware reset condition of all zeros, will result in none of DIO(8-1) being pulled low. This corresponds to the parallel poll idle state (PPIS). If it is desired to participate in a parallel poll, then the bit corresponding to the desired parallel poll response is set true. This implements the parallel poll standby state (PPSS), and, when the Identify message becomes true, the appropriate line of DIO(8-1) is pulled low. This is equivalent to the parallel poll active state (PPAS). Only one bit of the parallel Poll Register should be set true at once.

Remotely Configured Parallel Poll

The parallel poll configure command (PPC) is treated by the WD9914 as an unrecognized addressed command. It is passed through when the WD9914 is in LADS. If an instrument is to be remotely configured for parallel poll, then the pass through next secondary (pts) auxiliary command should be written before releasing the DAC holdoff. This will cause the next command received to also set a UNC interrupt if it is a secondary command. The secondary command will be either the parallel poll enable command (PPE) or the parallel poll disable command (PPD) and should be read from the Command Pass Through Register and identified. If it is the PPE command, then the attendant bits (S, P1, P2, P3) should be extracted and stored by the host MPU. The S bit should then be matched against the individual status of the instrument (represented by 'ist'), and if they are the same, the bit corresponding to the parallel poll response, specified by P1, P2, P3, should be set true in the Parallel Poll Register. If this is not the case, then the Parallel Poll Register should be cleared if it is not already clear. After this, each time the individual status of the device changes, the 'ist' should again be matched against the S bit and the Parallel Poll Register updated accordingly until PPD or PPU is received.

If a PPD command is passed through after the 'pts' feature has been written, the Parallel Poll Register should be cleared before the DAC holdoff is released. The PPC command that precedes PPD is an address command; it is a means of eliminating individual members of a parallel poll. The parallel unconfigure command is treated by the WD9914 as an unrecognized universal command. When it is passed through, the host MPU should clear its Parallel Poll Register before releasing the DAC holdoff. This command will clear all members of a parallel poll.

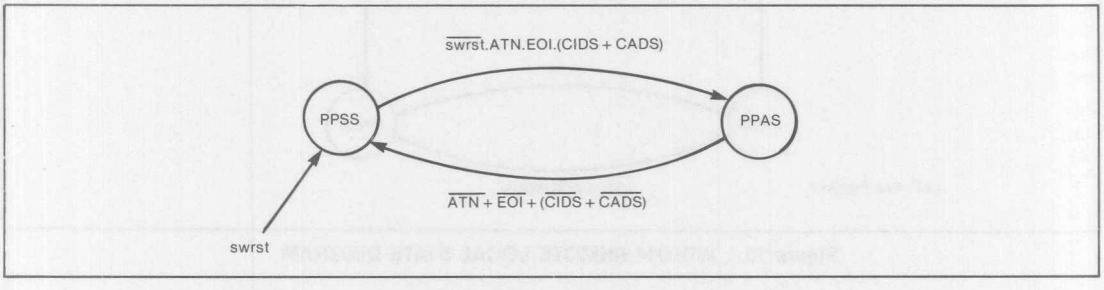


Figure 11. WD9914 PARALLEL POLL STATE DIAGRAM

Table 15. PARALLEL POLL MNEMONICS

MESSAGES			STATES		
swrst	=	software reset	PPSS	=	parallel poll standby state
ATN	=	attention	PPAS	=	parallel poll active state
EOI	=	end or identify	CIDS	=	controller idle state (controller function)
			CADS	=	controller addressed state (controller function)

Table 16. PARALLEL POLL MESSAGE OUTPUTS

STATE	REMOTE MESSAGES SENT DIO(8-1)	OTHER ACTIONS
PPSS	(NUL)	
PPSS	PARALLEL POLL REG*	

*If there is a true bit in the Parallel Poll Register, it must be sent active; any false bit must be sent passive.

CONTROLLER FUNCTION

The controller function of the WD9914 is greatly simplified compared with that of IEEE-488. It relies heavily on software support but, with suitable software, it enables all subsets of the controller function to be implemented. With this approach the controller logic is reduced to a small proportion of the chip area which means that the device may be economically used in situations where a talker/listener only is required.

Figure 12 shows the controller function state diagram. With suitable software, it will perform the full controller function, as described in the IEEE-488A 1980 supplement to the IEEE-488 1978. It therefore includes the additional state CSHS, which allows time for DAV to be recognized false by all devices on the bus before ATN is asserted. The 'tcs' local message is implemented by an immediate execute auxiliary command. The state CWAS is therefore added to record the occurrence of this command until the acceptor handshake enters ANRS and the device can enter CSHS. The 'tca' auxiliary command also causes entry into CSHS although IEEE-488A 1980 allows it to move directly from CSBS to CSWS. This is done for convenience of implementation and results in the 'tca' auxiliary command taking an extra 1.6 microseconds to assert ATN.

The delay between CSWS and CAWS is slightly less than specified in IEEE-488A 1980 but the total time taken in moving from CSWS to CACS is still greater than the specified minimum.

The Controller Parallel Poll State (CPPS) is not included on the WD9914. To conduct a parallel poll, a WD9914 based controller must set the 'rpp' clear/set auxiliary command true when it is in CACS, moving it to CPWS which sends EOI true. The host MPU must then wait 2 microseconds before reading back the parallel poll responses via the Command Pass Through Register. The 'rpp' auxiliary command can then be cleared, EOI will go false, and the parallel poll is complete. The host MPU will receive a BO interrupt as soon as the WD9914 reenters CACS and the source handshake becomes active.

Controller Self Addressing

The acceptor handshake does not operate when the controller is active. This means commands being sent are not monitored, and special precautions are required as a consequence of this when addressing devices and when passing control.

When the controller is active, it uses 'ton' or 'lon' to address and unaddress itself. IEEE-488 provides for the controller to locally address itself to listen, but there is no corresponding local message for the talker. The WD9914 should always accompany a 'ton' auxiliary command with 'cs' true with its own talk address or an UNT command sent over the bus. Similarly, if the WD9914 sends the talk address of another device over the bus, it should ensure that it is in TIDS by writing the 'ton' auxiliary command false.

Passing Control

As Figure 12 shows, the controller transfer state (CTRS) of IEEE-488 is not present, and all transitions associated with the TCT command have been removed. Instead, two immediate execute auxiliary commands are included. Request control (rqc) will cause a transition from CIDS to CADS, and the release control command (rlc) will return the function to CIDS. The TCT command is treated similarly to an unrecognized addressed command but will cause a UNC interrupt if the device is in TADS.

Figure 13 is a representation of the sequence of events involved in passing control from one WD9914 based device to another. The device passing control must initially ensure that it is not in TADS; then it should send out the talk address of the device to receive control. The receiving device will enter TADS, and after any DAC holdoff has been released, the host MPU of the device passing control will set a BO interrupt indicating that it may then send the TCT command. The TCT command will cause a UNC interrupt to the host MPU of the receiving device, and also a DAC holdoff will occur. The host MPU of the receiving device must examine its Command Pass Through Register, and upon identifying TCT, should write the auxiliary command 'rqc' to put its WD9914 into CADS. The receiving device may then release DAC with a 'dacr' auxiliary command causing another BO interrupt at the device passing control. This indicates that the 'ric' auxiliary command may then be used by the host MPU of the device passing control to return its WD9914 to CIDS and allowing ATN to go false. The receiving device then enters CACS, asserts ATN, and its host MPU gets a BO interrupt as the source handshake becomes active. The passing of control is complete.

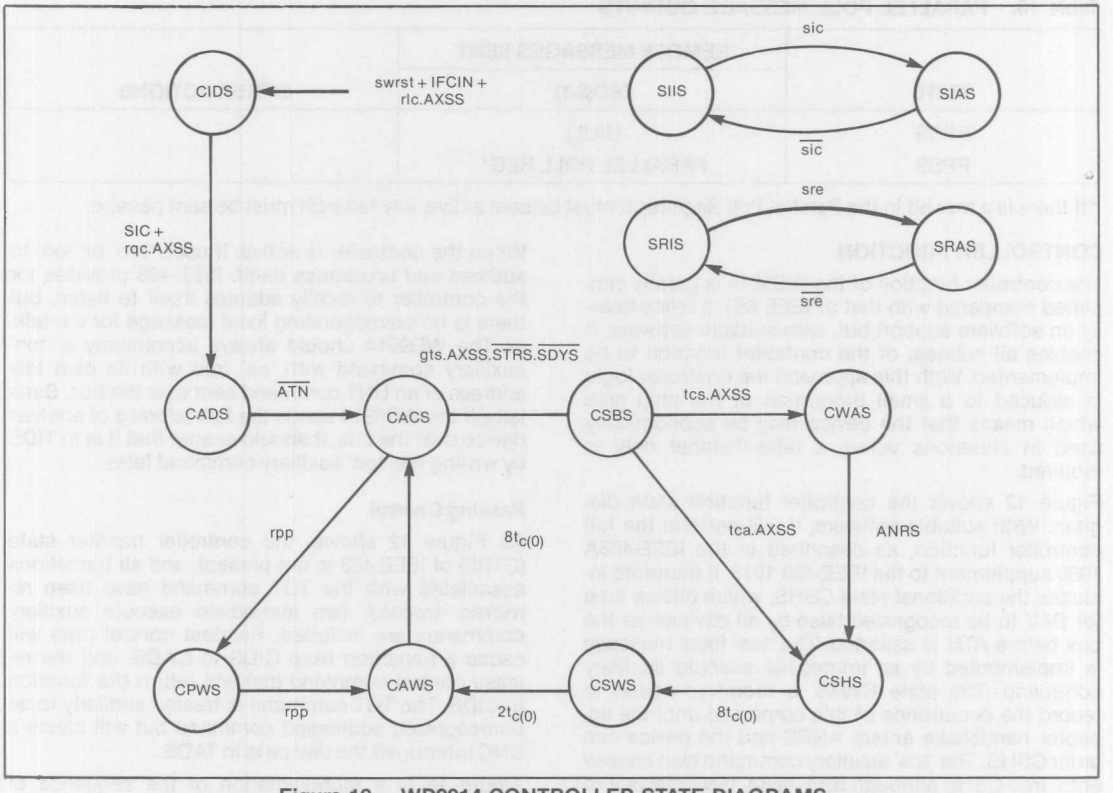


Figure 12. WD9914 CONTROLLER STATE DIAGRAMS

Table 17. CONTROLLER FUNCTION MNEMONICS

MESSAGES			STATES		
swrst	=	software reset	CIDS	=	controller idle state
sic	=	send interface clear	CADS	=	controller addressed state
sre	=	send remote enable	CACS	=	controller active state
rqc	=	request control	CSBS	=	controller standby state
rlc	=	release control	CSHS	=	controller standby hold state
gts	=	go to standby	CSWS	=	controller synchronous wait state
tcs	=	take control synchronously	CAWS	=	controller active wait state
tca	=	take control asynchronously	CPWS	=	controller parallel poll wait state
rpp	=	request parallel poll	ANRS	=	acceptor not ready state (acceptor handshake)
IFCIN	=	internal interface clear message (a debounced signal which is suppressed if 'sic' is true)	SDYS	=	source delay state (source handshake)
ATN	=	attention	STRS	=	source transfer state (source handshake)
$t_{c(0)}$	=	clock cycle time	AXSS	=	auxiliary command strobe state (auxiliary command register)
			LWAS	=	controller wait for ANRS state

Table 18. CONTROLLER FUNCTION MESSAGE OUTPUTS

STATE	REMOTE MESSAGE SENT			OTHER ACTIONS
	ATN	EOI	D10(8-1)	
CIDS	(F)	(F)	(NUL)	
CADS	(F)	(F)	(NUL)	
CACS	T	F	DATA OUT REG	Data Out Reg. may contain any of the commands in Table 19
CSBS	F	(F)	(NUL)	
CWAS	F	(F)	(NUL)	
CSHS	F	(F)	(NUL)	
CSWS	T	F	(NUL)	
CAWS	T	F	(NUL)	
CPWS	T	T	(NUL)	DIO(8-1) may be read via the Command Pass Through Register

STATE	REMOTE MESSAGES SENT	OTHER ACTIONS
	IFC	
SIIS*	(F)	Internal interface clear message IFCIN is held false
SIIS	F	
SIAS	T	

STATE	REMOTE MESSAGES SENT	OTHER ACTIONS
	REN	
SRIS*	(F)	
SRIS	F	
SRAS	T	

*Buffers not configured for a system controller; otherwise, buffers are configured for system controller.

The REN and IFC outputs of the WD9914 are controlled by the auxiliary commands 'sre' and 'sic.' These should never be used by the host MPU of a device unless it is the system controller. As may be seen from Figure 14, the REN and IFC outputs of the WD9914 are open drains with internal pull-ups. This means that the outputs are capable of driving the inputs of the buffers if the device is a system controller. If not, the buffers will drive into the REN and IFC pins and override the pull-ups. Hence, no direction control is required.

The false transition of REN and the true transition of IFC are both debounced to prevent noise on these lines from causing permanent state changes on the WD9914. In addition, the internal interface clear signal (IFCIN) is held false if the WD9914 is sending IFC. Figure 12 shows the reason for this. If the device is not a system controller, then the occurence of IFC will return the controller function to CIDS. If, however, the device is a system controller, when it asserts IFC and is in CIDS, the 'sic' auxiliary command will cause it to enter CADS. As IFCIN is suppressed, it will not be forced back into CIDS, and there will be no conflict.

System Controller

The WD9914 has no on-chip means of determining whether or not it is the system controller. Instead, this is determined by the software and by the configuration of the buffers to the IEEE-488 bus.

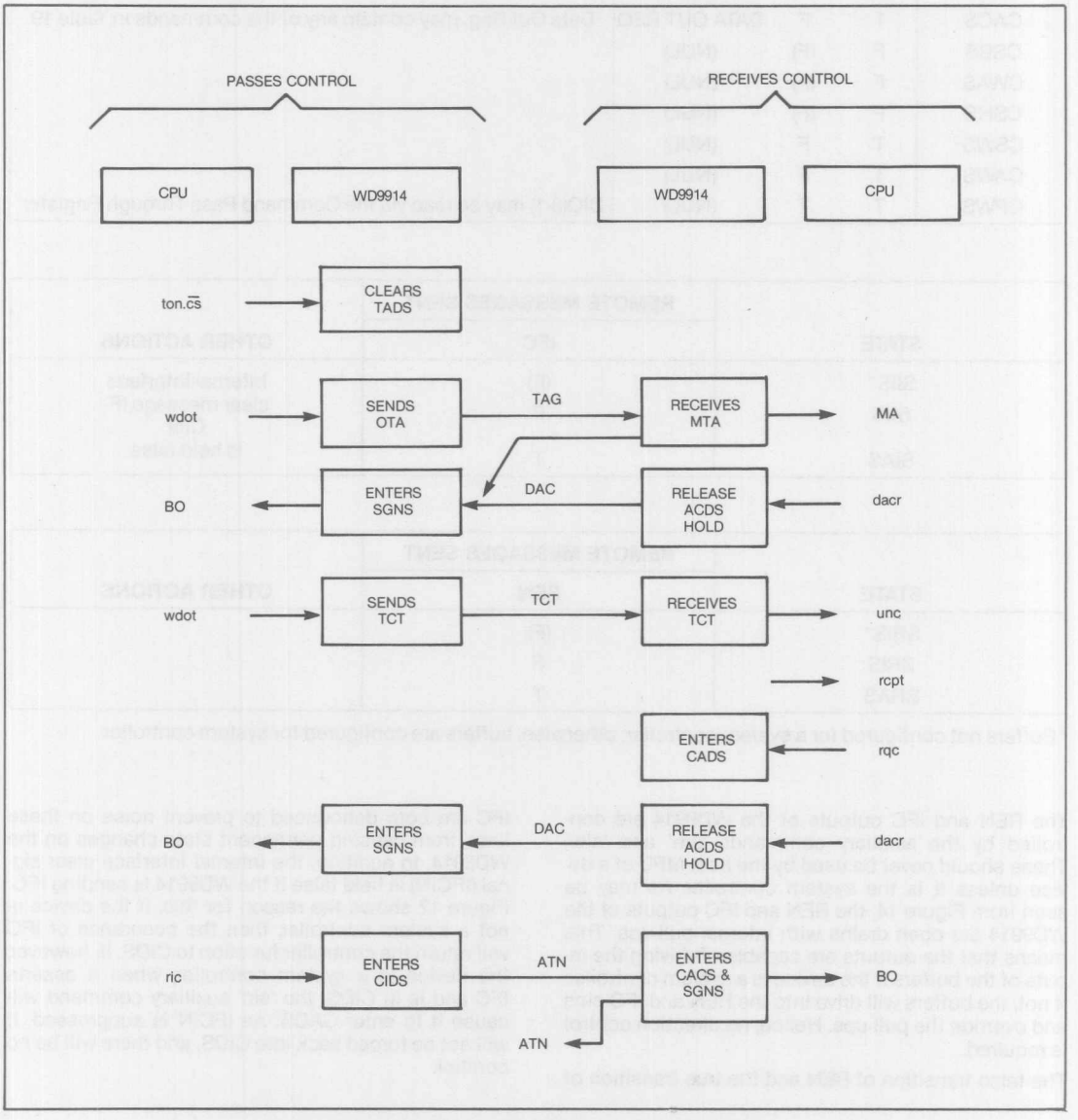
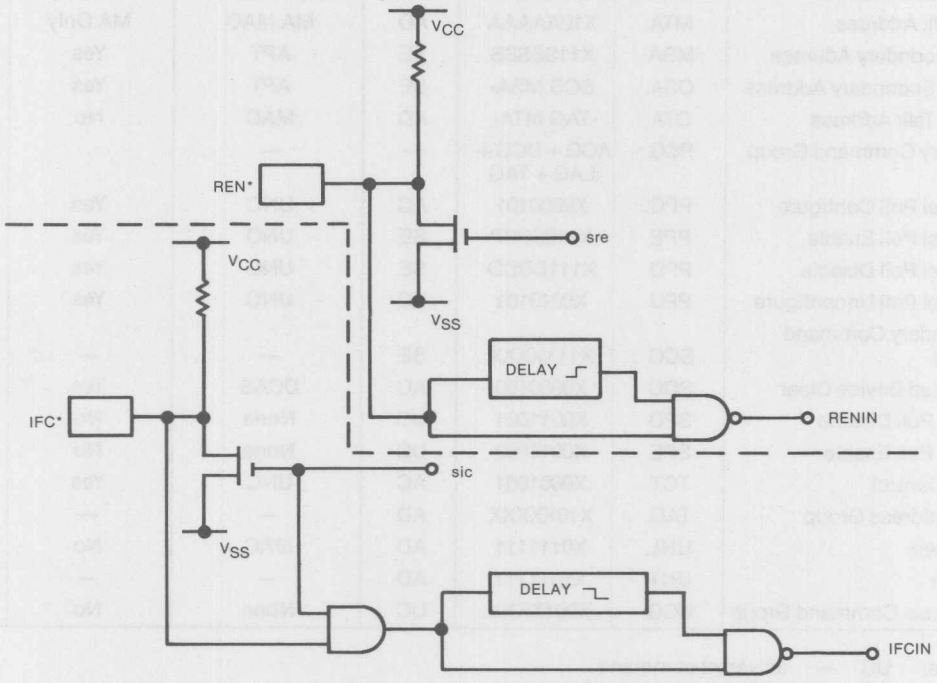


Figure 13. PASSING CONTROL BETWEEN WD9914



*The REN and IFC signals are at the pins of the WD9914 and are therefore negative logic signals. The remaining signals are conventional positive logic signals.

Figure 14. IFC AND REN PINS

Table 19. MULTILINE INTERFACE MESSAGES

COMMAND	SYMBOL	DIO 8-1	CLASS	INTERRUPT (1, 2)	DAC (3) HOLDOFF	NOTE
Addressed Command Group	ACG	000XXXX	AC	—	—	
Device Clear	DCL	X0010100	UC	DCAS	Yes	
Group Execute Trigger	GET	X0001000	AC	GET	Yes	
Go To Local	GTL	X0000001	AC	RLC	No	14
Listen Address Group	LAG	X01XXXXX	AD	—	—	
Local Lockout	LLO	X0010001	UC	None	No	
My Listen Address	MLA	X01AAAAA	AD	MA,MAC,RLC	MA Only	4,14
My Talk Address	MTA	X10AAAAA	AD	MA,MAC	MA Only	4
My Secondary Address	MSA	X11SSSSS	SE	APT	Yes	5,6
Other Secondary Address	OSA	SCG.MSA-	SE	APT	Yes	6,7
Other Talk Address	OTA	TAG.MTA-	AD	MAC	No	
Primary Command Group	PCG	ACG + UCG + LAG + TAG	—	—		
Parallel Poll Configure	PPC	X0000101	AC	UNC	Yes	8
Parallel Poll Enable	PPE	X110SPPP	SE	UNC	Yes	9,10
Parallel Poll Disable	PPD	X111DDDD	SE	UNC	Yes	9,11
Parallel Poll Unconfigure	PPU	X0010101	UC	UNC	Yes	12
Secondary Command Group	SCG	X11XXXXX	SE	—	—	
Selected Device Clear	SDC	X0000100	AC	DCAS	Yes	
Serial Poll Disable	SPD	X0011001	UC	None	No	
Serial Poll Enable	SPE	X0011000	UC	None	No	
Take Control	TCT	X0001001	AC	UNC	Yes	13
Talk Address Group	TAG	X10XXXXX	AD	—	—	
Unlisten	UNL	X0111111	AD	MAC	No	
Untalk	UNT	X1011111	AD	—	—	
Universal Command Group	UCG	X001XXXX	UC	None	No	

Classes: UC — universal command
AC — addressed command
AD — address
SE — secondary command

Symbols: 0 — logical zero (high level on GPIB)
1 — logical one (low level on GPIB)
x — don't care (received message)

NOTES:

1. Interrupts listed are as a direct consequence of the command received. They are set during ACDS1 and will cause the INT pin to be pulled low if unmasked.
2. The addressed commands will only cause their corresponding interrupt if the device is in LADS with the exception of TCT.
3. A DAC holdoff will only be caused if the corresponding interrupt is unmasked.
4. AAAAA represents the primary address of a device.
5. SSSSS represents the secondary address of a device.
6. Secondary addresses are handled via address pass through (APT interrupt). The host MPU should respond by writing the 'dacr' auxiliary command with 'cs' false.
7. If OSA is passed through via the APT interrupt,

the host MPU should respond by writing the 'dacr' auxiliary command with 'cs' false.

8. PPC is not recognized by the WD9914 and is therefore treated as an unrecognized addressed command.
9. PPE and PPD are secondary commands. These may be passed through to the host MPU using the 'pts' auxiliary command. When the PPC command is received the 'pts' auxiliary command should be written. PPE or PPD will then cause an APT interrupt.
10. SPPP specifies the sense bit, and the desired parallel poll response is a remotely configured parallel poll.
11. DDDD specifies don't care bits which must be sent as zeros but need not be decoded by the host MPU of the receiving devices.
12. PPU is not recognized by the WD9914 and will cause a UNC interrupt.
13. TCT is not recognized directly by the WD9914. It will cause a UNC interrupt when the device is in TADS.
14. RLC is set if MLA or GTL causes an appropriate transition in the Remote/Local function.

TYPICAL SEQUENCES OF EVENTS FOR THE CONTROLLER

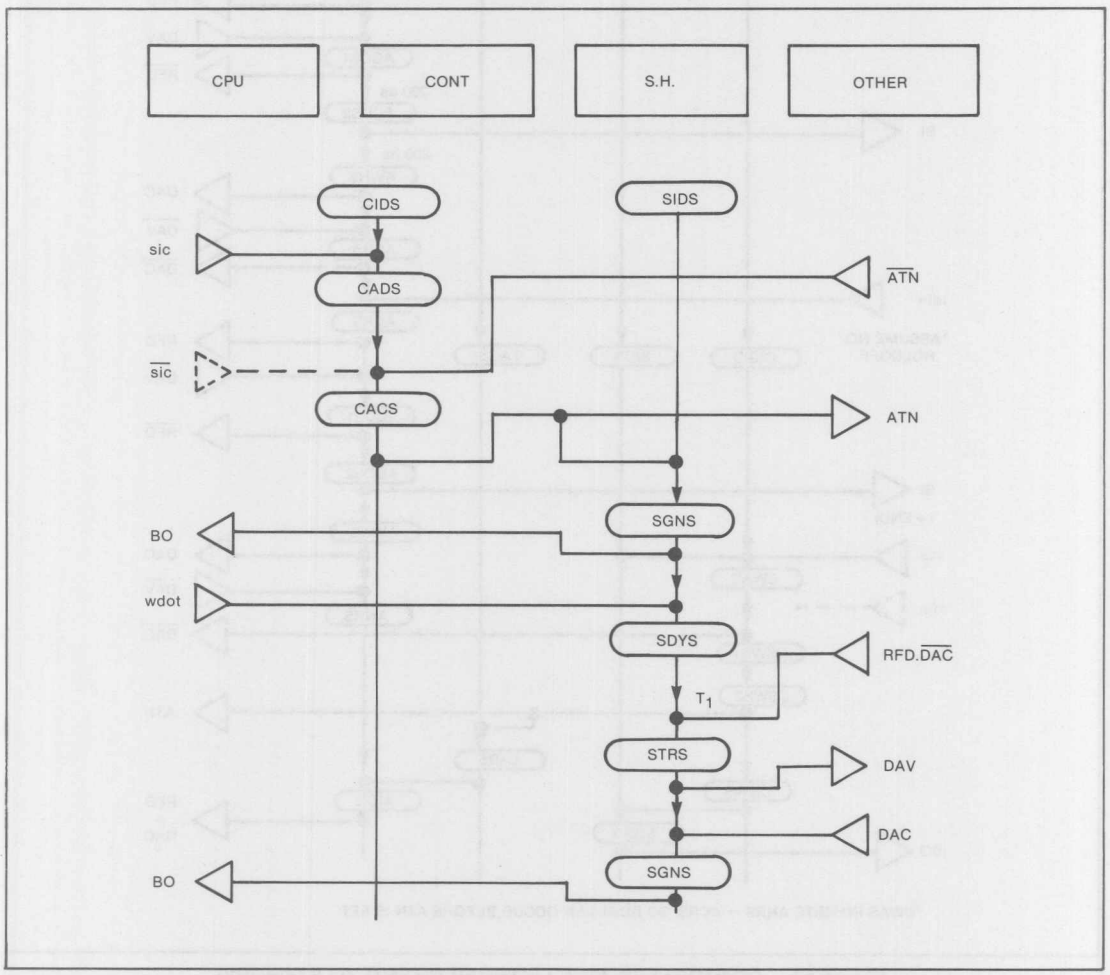


Figure 15. CONTROLLER TAKING CONTROL

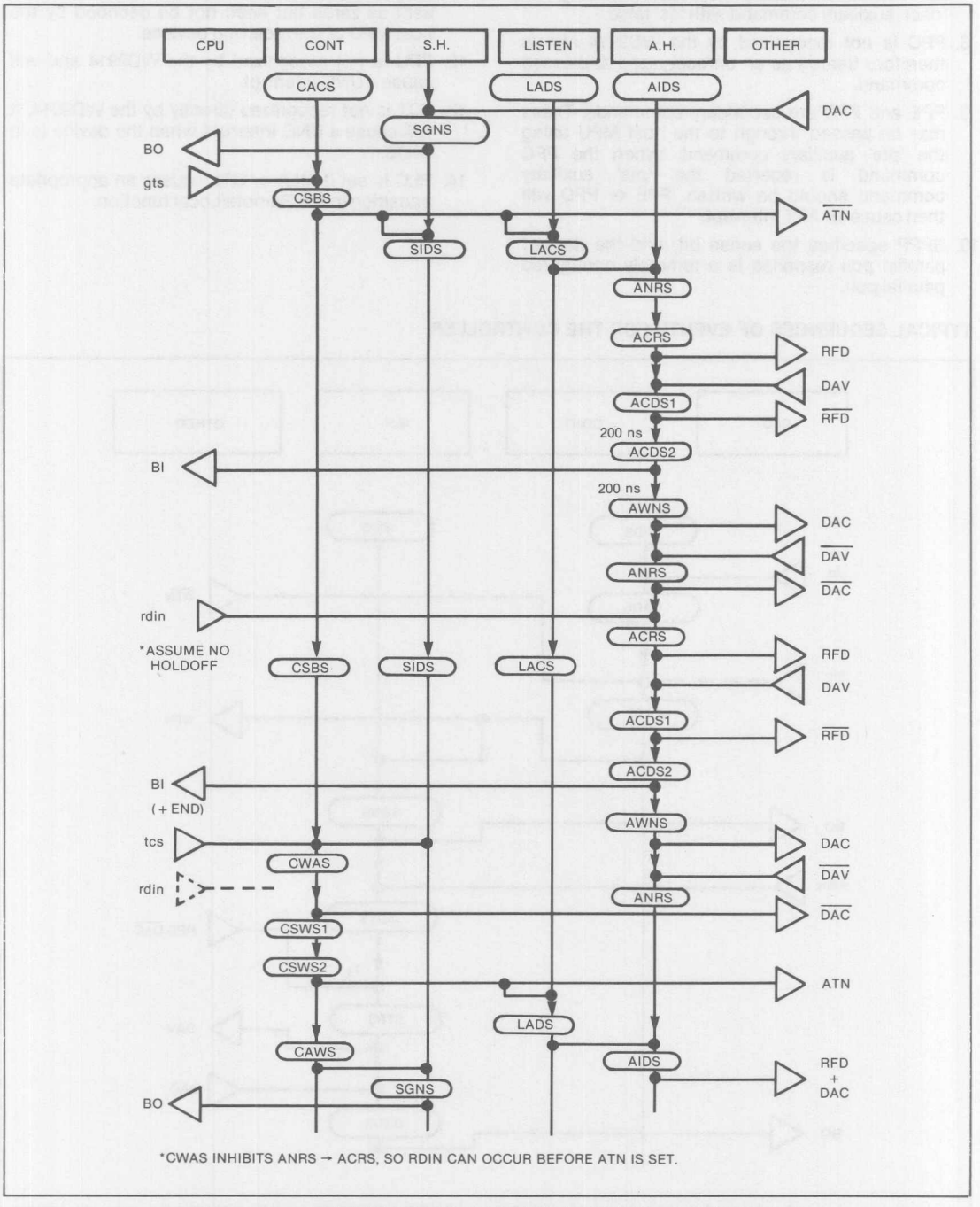


Figure 16. CONTROLLER AS A LISTENER (GOING TO STANDBY)

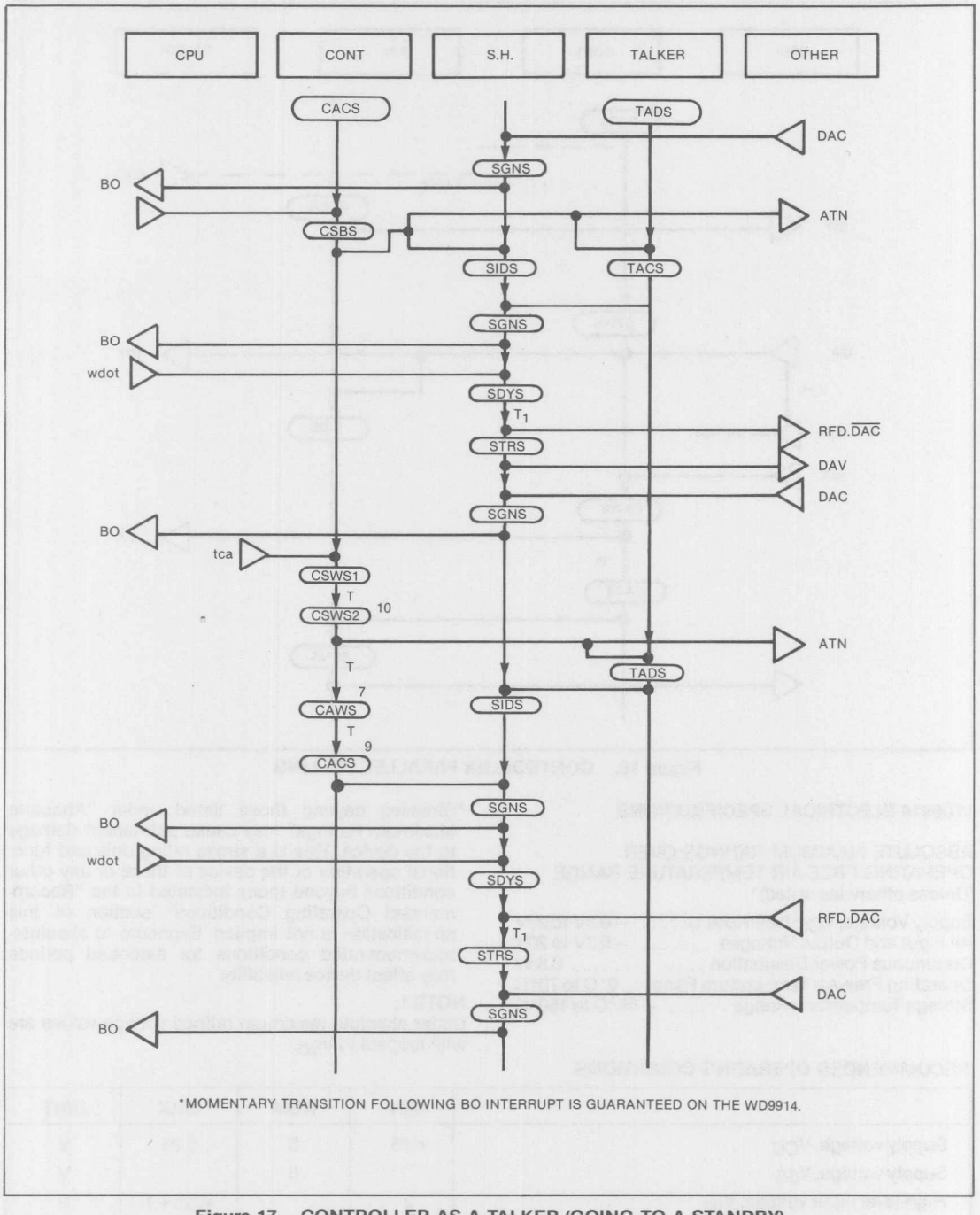


Figure 17. CONTROLLER AS A TALKER (GOING TO A STANDBY)

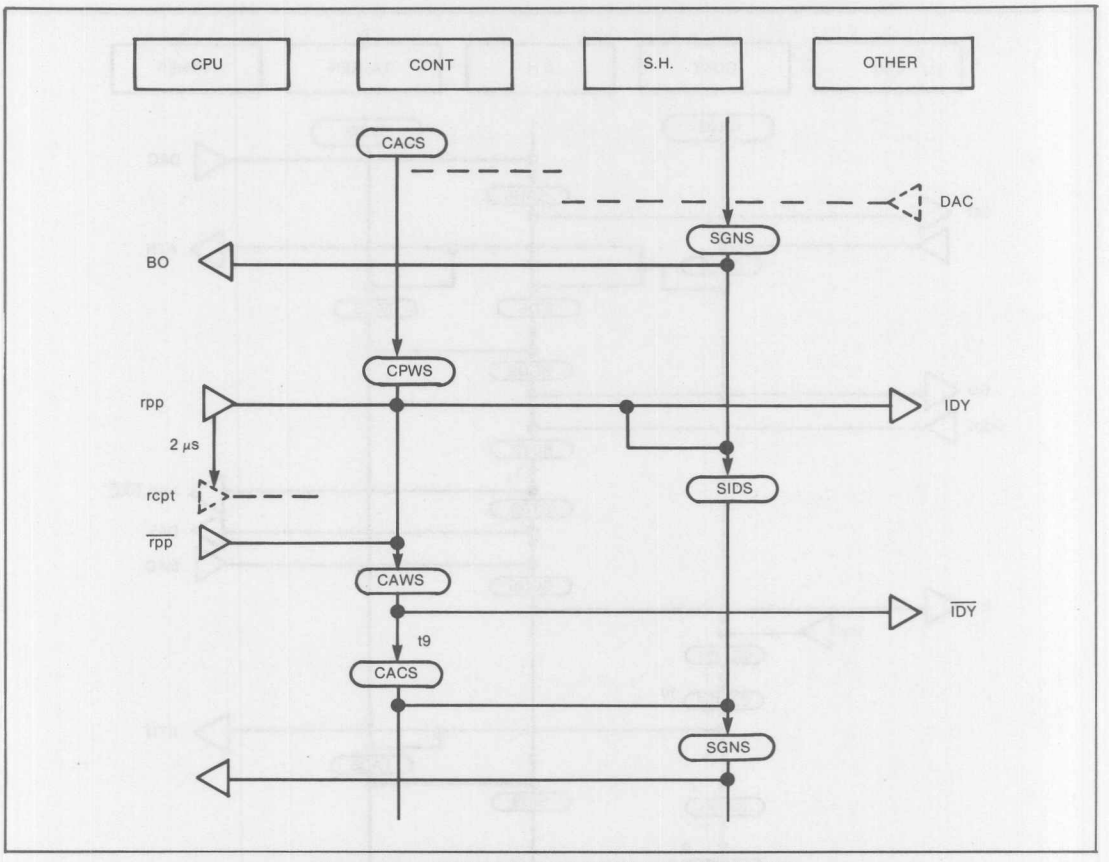


Figure 18. CONTROLLER PARALLEL POLLING

WD9914 ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS OVER OPERATING FREE-AIR TEMPERATURE RANGE (Unless otherwise noted)*

Supply Voltage, V_{CC} (see Note 1) .... −0.3V to 20V
All Input and Output Voltages ..... −0.3V to 20V
Continuous Power Dissipation ..... 0.8 W
Operating Free-Air Temperature Range . 0°C to 70°C
Storage Temperature Range ..... −55°C to 150°C

*Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1:
Under absolute maximum ratings voltage values are with respect to V_{SS}.

RECOMMENDED OPERATING CONDITIONS

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.75	5	5.25	V
Supply voltage, V_{SS}		0		V
High-level input voltage, V_{IH}	2		$V_{CC}+1$	V
Low-level input voltage, V_{IL}	V_{SS}-0.3		0.8	V
Operating free-air temperature, T_A	0		70	°C

ELECTRICAL CHARACTERISTICS OVER FULL RANGE OF RECOMMENDED OPERATING CONDITIONS

	PARAMETER	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage Except REN,IFC,INT	$I_{OH} = -400\,\mu A$	2.4		V_{CC}	V
	$\overline{REN}$,IFC only	$I_{OH} = -100\,\mu A$	2.2		V_{CC}	V
V_{OL}	Low-level output voltage	$I_{OL} = 2$ mA	V_{SS}		0.4	V
I_I	Input current (any input)	$V_I = 2$ V to V_{CC}			± 10	μA
I_{CC}	V_{CC} supply current				150	mA
C_i	Input capacitance (any input)	f = 1 MHz, unmeasured pins at 0 V			15	pF

† All typical values are at $T_A = 25°C$ and nominal voltage.

TIMING CHARACTERISTICS AND REQUIREMENTS

Timing characteristics and requirements are given in the following and relevant timing diagrams are shown in Figure 10 through Figure 27.

Clock and Host Interface Timing Requirements Over Full Range of Operating Conditions

	PARAMETER	MIN	TYP	MAX	UNIT
$t_{c(0)}$	Clock cycle time	200		2000	ns
$t_{w(0H)}$	Clock high pulse width	100		1955	ns
$t_{w(0L)}$	Clock low pulse width	45			ns
$t_{su(AD)}$	Address setup time	0			ns
$t_{su(DBIN)}$	DBIN setup time	0			ns
$t_{su(CE)}$	$\overline{CE}$ setup time	100			ns
$t_{su(WE)}$	$\overline{WE}$ setup time	0			ns
$t_{w(WE)}$	$\overline{WE}$ low pulse width	80			ns
$t_{su(DA)}$	Data setup time	60			ns
$t_{h(DA)}$	Data hold time	0			ns
$t_{h(AD)}$	Address hold time	0			ns
$t_{h(DBIN)}$	DBIN hold time	0			ns
$t_{h(CE)}$	$\overline{CE}$ hold time	80			ns
$t_{su(GR)}$	$\overline{ACCGR}$ setup time	100			ns
$t_{h(GR)}$	$\overline{ACCGR}$ hold time	80			ns

Host Interface Timing Characteristics Over Full Range of Operating Conditions

	PARAMETER	MIN	TYP	MAX	UNIT
$t_{a(CE)}$	Access time from $\overline{CE}$			150	ns
$t_{a(DBIN)}$	Access time from DBIN			150	ns
$t_{su(AD)}$	Address setup time to $\overline{CE}$	0			ns
$t_{z(DBIN)}$	Hi-Z time from DBIN		50	100	ns
$t_{z(CE)}$	Hi-Z time from $\overline{CE}$		50	100	ns
$t_{a(GR)}$	Access time from $\overline{ACCGR}$			150	ns
$t_{z(GR)}$	Hi-Z time from $\overline{ACCGR}$		50	100	ns
$t_{d(GR/RQ)}$	Delay of $\overline{ACCRQ}$ high from $\overline{ACCGR}$			100	ns

Source Handshake Timing Characteristics Over Full Range of Operating Conditions (see Note 1)

	PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
t_{d1}	Delay of DAV true from end of write operation to data out register	Normal T_1 (see Note 2)	12(0)↑	12(0)↑ + 310	ns
		Short T_1 (see Note 2)	8(0)↑	8(0)↑ + 310	ns
		Very short T_1 (see Note 2)	4(0)↑	4(0)↑ + 310	ns
t_{d2}	Delay of valid GPIB data lines from end of write cycle			140	ns
t_{d3}	Delay of BO interrupt from DAC true	BO interrupt unmasked		300	ns
t_{d4}	Delay of $\overline{\text{ACCRQ}}$ DAC true			300	ns
t_{d5}	Delay of DAV false from DAC true			160	ns

NOTES:

1. The timing of the source handshake is the same whether ATN is true or false, i.e., whether the device is in TACS, CACS, or SPAS.
2. A very short bus settling time (T_1) occurs on the second and subsequent data byte sent when ATN is false if the 'vstd1' feature is set. A slightly longer bus settling time takes place if 'std1' is set unless there is a very short bus settling time. In all other instances, a normal bus settling time occurs.

Acceptor Handshake Timing Characteristics Over Full Range of Operating Conditions

	PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
t_{d6}	Delay of BI interrupt from DAV true	BI interrupt unmarked ATN = false device is in LACS	2(0)↑	2(0)↑ + 415	ns
t_{d7}	Delay of $\overline{\text{ACCRQ}}$ from DAV true	ATN = false device is in LACS	2(0)↑	2(0)↑ + 290	ns
t_{d8}	Delay of DNAC false from DAV true	ATN = false device is in LACS	3(0)↑	3(0)↑ + 445	ns
t_{d9}	Delay of NRFD false from end of read operation of Data In register	ATN = false device is in LACS		220	ns
t_{d10}	Delay of interface message interrupt from DAV true	ATN = true device not in CACS all interface message interrupts (except UNO)	2(0)↑	2(0)↑ + 415	ns
		$\overline{\text{UNO}}$ interrupt only	5(0)↑	5(0)↑ + 415	ns
t_{d11}	Delay of NDAC false from DAV true	ATN = true device not in CACS no DAC holdoff	7(0)↑	7(0)↑ + 415	ns
t_{d12}	Delay of NDAC false from end of write operation			230	ns
t_{d13}	Delay of NRFD false from DAV false	ATN = true device not in CACS		180	ns

ATN, EOI, and IFC Timing Characteristics Over Full Range of Operating Conditions

	PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
t_{d14}	Delay of NDAC true from ATN true	Device is not in CACS		195	ns
t_{d15}	Delay of TE high from EOI true	Device is not in CACS		125	ns
t_{d16}	Delay of valid data from EOI true	Device is not in CACS		140	ns
t_{d17}	Delay of TE low from EOI false	Device is not in CACS		125	ns
t_{d18}	Delay of NRFD true from ATN false	Device is in LADS/LACS		140	ns
t_{d19}	Response time to IFC		$16t_{c(0)}$	$30t_{c(0)}$	ns

Controller Timing Characteristics Over Full Range of Operating Conditions

	PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
t_{d20}	Delay of ATN true from end of t_{ca} aux command		$8t_{c(0)}$	$10(0)\uparrow + 220$	ns
t_{d21}	Delay of BO interrupt from end of t_{ca} aux command		$18t_{c(0)}$	$22(0)\uparrow + 415$	ns
t_{d22}	Delay of ATN true from end of t_{cs} aux command	BO unmasked device is in ANRS	$8t_{c(0)}$	$10(0)\uparrow + 220$	ns
t_{d23}	Delay of BO interrupt from end of t_{cs} aux command	BO unmasked device is in ANRS	$18t_{c(0)}$	$22(0)\uparrow + 415$	ns
t_{d24}	Delay of EOI true from r_{pp} aux command set			230	ns
t_{d25}	Delay of EOI false from r_{pp} aux command cleared			230	ns
t_{d26}	Delay of EOI from r_{pp} aux command cleared	BO unmasked	$8t_{c(0)}$	$10(0)\uparrow + 415$	ns
t_{d27}	Delay of ATN false from sts aux command	Device is not in SDYS or STRS		210	ns

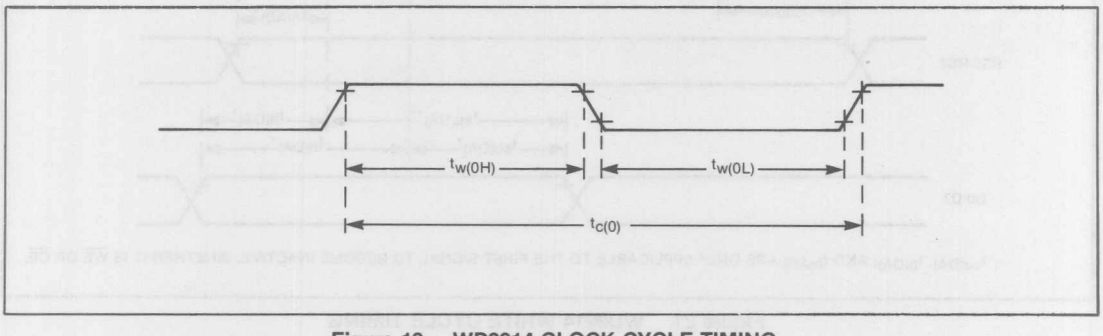


Figure 19. WD9914 CLOCK CYCLE TIMING

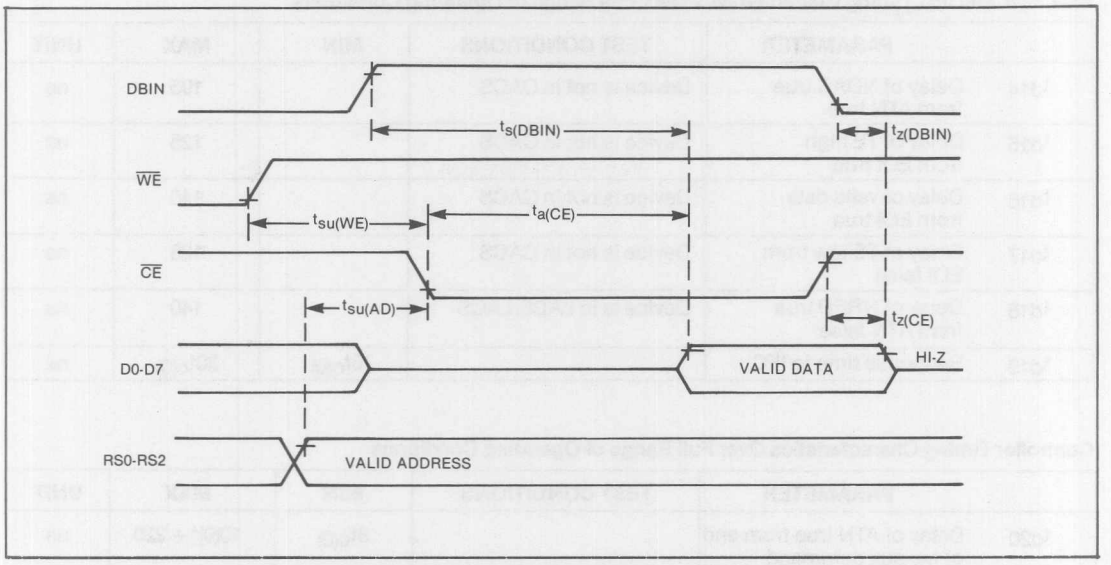


Figure 20. WD9914 READ CYCLE TIMING

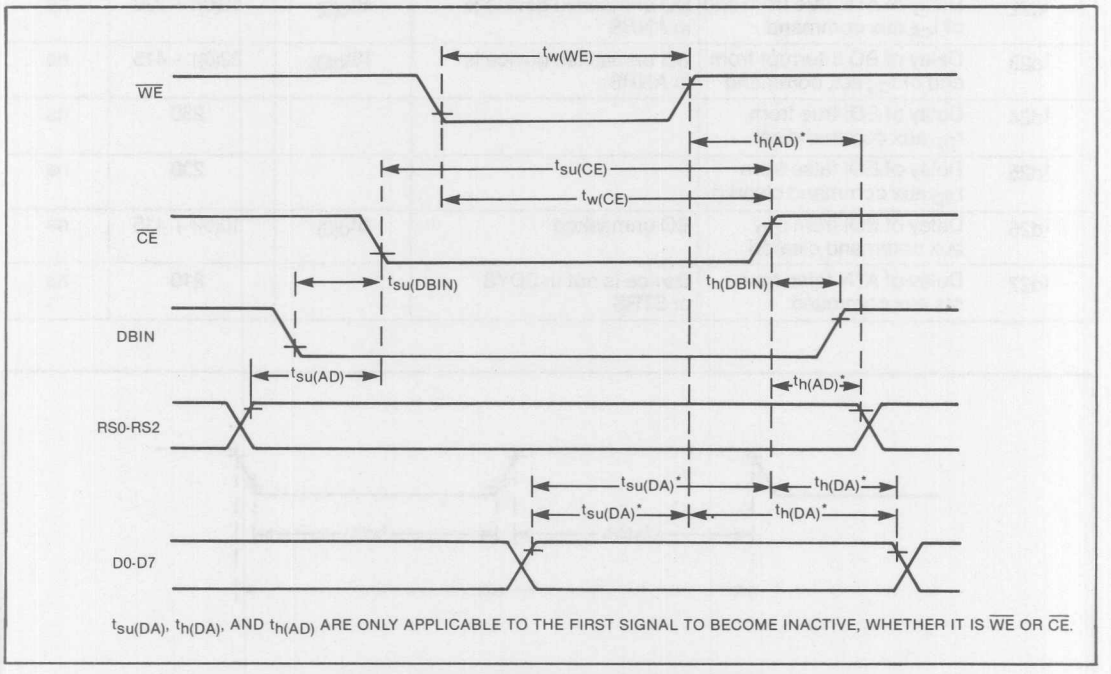
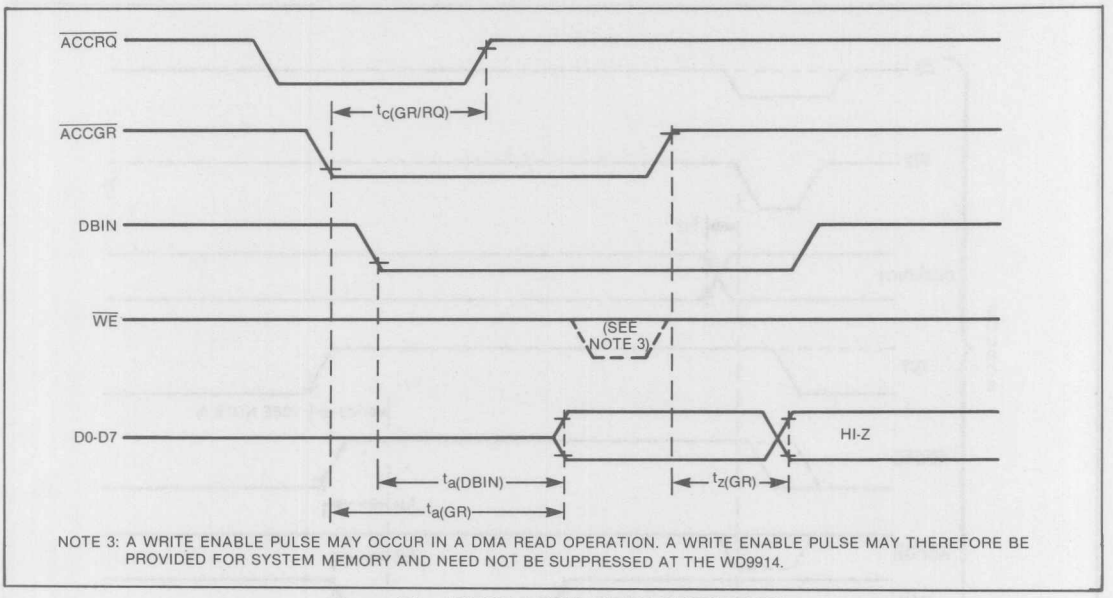
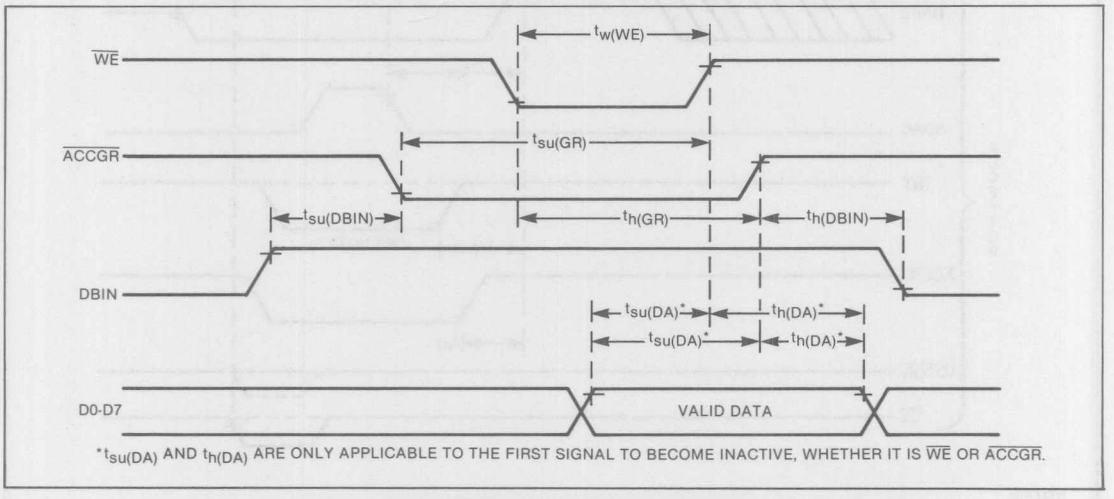


Figure 21. WD9914 WRITE CYCLE TIMING



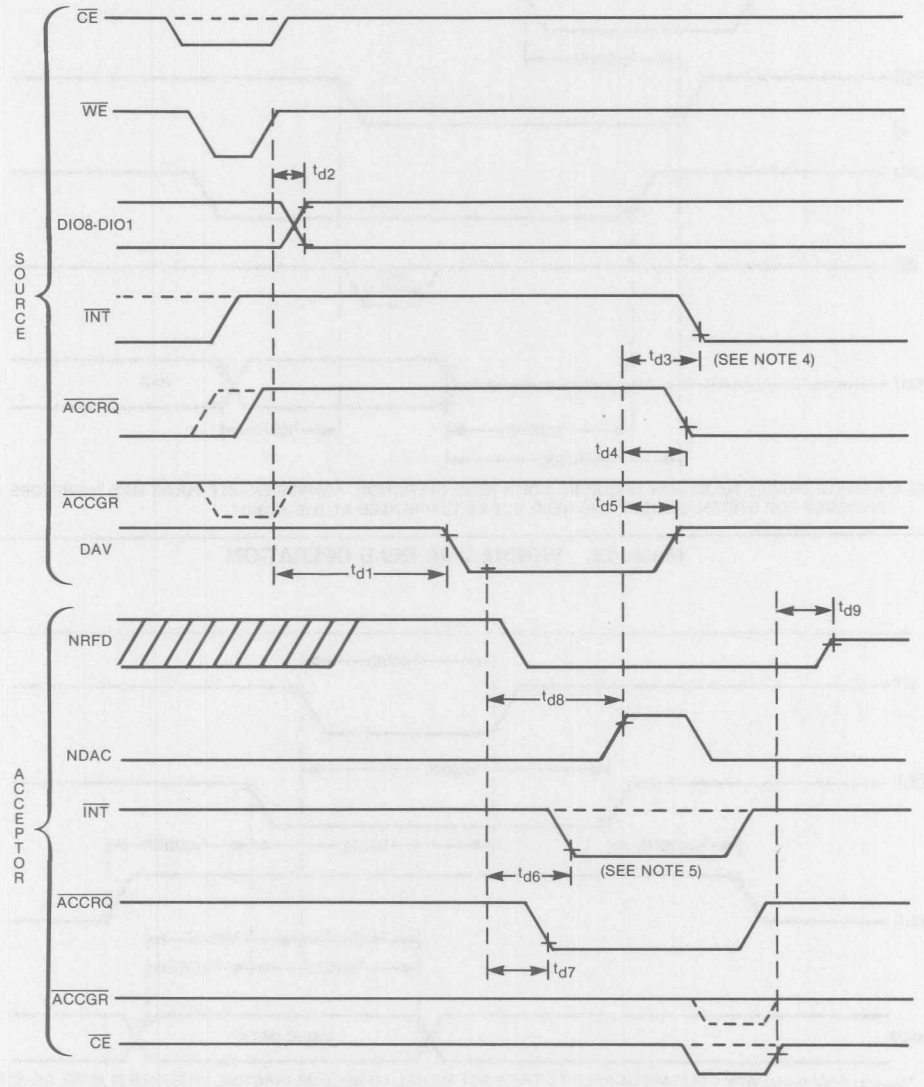
NOTE 3: A WRITE ENABLE PULSE MAY OCCUR IN A DMA READ OPERATION. A WRITE ENABLE PULSE MAY THEREFORE BE PROVIDED FOR SYSTEM MEMORY AND NEED NOT BE SUPPRESSED AT THE WD9914.

Figure 22. WD9914 DMA READ OPERATION



*$t_{su(DA)}$ AND $t_{h(DA)}$ ARE ONLY APPLICABLE TO THE FIRST SIGNAL TO BECOME INACTIVE, WHETHER IT IS $\overline{WE}$ OR $\overline{ACCGR}$.

Figure 23. WD9914 DMA WRITE OPERATION

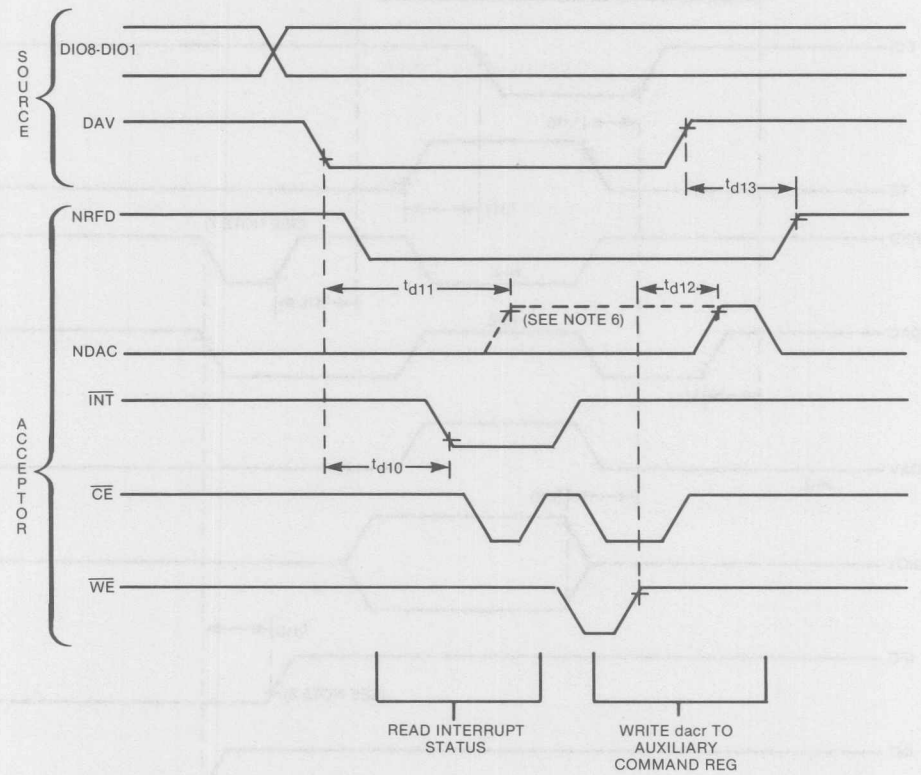


NOTES:

4: THE INTERRUPT LINE IS TAKEN LOW BY A BO INTERRUPT.

5: THE INTERRUPT LINE IS TAKEN LOW BY A BI INTERRUPT.

Figure 24. WD9914 SOURCE AND ACCEPTOR HANDSHAKE TIMING(S)



NOTES:

6: THE BROKEN LINE SHOWS THE WAVEFORM IF THERE IS NO DAC HOLDOFF. THE SOLID LINES ASSUME THERE IS A DAC HOLDOFF.

Figure 25. WD9914 ACCEPTOR HANDSHAKE TIMING "ATN" TRUE

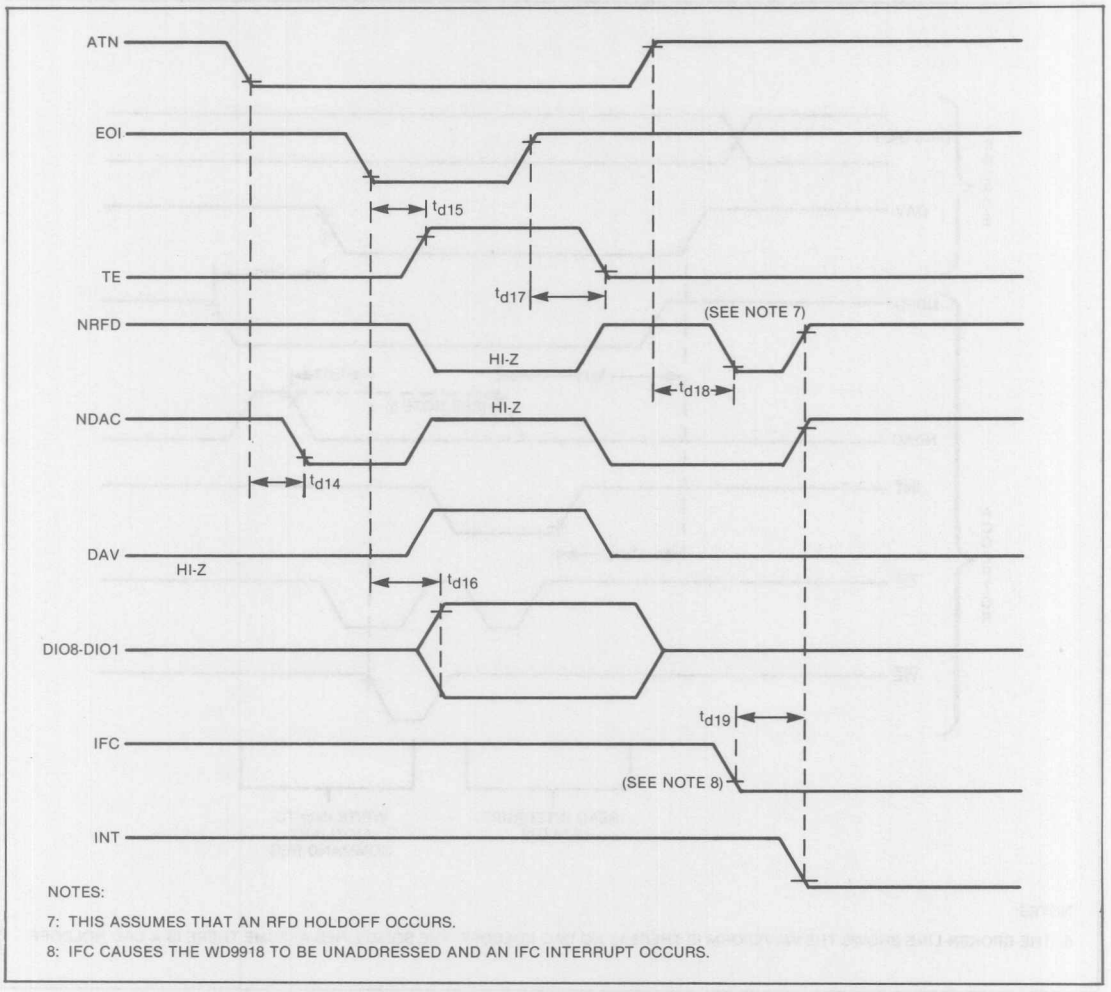
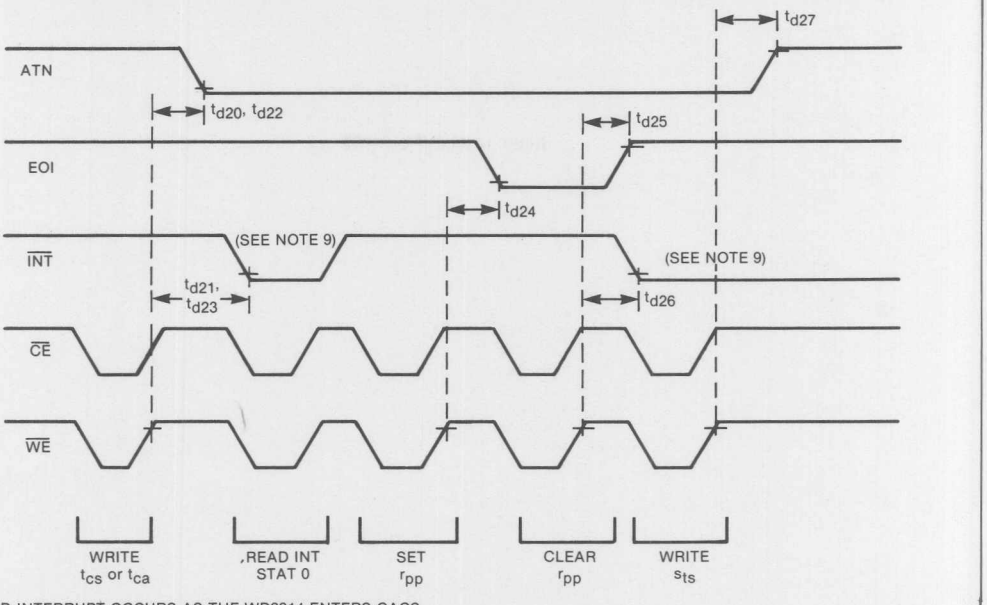


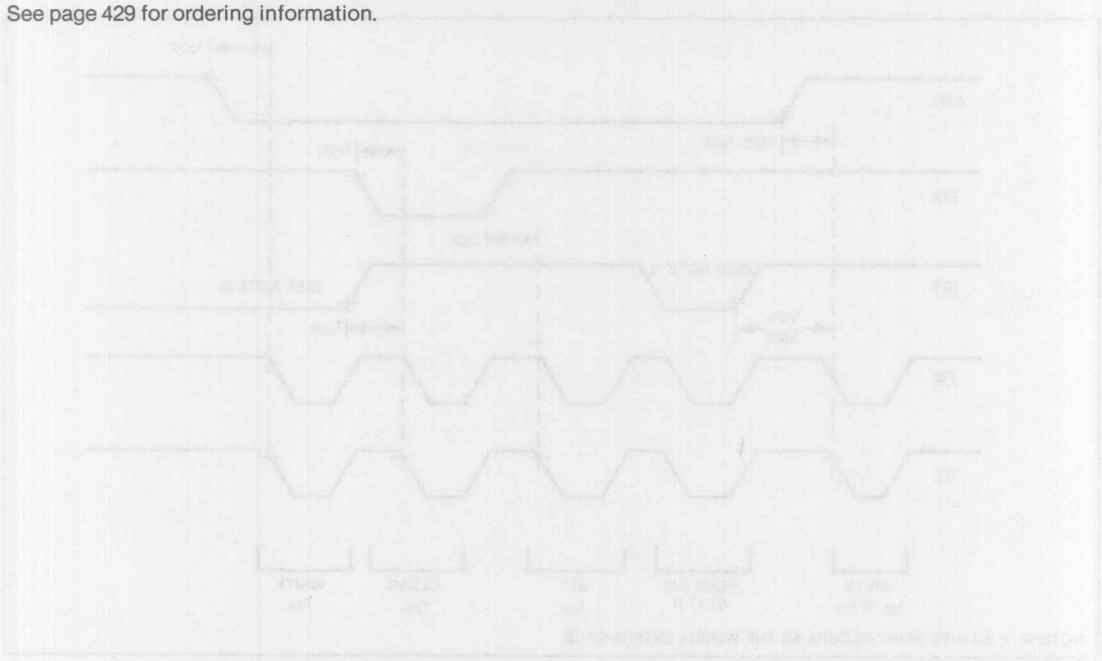
Figure 26. WD9914 RESPONSE TO 'ATN' AND 'EOI'



NOTE: 9: A BD INTERRUPT OCCURS AS THE WD9914 ENTERS CACS.

Figure 27. WD9914 CONTROLLER TIMING

See page 429 for ordering information.



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Printed in U.S.A.

WD1943(8116)/WD1945(8136) Dual Baud Rate Clock

FEATURES

- 16 SELECTABLE BAUD RATE CLOCK FREQUENCIES
- OPERATES WITH CRYSTAL OSCILLATOR OR EXTERNALLY GENERATED FREQUENCY INPUT
- ROM MASKABLE FOR NON-STANDARD FREQUENCY SELECTIONS
- INTERFACES EASILY WITH MICROCOMPUTERS
- OUTPUTS A 50% DUTY CYCLE CLOCK WITH 0.01% ACCURACY
- 6 DIFFERENT FREQUENCY/DIVISOR PAIRS AVAILABLE
- SINGLE +5V POWER SUPPLY
- COMPATIBLE WITH BR1941
- TTL, MOS COMPATIBILITY

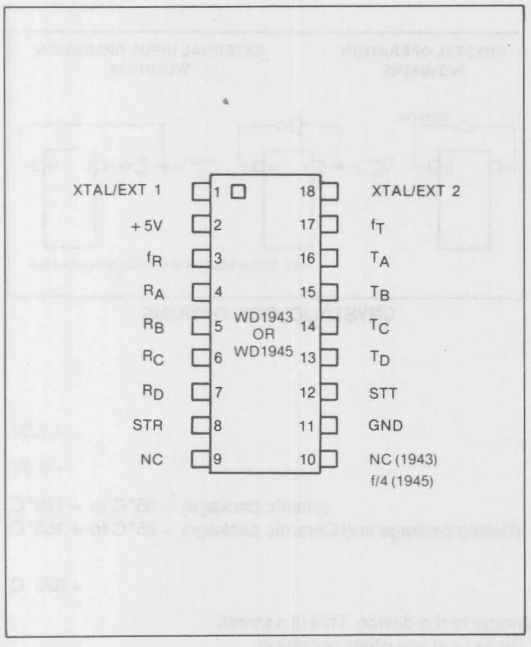
- WD1943 IS PIN COMPATIBLE TO THE COM8116
- WD1945 IS PIN COMPATIBLE TO THE COM8136 AND COM5036 (PIN 9 ON WD1945 IS A NO CONNECT)

GENERAL DESCRIPTION

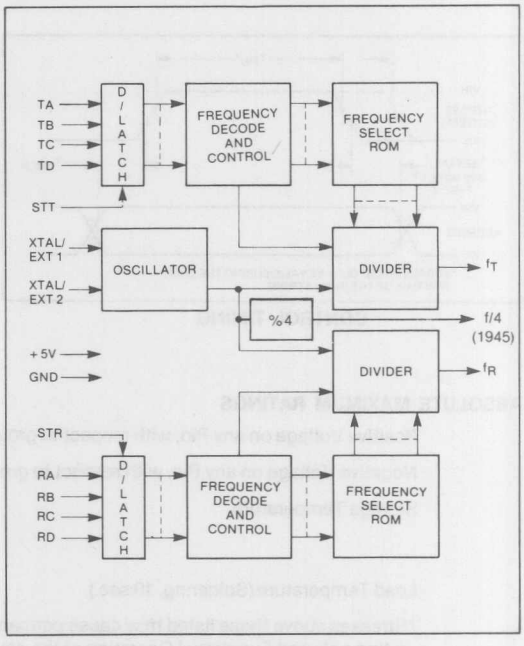
The WD1943/45 is an enhanced version of the BR1941 Dual Baud Rate Clock. The WD1943/45 is a combination Baud Rate Clock Generator and Programmable Divider. It is manufactured in N-channel MOS using silicon gate technology. This device is capable of generating 16 externally selected clock rates whose frequency is determined by either a single crystal or an externally generated input clock. The WD1943/45 is a programmable counter capable of generating a division by any integer from 4 to $2^{15} - 1$, inclusive.

The WD1943/45 is available programmed with the most used frequencies in data communication. Each frequency is selectable by strobing or hard wiring each of the two sets of four Rate Select inputs. Other frequencies/division rates can be generated by reprogramming the internal ROM coding through a MOS mask change. Additionally, further clock division may be accomplished through cascading of devices. The frequency output is fed into the XTAL/EXT input on a subsequent device.

The WD1943/45 can be driven by an external crystal or by TTL logic.



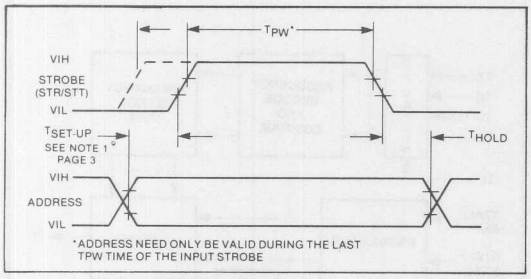
PIN CONNECTIONS



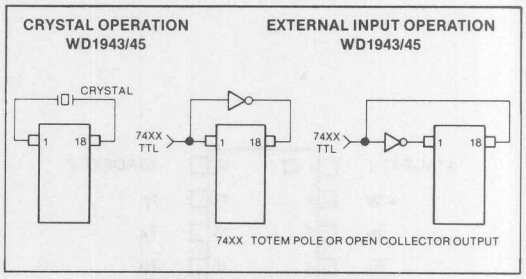
BLOCK DIAGRAM

PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME	FUNCTION
1	XTAL/EXT 1	Crystal or External Input 1	This input receives one pin of the crystal package or one polarity of the external input.
2	V_{CC}	Power Supply	+5 volt Supply
3	f_R	Receiver Output Frequency	This output runs at a frequency selected by the Receiver Address inputs.
4-7	R_A, R_B, R_C, R_D	Receiver Address	The logic level on these inputs as shown in Table 1 thru 6, selects the receiver output frequency, f_R.
8	STR	Strobe-Receiver Address	A high-level input strobe loads the receiver address (R_A, R_B, R_C, R_D) into the receiver address register. This input may be strobed or hard wired to +5V.
9	NC	No Connection	No Internal Connection
10	NC (1943) f/4 (1945)	No Connection freq/4 Output	No Internal Connection XTAL1 input freq divided by four.
11	GND	Ground	Ground
12	STT	Strobe-Transmitter Address	A high-level input strobe loads the transmitter address (T_A, T_B, T_C, T_D) into the transmitter address register. This input may be strobed or hard wired to +5V.
13-16	T_D, T_C, T_B, T_A	Transmitter Address	The logic level on these inputs, as shown in Table 1 thru 6, selects the transmitter output frequency, f_T.
17	f_T	Transmitter Output Frequency	This output runs at a frequency selected by the Transmitter Address inputs.
18	XTAL/EXT 2	Crystal or External Input 2	This input receives the other pin of the crystal package or the other polarity of the external input.



CONTROL TIMING



CRYSTAL/CLOCK OPTIONS

ABSOLUTE MAXIMUM RATINGS

Positive Voltage on any Pin, with respect to ground	+7.0V
Negative Voltage on any Pin, with respect to ground	−0.3V
Storage Temperature	(plastic package) −55°C to +125°C (Cerdip package and Ceramic package) −65°C to +150°C
Lead Temperature (Soldering, 10 sec.)	+325°C

*Stresses above those listed may cause permanent damage to the device. This is a stress rating only and Functional Operation of the device at these or at any other condition above those indicated in the operational sections of this specification are not implied.

ELECTRICAL CHARACTERISTICS (T_A = 0°C to +70°C, V_{CC} = +5V ±5% standard.)

PARAMETER	MIN	TYP	MAX	UNIT	COMMENTS
DC CHARACTERISTICS					
INPUT VOLTAGE LEVELS					
Low-level, V_{IL}			0.8	V	See Note 1
High-level, V_{IH}	2.0		V_{CC}	V	
OUTPUT VOLTAGE LEVELS					
Low-level, V_{OL}			0.4	V	I_{OL} = 3.2 mA
High-level, V_{OH}	V_{CC}-1.5	4.0		V	I_{OH} = 100μA
INPUT CURRENT					
High-level, I_{IH}			−10	μA	$V_{IN} = V_{CC}$ } STR (8) and STT (12) Only
Low-level, I_{IL}			10	μA	V_{IN} = GND }
Low-level, I_{IL}			300	μA	V_{IN} = GND (All inputs except XTAL, STR and STT)
INPUT CAPACITANCE					
All Inputs, C_{IN}		5	10	pf	V_{IN} = GND, excluding XTAL inputs
EXT. INPUT LOAD		4	5		Series 7400 unit loads
INPUT RESISTANCE					
Crystal Input, R_{XTAL}	1.1			KΩ	Resistance to ground for Pin 1 and Pin 18
POWER SUPPLY CURRENT I_{CC}		40	80	mA	
AC CHARACTERISTICS					T_A = +25°C
CLOCK FREQUENCY					See Note 2
PULSE WIDTH (T_{PW})					
Clock					50% Duty Cycle ± 10%. See Note 2
Receiver strobe	150		DC	ns	See Note 3
Transmitter strobe	150		DC	ns	See Note 3
INPUT SET-UP TIME (T_{SET-UP})					
Address	50			ns	See Note 3
OUTPUT HOLD TIME (T_{HOLD})					
Address	50			ns	
STROBE TO NEW FREQUENCY DELAY			6	CLK	

NOTE 1: XTAL/EXT inputs are either TTL compatible or crystal compatible. See crystal specification in Applications Information section.
All inputs except XTAL, STR and STT have internal pull-up resistors.

NOTE 2: Refer to frequency option tables for maximum input frequency on XTAL/EXT pins.
Typical clock pulse width is 1/2 x CL

NOTE 3: Input set-up time can be decreased to >0 ns by increasing the minimum strobe width (50 ns) to a total of 200 ns.
T_{A-D} and R_{A-D} have internal pull-up resistors.

OPERATION

Standard Frequencies

Choose a Transmitter and Receiver frequency from the table below. Program the corresponding address into TA-TD and RA-RD respectively using strobe pulses or by hard wiring the strobe and address inputs.

Non-Standard Frequencies

To accomplish non-standard frequencies do one of the following:

1. Choose a crystal that when divided by the WD1943 generates the desired frequency.
2. Cascade devices by using the frequency outputs as an input to the XTAL/EXT inputs of the subsequent WD1943/45.
3. Consult the factory for possible changes via ROM mask reprogramming.

FREQUENCY OPTIONS

TABLE 1. CRYSTAL FREQUENCY = 5.0688 MHZ

Transmit/Receive Address				Baud Rate	Theoretical	Actual	Percent	Duty Cycle	
D	C	B	A	(16X Clock)	Freq. (kHz)	Freq. (kHz)	Error	%	Divisor
0	0	0	0	50	0.8	0.8	—	50/50	6336
0	0	0	1	75	1.2	1.2	—	50/50	4224
0	0	1	0	110	1.76	1.76	—	50/50	2880
0	0	1	1	134.5	2.152	2.1523	0.016	50/50	2355
0	1	0	0	150	2.4	2.4	—	50/50	2112
0	1	0	1	300	4.8	4.8	—	50/50	1056
0	1	1	0	600	9.6	9.6	—	50/50	528
0	1	1	1	1200	19.2	19.2	—	50/50	264
1	0	0	0	1800	28.8	28.8	—	50/50	176
1	0	0	1	2000	32.0	32.081	0.253	50/50	158
1	0	1	0	2400	38.4	38.4	—	50/50	132
1	0	1	1	3600	57.6	57.6	—	50/50	88
1	1	0	0	4800	76.8	76.8	—	50/50	66
1	1	0	1	7200	115.2	115.2	—	50/50	44
1	1	1	0	9600	153.6	153.6	—	48/52	33
1	1	1	1	19,200	307.2	316.8	3.125	50/50	16

WD1943-00 or WD1945-00

TABLE 2. CLOCK FREQUENCY = 2.76480 MHZ

Transmit/Receive Address				Baud Rate	Theoretical	Actual	Percent	Duty Cycle	
D	C	B	A	(16X Clock)	Freq. (kHz)	Freq. (kHz)	Error	%	Divisor
0	0	0	0	50	0.8	0.8	—	50/50	3456
0	0	0	1	75	1.2	1.2	—	50/50	2304
0	0	1	0	110	1.76	1.76	−0.006	50/50	1571
0	0	1	1	134.5	2.152	2.152	−0.019	50/50	1285
0	1	0	0	150	2.4	2.4	—	50/50	1152
0	1	0	1	200	3.2	3.2	—	50/50	864
0	1	1	0	300	4.8	4.8	—	50/50	576
0	1	1	1	600	9.6	9.6	—	50/50	288
1	0	0	0	1200	19.2	19.2	—	50/50	144
1	0	0	1	1800	28.8	28.8	—	50/50	96
1	0	1	0	2000	32.0	32.15	+0.465	50/50	86
1	0	1	1	2400	38.4	38.4	—	50/50	72
1	1	0	0	3600	57.6	57.6	—	50/50	48
1	1	0	1	4800	76.8	76.8	—	50/50	36
1	1	1	0	9600	153.6	153.6	—	50/50	18
1	1	1	1	19,200	307.2	307.2	—	50/50	9

WD1943-02 or WD1945-02

TABLE 3. CRYSTAL FREQUENCY = 6.018305 MHZ

Transmit/Receive Address				Baud Rate	Theoretical	Actual	Percent	Duty Cycle	
D	C	B	A	(16X Clock)	Freq. (kHz)	Freq. (kHz)	Error	%	Divisor
0	0	0	0	50	0.8	.7999	0	50/50	7523*
0	0	0	1	75	1.2	1.2000	0	50/50	5015*
0	0	1	0	110	1.76	1.7597	0	50/50	3420
0	0	1	1	134.5	2.152	2.1517	0	50/50	2797*
0	1	0	0	150	2.4	2.3996	0	50/50	2508
0	1	0	1	200	3.2	3.1995	0	50/50	1881*
0	1	1	0	300	4.8	4.7993	0	50/50	1254
0	1	1	1	600	9.6	9.5986	0	50/50	627*
1	0	0	0	1200	19.2	19.2279	+0.14	50/50	31.3*
1	0	0	1	1800	28.8	28.7959	0	50/50	209*
1	0	1	0	2000	32.0	32.0125	0	50/50	188
1	0	1	1	2400	38.4	38.3334	−0.17	50/50	157*
1	1	0	0	3600	57.6	57.8687	+0.46	50/50	104
1	1	0	1	4800	76.8	77.1583	+0.46	50/50	78
1	1	1	0	9800	153.6	154.3166	+0.46	50/50	39*
1	1	1	1	19,200	307.2	300.9175	−2.04	50/50	20

WD1943-03 or WD1945-03

TABLE 4. CLOCK FREQUENCY = 5.52960 MHZ

Transmit/Receive Address				Baud Rate	Theoretical	Actual	Percent	Duty Cycle	
D	C	B	A	(32X Clock)	Freq. (kHz)	Freq. (kHz)	Error	%	Divisor
0	0	0	0	50	1.6	1.6	—	50/50	3456
0	0	0	1	75	2.4	2.4	—	50/50	2304
0	0	1	0	110	3.52	3.52	−0.006	50/50	1571
0	0	1	1	134.5	4.304	4.303	−0.019	50/50	1285
0	1	0	0	150	4.8	4.8	—	50/50	1152
0	1	0	1	200	6.4	6.4	—	50/50	864
0	1	1	0	300	9.6	9.6	—	50/50	576
0	1	1	1	600	19.2	19.2	—	50/50	288
1	0	0	0	1200	38.4	38.4	—	50/50	144
1	0	0	1	1800	57.6	57.6	—	50/50	96
1	0	1	0	2000	64.0	64.3	+0.465	50/50	86
1	0	1	1	2400	76.8	76.8	—	50/50	72
1	1	0	0	3600	115.2	115.2	—	50/50	48
1	1	0	1	4800	153.6	153.6	—	50/50	36
1	1	1	0	9600	307.2	307.2	—	50/50	18
1	1	1	1	19,200	614.4	614.4	—	50/50	9

WD1943-04 or WD1945-04

TABLE 5. CRYSTAL FREQUENCY = 4.9152 MHZ

Transmit/Receive Address				Baud Rate	Theoretical	Actual	Percent	Duty Cycle	
D	C	B	A	(16X Clock)	Freq. (kHz)	Freq. (kHz)	Error	%	Divisor
0	0	0	0	50	0.8	0.8	—	50/50	6144
0	0	0	1	75	1.2	1.2	—	50/50	4096
0	0	1	0	110	1.76	1.7598	−0.01	*	2793
0	0	1	1	134.5	2.152	2.152	—	50/50	2284
0	1	0	0	150	2.4	2.4	—	50/50	2048
0	1	0	1	300	4.8	4.8	—	50/50	1024
0	1	1	0	600	9.6	9.6	—	50/50	512
0	1	1	1	1200	19.2	19.2	—	50/50	256
1	0	0	0	1800	28.8	28.7438	−0.19	*	171
1	0	0	1	2000	32.0	31.9168	−0.26	50/50	154
1	0	1	0	2400	38.4	38.4	—	50/50	128
1	0	1	1	3600	57.6	57.8258	0.39	*	85
1	1	0	0	4800	76.8	76.8	—	50/50	64
1	1	0	1	7200	115.2	114.306	−0.77	*	43
1	1	1	0	9600	153.6	153.6	—	50/50	32
1	1	1	1	19,200	307.2	307.2	—	50/50	16

WD1943-05 or WD1945-05

TABLE 6. CRYSTAL FREQUENCY = 5.0688 MHZ

Transmit/Receive Address				Baud Rate	Theoretical	Actual	Percent	Duty Cycle	
D	C	B	A	(32X Clock)	Freq. (kHz)	Freq. (kHz)	Error	%	Divisor
0	0	0	0	50	1.6	1.6	—	50/50	3168
0	0	0	1	75	2.4	2.4	—	50/50	2112
0	0	1	0	110	3.52	3.52	—	50/50	1440
0	0	1	1	134.5	4.304	4.303	.026	50/50	1178
0	1	0	0	150	4.8	4.8	—	50/50	1056
0	1	0	1	200	6.4	6.4	—	50/50	792
0	1	1	0	300	9.6	9.6	—	50/50	528
0	1	1	1	600	19.2	19.2	—	50/50	264
1	0	0	0	1200	38.4	38.4	—	50/50	132
1	0	0	1	1800	57.6	57.6	—	50/50	88
1	0	1	0	2400	76.8	76.8	—	50/50	66
1	0	1	1	3600	115.2	115.2	—	50/50	44
1	1	0	0	4800	153.6	153.6	—	*	33
1	1	0	1	7200	230.4	230.4	—	50/50	22
1	1	1	0	9600	307.2	298.16	2.941	*	17
1	1	1	1	19,200	614.4	633.6	3.125	50/50	8

*When the duty cycle is not exactly 50% it is 50% ± 10%

WD1943-06 or WD1945-06

APPLICATIONS INFORMATION

OPERATION WITH A CRYSTAL

The WD1943/45 Baud Rate Generator may be driven by either a crystal or TTL level clock. When using a crystal, the waveform that appears at pins 1 (XTAL/EXT 1) and 18 (XTAL/EXT 2) does not conform to the normal TTL limits of $V_{IL} \leqslant 0.8V$ and $V_{IH} \geqslant 2.0V$. Figure 1 illustrates a typical crystal waveform when connected to a WD1943/45.

Since the D.C. level of the waveform causes the least positive point to typically be greater than 0.8V, the WD1943/45 is designed to look for an edge, as opposed to a TTL level. The XTAL/EXT logic triggers on a rising edge of typically 1V in magnitude. This allows the use of a crystal without any additional components.

OPERATIONS WITH TTL LEVEL CLOCK

With clock frequencies in the area of 5 MHz, significant overshoot and undershoot ("ringing") can appear at pins 1 and/or 18. The clock oscilator may, at times be triggered on a rising edge of an overshoot or undershoot waveform, causing the device to effectively "double-trigger." This phenomenon may result as a twice expected baud rate, or as an apparent device failure. Figure 2 shows a typical waveform that exhibits the "ringing" problem.

The design methods required to minimize ringing include the following:

1. Minimize the P.C. trace length. At 5 MHz, each inch of trace can add significantly to overshoot and undershoot.
2. Match impedances at both ends of the trace. For example, a series resistor near the device may be helpful.
3. A uniform impedance is important. This can be accomplished through the use of:
   a. parallel ground lines
   b. evenly spaced ground lines crossing the trace on the opposite side of PC board
   c. an inner plane of ground, e.g., as in a four layered PC board.

In the event that ringing exists on an already finished board, several techniques can be used to reduce it. These are:

1. Add a series resistor to match impedance as shown in Figure 3.
2. Add pull-up/pull-down resistor to match impedance, as shown in Figure 4.
3. Add a high speed diode to clamp undershoot, as shown in Figure 5.

The method that is easiest to implement in many systems is method 1, the series resistor. The series resistor will cause the D.C. level to shift up, but that does not cause a problem since the OSC is triggered by an edge, as opposed to a TTL level.

The 1943/45 Baud Rate Generator can save both board space and cost in a communications system. By choosing either a crystal or a TTL level clock, the user can minimize the logic required to provide baud rate clocks in a given design.

POWER LINE SPIKES

Voltage transients on the AC power line may appear on the DC power output. If this possibility exists, it is suggested that a by-pass capacitor is used between +5V and GND.

CRYSTAL SPECIFICATIONS

User must specify termination (pin, wire, other)
Frequency — See Tables 1-6.
Temperature range 0°C to +70°C
Series resistance $\leqslant 50\Omega$
Series resonant
Overall tolerance ± 0.01%

CRYSTAL MANUFACTURERS (Partial List)

American Time Products Div.
Frequency Control Products, Inc.
61-20 Woodside Ave.
Woodside, New York 11377
(213) 458-5811

Bliley Electric Co.
2545 Grandview Blvd.
Erie, Pennsylvania 16508
(814) 838-3571

M-tron Ind. Inc.
P.O. Box 630
Yankton, South Dakota 57078
(605) 665-9321

Erie Frequency Control
453 Lincoln St.
Calisle, Pennsylvania 17013
(714) 249-2232

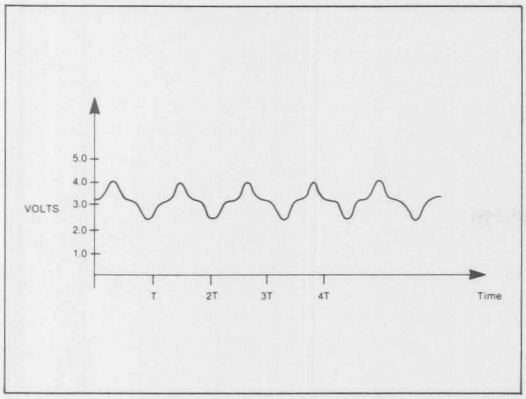


Figure 1. TYPICAL CRYSTAL WAVEFORM

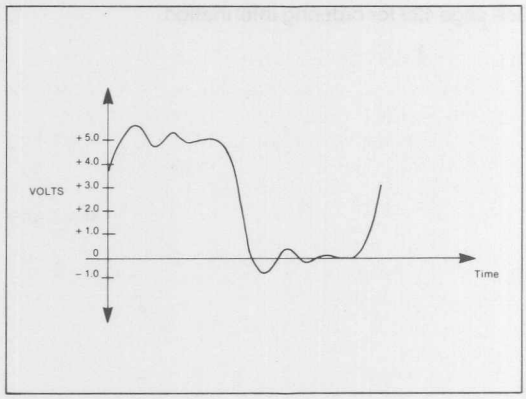


Figure 2. TYPICAL "RINGING" WAVEFORM from TTL INPUT

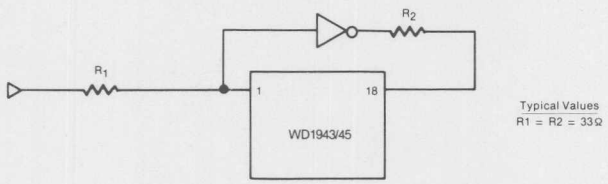


Figure 3. SERIES RESISTOR TO MATCH IMPEDANCE

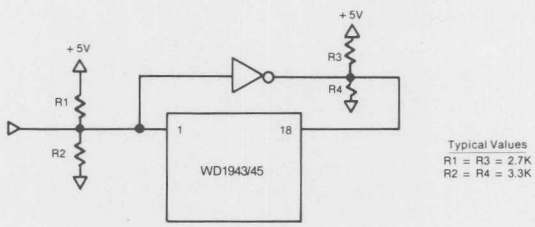


Figure 4. PULL-UP/PULL-DOWN RESISTORS TO MATCH IMPEDANCE

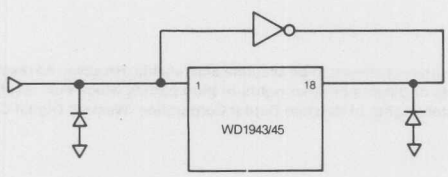


Figure 5. HIGH-SPEED DIODE TO CLAMP UNDERSHOOT

See page 429 for ordering information.

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Printed in U.S.A.

WD2001/WD2002 Data Encryption Devices

FEATURES

- CERTIFIED BY NATIONAL BUREAU OF STANDARDS.
- TRANSFER RATE:
  WD2001/2-05 300Kbs with 500KHz clock
  WD2001/2-20 1.3 Mbs with 2MHz clock
  WD2001/2-30 1.8 Mbs with 3MHz clock
- ENCRYPTS/DECRYPTS 64 BIT DATA WORDS USING 56 BIT KEY WORD
- SINGLE PORT 28 PIN PACKAGE WD2001 OR DUAL PORT 40 PIN PACKAGE WD2002
- COMMAND BIT PROGRAMMING VIA DAL BUS OR INPUT PINS
- DMA COMPATIBLE (SEE WESTERN DIGITAL DM1883)
- PARITY CHECK ON KEY WORD LOADING
- STANDARD 8 BIT MICROPROCESSOR INTERFACE
- INPUTS AND OUTPUTS TTL COMPATIBLE
- KEY STORED ON CHIP IS NOT EXTERNALLY ACCESSIBLE

  SEPARATE CLEAR AND CIPHER BUS STRUCTURE ON WD2002

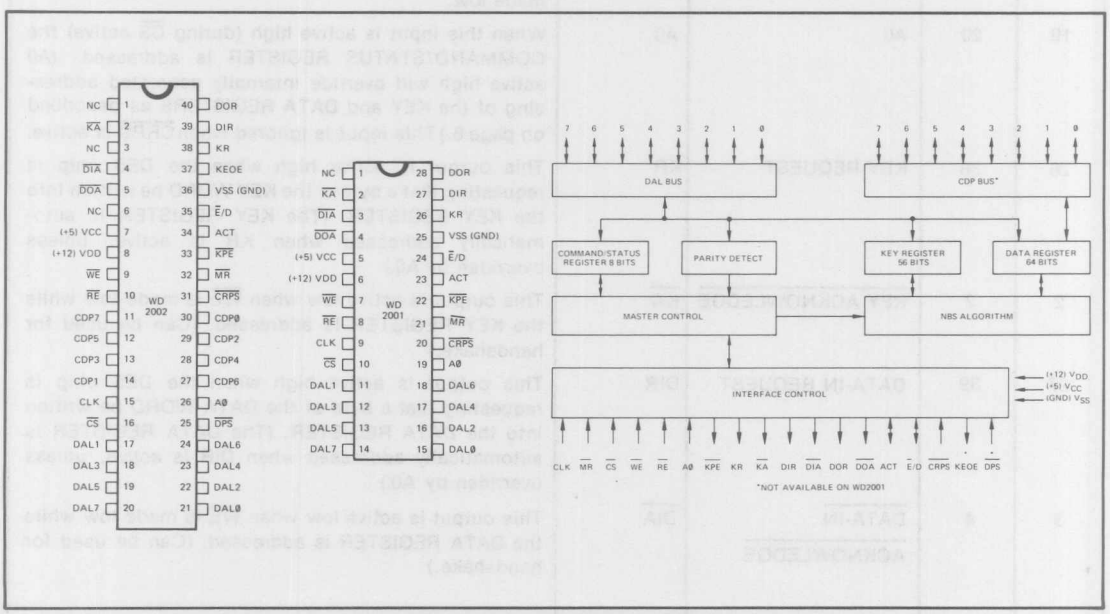
APPLICATIONS

- SECURE BROKERAGE TRANSACTIONS
- ELECTRONIC FUNDS TRANSFERS
- SECURE BANKING/BUSINESS ACCOUNTING
- MAINFRAME COMMUNICATIONS
- REMOTE AND HOST COMPUTER COMMUNICATIONS
- SECURE A/D
- SECURE DISK OR MAG TAPE DATA STORAGE
- SECURE PACKET SWITCHING TRANSMISSION

GENERAL DESCRIPTION

The Western Digital WD2001 and WD2002 Data Encryption/Decryption devices are designed to encrypt and decrypt 64-bit blocks of data using the algorithm specified in the Federal Information Processing Data Encryption Standard (#46). These devices encrypt a 64-Bit clear text word using a 56-Bit user-specified key to produce a 64-Bit cipher text word. When reversed, the cipher text word is decrypted to produce the original clear text word.

The DE2001/2 are fabricated in N-channel silicon gate MOS technology and are TTL compatible on all inputs and outputs.



WD2001/WD2002 BLOCK DIAGRAM

PIN OUTS

PIN NO.		PIN NAME	SYMBOL	FUNCTION
WD2001	WD 2002			
11-18	17-24	DATA LINES	DAL 0 → DAL 7	Eight active true three-state bi-directional I/O lines used for information transfer to and from the DES chip's registers. During single port operation, all COMMAND/STATUS, KEY WORD and DATA WORD transfers are via this bus. During dual port operation, all COMMAND/STATUS, KEY WORD and clear DATA WORD transfers are via this bus. (Cipher DATA WORD transfers are via the CIPHER DATA PORT (CDP) bus.)
N/A	11-14 27-30	CIPHER DATA PORT	CDP 0 → CDP 7	Eight active true three-state bi-directional I/O lines used only in dual port operation. Cipher DATA WORD transfers are via this bus. These pins are available on the WD2002 40 pin package version only.
6	8	POWER SUPPLY	V_{DD}	+ 12v
5	7	POWER SUPPLY	V_{CC}	+ 5v
25	36	GROUND	V_{SS}	GROUND
9	15	CLOCK	CLK	System clock input.
21	32	$\overline{\text{MASTER RESET}}$	$\overline{\text{MR}}$	$\overline{\text{MR}}$ active low resets the COMMAND/STATUS REGISTER and resets internal circuitry. (Requires active clock for reset operation.)
10	16	$\overline{\text{CHIP SELECT}}$	$\overline{\text{CS}}$	$\overline{\text{CS}}$ is made low to access registers within the device.
8	10	$\overline{\text{READ ENABLE}}$	$\overline{\text{RE}}$	The contents of the selected register are placed on the DAL (or CDP) bus lines when $\overline{\text{CS}}$ and $\overline{\text{RE}}$ are made low.
7	9	$\overline{\text{WRITE ENABLE}}$	$\overline{\text{WE}}$	Information on the DAL (or CDP) bus lines is written into the selected DES register when $\overline{\text{CS}}$ and $\overline{\text{WE}}$ are made low.
19	26	A0	A0	When this input is active high (during $\overline{\text{CS}}$ active) the COMMAND/STATUS REGISTER is addressed. (A0 active high will override internally generated addressing of the KEY and DATA REGISTERS as described on page 6.) This input is ignored when $\overline{\text{CRPS}}$ is active.
26	38	KEY REQUEST	KR	This output is active high when the DES chip is requesting that a byte of the KEY WORD be written into the KEY REGISTER. (The KEY REGISTER is automatically addressed when KR is active, unless overriden by A0.)
2	2	$\overline{\text{KEY ACKNOWLEDGE}}$	$\overline{\text{KA}}$	This output is active low when $\overline{\text{WE}}$ is made low while the KEY REGISTER is addressed. (Can be used for handshake.)
27	39	DATA-IN REQUEST	DIR	This output is active high when the DES chip is requesting that a byte of the DATA WORD be written into the DATA REGISTER. (The DATA REGISTER is automatically addressed when DIR is active, unless overriden by A0.)
3	4	$\overline{\text{DATA-IN}}$ $\overline{\text{ACKNOWLEDGE}}$	$\overline{\text{DIA}}$	This output is active low when $\overline{\text{WE}}$ is made low while the DATA REGISTER is addressed. (Can be used for handshake.)

PIN NO.		PIN NAME	SYMBOL	FUNCTION
WD2001	WD2002			
28	40	DATA-OUT REQUEST	DOR	This output is active high when the DES chip is requesting that a byte of the DATA WORD be read from the DATA REGISTER. (The DATA REGISTER is automatically addressed when the DOR is active, unless overridden by A0.)
4	5	$\overline{\text{DATA-OUT ACKNOWLEDGE}}$	$\overline{\text{DOA}}$	This output is active low when $\overline{\text{RE}}$ is made low while the DATA REGISTER is addressed. (Can be used for handshake.)
22	33	$\overline{\text{KEY PARITY ERROR}}$	$\overline{\text{KPE}}$	This output is active low when enabled via the COMMAND/STATUS REGISTER BIT 2 (KEOE) and a parity error has been detected during loading of the KEY REGISTER.
20	31	$\overline{\text{COMMAND REGISTER PIN SELECT}}$	$\overline{\text{CRPS}}$	This input selects DAL bus or input pin programming of the COMMAND/STATUS REGISTER. $\overline{\text{CRPS}}$ high or open selects DAL bus programming. $\overline{\text{CRPS}}$ low selects input pin programming.
23	34	ACTIVATE	ACT	When $\overline{\text{CRPS}}$ is high or open, this pin is an output reflecting the status of the ACTIVATE bit (bit 1) of the COMMAND/STATUS REGISTER. When $\overline{\text{CRPS}}$ is low, this pin is an input that overrides the ACTIVATE bit of the COMMAND/STATUS REGISTER.
N/A	37	KEY ERROR OUTPUT ENABLE	KEOE	This output indicates the status of the KEY ERROR OUTPUT ENABLE bit (bit 2) of the COMMAND/STATUS REGISTER. This output is active when input pin programming is selected ($\overline{\text{CRPS}}$ low). This pin is available on the WD2002 40 pin package version only.
24	35	$\overline{\text{ENCRYPT}}$/DECRYPT	$\overline{\text{E}}$/D	When $\overline{\text{CRPS}}$ is high or open, this pin is an output reflecting the status of the $\overline{\text{ENCRYPT}}$/DECRYPT bit (bit 3) of the COMMAND/STATUS REGISTER. When $\overline{\text{CRPS}}$ is low, this pin is an input pin that overrides the $\overline{\text{ENCRYPT}}$/DECRYPT bit of the COMMAND/STATUS REGISTER.
N/A	25	$\overline{\text{DUAL PORT SELECT}}$	$\overline{\text{DPS}}$	When this input is high or open, single port operation is selected and all DES chip transfers are via the DAL bus. When $\overline{\text{DPS}}$ is low, dual port operation is selected and both the DAL bus and the CDP bus are used [separate busses for clear data (DAL bus) and cipher data (CDP bus)]. This pin is available on the WD2002 40 pin package version only.

NOTE: The WD2001 28 pin package version does not have the following pins:
The 8 CDP pins, the KEOE pin, and the $\overline{\text{DPS}}$ pin.

ORGANIZATION

The Data Encryption Standard chip consists of a 56-bit KEY REGISTER, a 64-bit DATA REGISTER, an 8-bit COMMAND/STATUS REGISTER, plus the necessary logic to check KEY parity and implement the NBS algorithm. A typical system implementation is shown on page 10 and the block diagram is shown on page 1. Although the DES chip interfaces to a wide variety of processors including mini-computers, the interface is tailored to the 8080A class microprocessor.

GENERAL OPERATING DESCRIPTION

The user programs the DES chip for encryption or decryption, and single or dual port operation.* Data is encrypted/decrypted with a 64-bit user defined KEY WORD. Data encrypted with a given KEY WORD can be decrypted only using that KEY WORD. The KEY REGISTER is loaded by the computer with eight successive 8-bit bytes. Parity is checked on each byte of the KEY WORD as it is loaded into the KEY REGISTER (The 8th bit (DAL0) of each 8-bit byte is reserved for odd parity for that byte and is not used in the algorithm calculation.) Similarly the DATA REGISTER is loaded with eight successive 8-bit bytes. The DATA REGISTER is read by reading eight successive 8-bit bytes.

When the DES chip is programmed for encryption, the DATA REGISTER is loaded with eight bytes of plain or clear text. The DES chip encrypts the data, then the encrypted data may be read from the DATA REGISTER (64-bits of encrypted text). When the DES chip is programmed for decryption, the DATA REGISTER is loaded with eight bytes of encrypted or cipher text. The DES chip decrypts the data, then the plain text may be read from the DATA REGISTER (64-bits of plain text). Note that all transfers to and from the KEY REGISTER and/or DATA REGISTER must occur in eight successive 8-bit bytes.

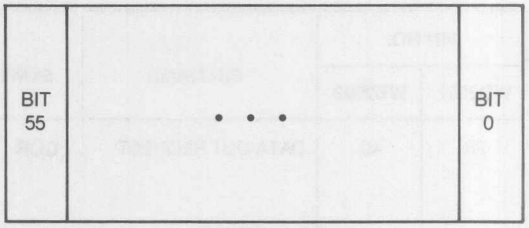
***Note:** Dual port operation available with WD2002 40 pin package version only. (Single and dual port operation is described in detail under PART V. OPERATION.)

REGISTER DESCRIPTION

The following describes the KEY, DATA, and COMMAND/STATUS REGISTERS of the DES chip.

Key Register

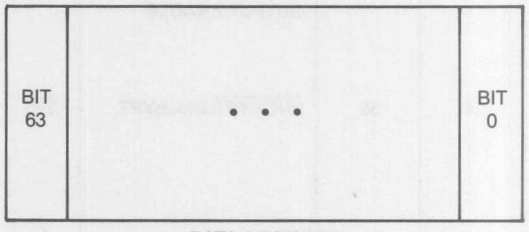
This 56-bit register contains the KEY by which the Data Encryption Algorithm operates. Eight successive bytes are needed to load the KEY REGISTER. The KEY REGISTER can be loaded only when there is a KEY REQUEST (Status bit and output). THIS REGISTER IS LOAD ONLY AND CANNOT BE READ.



KEY REGISTER (LOAD ONLY)

Data Register

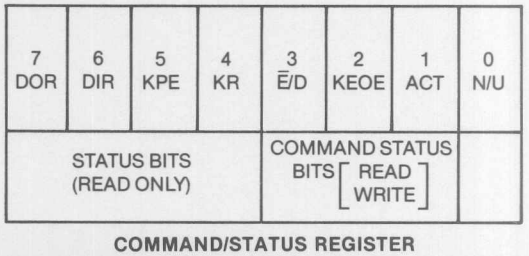
This 64-bit register contains plain or cipher text. When in the encrypt mode, the DATA REGISTER is loaded with plain text, and when read contains cipher text. When in the decrypt mode, the DATA REGISTER is loaded with cipher text, and when read contains plain text. The DATA REGISTER is always read or loaded with eight successive byte transfers. The DATA REGISTER can be loaded only when there is a DATA-IN REQUEST (status bit and output); similarly the DATA REGISTER can be read only when there is a DATA-OUT REQUEST (status bit and output).



DATA REGISTER

Command/Status Register (C/S R)

This 8-bit register controls the operation of the DES chip and monitors its status. Bits 7, 6, 5 and 4 are status-only bits (read only). Bits 3, 2 and 1 are COMMAND/STATUS bits (read/write). Bit 0 is not used. The COMMAND/STATUS bits (bits 3, 2, and 1) are normally loaded only once for an entire encrypt or decrypt process.



COMMAND/STATUS REGISTER

COMMAND/STATUS REGISTER (C/S R)

Bit	Name	Function
C/S R0	NOT USED	
C/S R1	ACTIVATE	This bit must be set from '0' to '1' to initiate loading the KEY REGISTER. This bit must be '1' for encrypt/decrypt operation. This is a read/write bit.
C/S R2	KEY ERROR OUTPUT ENABLE (KEOE)	When '0', the $\overline{\text{KEY PARITY ERROR}}$ output pin ($\overline{\text{KPE}}$) remains inactive regardless of the status of the $\overline{\text{KEY PARITY ERROR}}$ bit (bit 5). When '1', the $\overline{\text{KEY PARITY ERROR}}$ output pin is active when the KPE bit (bit 5) is '1'. This bit is set to '1' upon a MASTER RESET. This is a read/write bit.
C/S R3	$\overline{\text{ENCRYPT}}$/DECRYPT ($\overline{\text{E}}$/D)	When '0' data is to be encrypted. When '1' data is to be decrypted. This is a read/write bit.
C/S R4	KEY REQUEST (KR)	This bit is set one clock period after the ACTIVATE bit is set (from '0' to '1'). It is reset upon loading of the 8th and final byte of the KEY REGISTER. This is a read only bit.
C/S R5	KEY PARITY ERROR (KPE)	This bit is set internally upon detection of a parity error during loading of the KEY REGISTER. It is reset when the ACTIVATE bit is programmed from '1' to '0' (i.e., chip is deactivated). This is a read only bit.
C/S R6	DATA-IN REQUEST (DIR)	This bit is set upon either: a) Completion of KEY REGISTER loading - or - b) Completion of DATA REGISTER reading, (ie, the last DATA-OUT REQUEST has been serviced by an 8-byte read and the DATA REGISTER is now empty and ready to be loaded with the next DATA WORD). It is reset upon loading of the 8th and final byte of the DATA REGISTER. This is a read only bit.
C/S R7	DATA-OUT REQUEST (DOR)	This bit is set upon completion of the internal encrypt/decrypt calculation of a DATA WORD. It is reset upon reading of the 8th and final byte of the DATA REGISTER. This is a read only bit.

Note: All bits of the COMMAND/STATUS REGISTER are reset to '0' upon MASTER RESET, except bit 2 (KEOE) which is set to '1' and bit 0 (not used) which will read '1' by default during a COMMAND/STATUS REGISTER read.

DETAILED OPERATING DESCRIPTION

The DES chip is initiated by programming a '1' in the ACTIVATE bit of the COMMAND/STATUS REGISTER. The DES chip will respond by activating the KEY REQUEST (KR) bit (bit 4) of the STATUS REGISTER and the KEY REQUEST output.

The user must deactivate A0 (allowing the chip to internally address the KEY REGISTER), and load the KEY REGISTER with the 64-bit KEY WORD. The KEY REGISTER is loaded with 8 consecutive 8-bit bytes by activating $\overline{WE}$ 8 times (with $\overline{CS}$ active).

When $\overline{WE}$ is made active, the DES chip deactivates the KR output. When $\overline{WE}$ is deactivated, the KR output is again activated. The DES chip will activate 8 KEY REQUESTs in this fashion until the KEY REGISTER is full.

Also, when $\overline{WE}$ is made active, the DES chip responds by activating the $\overline{KEY\ ACKNOWLEDGE}$ ($\overline{KA}$) output. Thus, 8 $\overline{KA}$ activations will be made.

The KR and $\overline{KA}$ outputs can be used for asynchronous handshaking (as in DMA control) or further activations following the first KR can be ignored and the KEY REGISTER can be loaded in a synchronous (programmed I/O) manner via 8 successive activations of $\overline{WE}$.

Each byte of the KEY WORD is checked for odd parity as it is loaded. If a parity error is found, the chip will set the KEY PARITY ERROR (KPE) bit (bit 5) of the COMMAND/STATUS REGISTER. If the KEY ERROR OUTPUT ENABLE bit (bit 2) of the COMMAND/STATUS REGISTER has been set, the DES chip will also activiate the $\overline{KPE}$ output. The KPE bit will be reset when the ACTIVATE bit is re-programmed to a '0'.

After loading the last (8th) byte of the KEY WORD into the KEY REGISTER, the DES chip will set the DATA-IN REQUEST bit (bit 6) of the STATUS REGISTER and activate the DATA-IN REQUEST (DIR) output. The 64-bit DATA WORD must then be loaded into the DATA REGISTER. The DATA REGISTER is loaded in the same manner as the KEY REGISTER via 8 successive activations of DATA-IN REQUEST (DES output), $\overline{WE}$ (DES input, and DATA-IN ACKNOWLEDGE (DES output).

After the last (8th) byte of the DATA WORD has been loaded, the chip begins the internal calculation of the NBS algorithm. Upon completion of the calculation, the new data is internally loaded into the DATA REGISTER, and the DES chip sets the DATA-OUT REQUEST bit (bit 7) of the STATUS REGISTER and activates the DATA-OUT REQUEST (DOR) output. The DATA WORD must then be read from the DATA REGISTER. The DATA REGISTER is read in the same manner as it was loaded via 8 successive activations of DATA-OUT REQUEST (DES output), $\overline{RE}$ (DES input), and $\overline{DATA\text{-}OUT\ ACKNOWLEDGE}$ (DES output).

Again, for both data-in and data-out, further activations of the DIR, DOR and $\overline{DIA}$, $\overline{DOA}$ outputs, after the first request, can be ignored and the DATA REGISTER loaded (read) by 8 successive activations of $\overline{WE}$ ($\overline{RE}$).

After the last (8th) byte of the DATA REGISTER has been read, the DES chip will reactivate the DATA-IN REQUEST. This cycle of loading the DATA REGISTER, internal algorithm calculation, and reading the new data from the DATA REGISTER can continue indefinitely until all desired data has been encrypted or decrypted with the current KEY WORD.

After all desired data has been encrypted/decrypted with the current KEY WORD, the ACTIVATE bit of the COMMAND/STATUS REGISTER should be programmed to '0'. When the ACTIVATE bit has been reset to '0', an unauthorized user will not have access to the last KEY loaded into the DES chip since to resume operation, the ACTIVATE bit must be programmed to '1' which activates KEY REQUEST and a new KEY must be loaded before access to the DATA REGISTER is possible.

To encrypt plain data, plain data is loaded into the DATA REGISTER, and encrypted data is read from the DATA REGISTER. (The $\overline{ENCRYPT}$/DECRYPT bit (bit 3 of the COMMAND/STATUS REGISTER) must have been previously programmed to '0'.)

To decrypt encrypted data, encrypted data is loaded into the DATA REGISTER, and plain data is read from the DATA REGISTER. (The $\overline{ENCRYPT}$/DECRYPT bit must have been previously programmed to '1'.)

Note: If it is desired to switch from encrypt to decrypt (or vice versa) under the same KEY WORD, this can be accomplished before a DATA WORD transfer is initiated. By making A0 high, the DES chip will override the internal addressing of the DATA REGISTER, and address the COMMAND/STATUS REGISTER. The COMMAND/STATUS REGISTER can be re-programmed. When A0 is returned to a low state, the DES chip will internally address the DATA REGISTER awaiting loading of the next DATA WORD.

DUAL PORT OPTION

(Available on WD2002 40 Pin Version Only)

When the $\overline{DUAL\ PORT\ SELECT}$ ($\overline{DPS}$) input is high or left open (ie., single port operation is selected), all transfers to/from the DES chip are via the DAL bus. The CDP bus is not used and remains three-stated.

When $\overline{DPS}$ is made low (ie., dual port operation is selected), all transfers to/from the COMMAND/STATUS REGISTER, and transfers to the KEY REGISTER are still via the DAL bus. Clear DATA WORDS are also transferred via the DAL bus. However, cipher DATA WORDS are now transferred via the CDP bus. This provides separate busses for clear and ciphered text.

Encryption during dual port operation requires loading clear data via the DAL bus, and reading cipher data via the CDP bus.

Decryption during dual port operation requires loading cipher data via the CDP bus, and reading clear data via the DAL bus.

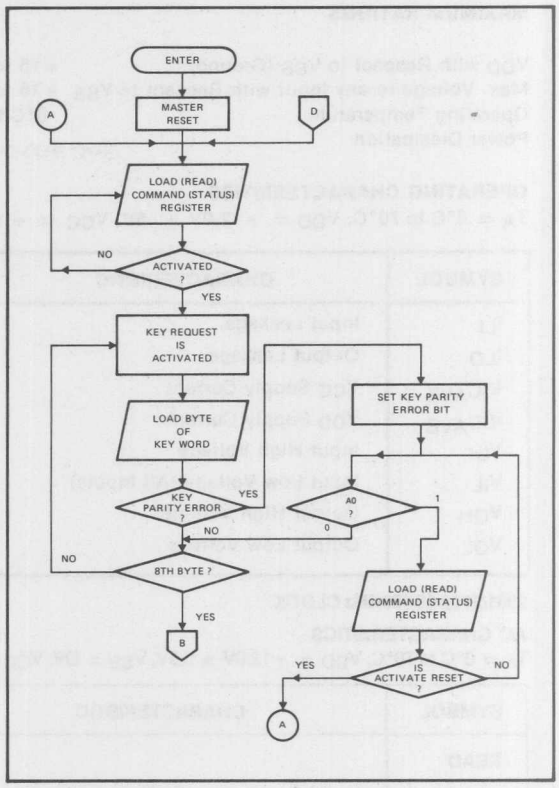
COMMAND SELECT OPTION

When the COMMAND REGISTER PIN SELECT ($\overline{CRPS}$) input is made low, the ACT and $\overline{E}/D$ pins are enabled as inputs. These inputs override bits 1 and 3 (respectively) of the COMMAND/STATUS REGISTER. This allows input pin control of the DES chip. The KEOE bit (bit 2) of the COMMAND/STATUS REGISTER will be held to '1'.

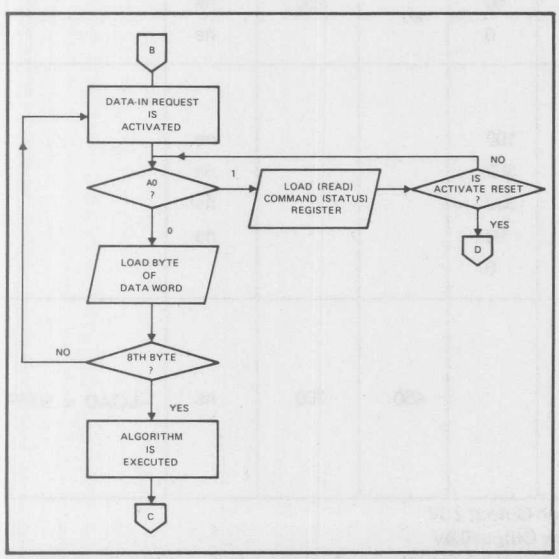
Input A0 will be disregarded in this mode of operation, and the COMMAND/STATUS REGISTER cannot be accessed via the DAL lines.

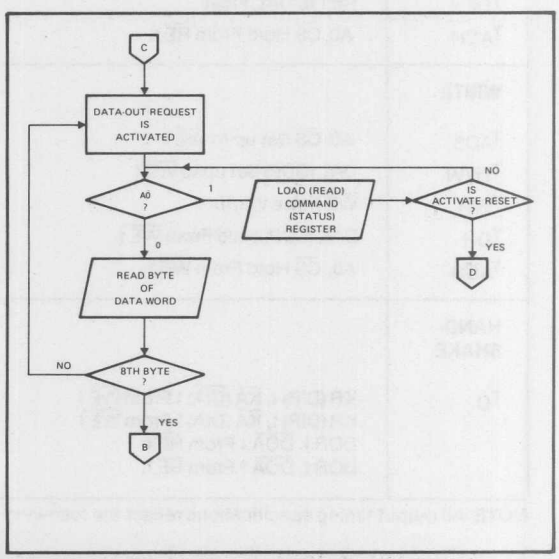
Note that the ACT pin must be toggled from '1' to a '0' to clear a parity error detection in this mode of operation.

All other operation remains as described previously.



WD2001/WD2002 FLOW CHARTS





MAXIMUM RATINGS

V_{DD} with Respect to V_{SS} (Ground)	+15 to - 0.3V	Storage Temp. Ceramic	-65°C to +150°C
Max. Voltage to any Input with Respect to V_{SS}	+15 to - 0.3V	Plastic	-55°C to +125°C
Operating Temperature	0°C to 70°C		
Power Dissipation	1 W		

OPERATING CHARACTERISTICS

T_A = 0°C to 70°C, V_{DD} = +12.0V ± .6V, V_{CC} = + 5.0V ± .25V, V_{SS} = OV

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNITS	CONDITIONS
I_{LI}	Input Leakage			10	uA	$V_{IN} = V_{DD}$
I_{LO}	Output Leakage			10	uA	$V_{OUT} = V_{CC}$
I_{CCAVE}	V_{CC} Supply Current		68	100	mA	
I_{DDAVE}	V_{DD} Supply Current		17	25	mA	
V_{IH}	Input High Voltage	2.4			V	
V_{IL}	Input Low Voltage (All Inputs)			.8	V	
V_{OH}	Output High Voltage	2.8			V	I_O = -100uA
V_{OL}	Output Low Voltage			.4	V	I_O = 1.6 mA

2001/2002-05 500KHz CLOCK

AC CHARACTERISTICS

T_A = 0°C to 70°C, V_{DD} = +12.0V ± 0.6V, V_{SS} = OV, V_{CC} = +5.0 ± .25V

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNITS	CONDITIONS
READ						
T_{ACS}	A0, $\overline{CS}$ Set up to $\overline{RE}\downarrow$	100			ns	
T_{RDV}	$\overline{RE}\downarrow$ to DAL (CDP) Valid			500	ns	C_{LOAD} = 50PF
T_{RD}	$\overline{RE}$ Pulse Width	500			ns	
T_{DF}	$\overline{RE}\uparrow$ to DAL Float	50		250	ns	
T_{ACH}	A0, $\overline{CS}$ Hold From $\overline{RE}\uparrow$	0			ns	
WRITE						
T_{ACS}	A0, $\overline{CS}$ Set up to $\overline{WE}\downarrow$	100			ns	
T_{DVW}	DAL (CDP) Set up to $\overline{WE}\uparrow$	300			ns	
T_{WR}	$\overline{WE}$ Pulse Width	300			ns	
T_{DH}	DAL (CDP) Hold From $\overline{WE}\uparrow$	90			ns	
T_{ACH}	A0, $\overline{CS}$ Hold From $\overline{WE}\uparrow$	0				
HAND-SHAKE						
T_D	KR (DIR)↓, $\overline{KA}$ ($\overline{DIA}$)↓ From $\overline{WE}\downarrow$ KR (DIR)↑, $\overline{KA}$ (DIA)↑ From $\overline{WE}\uparrow$ DOR↓, $\overline{DOA}$↓ From $\overline{RE}\downarrow$ DOR↑, $\overline{DOA}$↑ From $\overline{RE}\uparrow$		450	700	ns	C_{LOAD} = 50PF

NOTE: All output timing specifications reflect the following: High Output 2.0V
Low Output 0.8V

2001/2002-20 2MHz CLOCK

AC CHARACTERISTICS

T_A = 0°C to 70°C, V_{DD} = +12.0V ± 0.6V, V_{SS} = OV, V_{CC} = +5.0 ± .25V

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNITS	CONDITIONS
READ						
T_{ACS}	A0, $\overline{CS}$ Set up to $\overline{RE}\downarrow$	80			ns	
T_{RDV}	$\overline{RE}\downarrow$ to DAL (CDP) Valid			330	ns	C_{LOAD} = 50PF
T_{RD}	$\overline{RE}$ Pulse Width	330			ns	
T_{DF}	$\overline{RE}\uparrow$ to DAL Float	30		200	ns	
T_{ACH}	A0, $\overline{CS}$ Hold From $\overline{RE}\uparrow$	0			ns	
WRITE						
T_{ACS}	A0, $\overline{CS}$ Set up to $\overline{WE}\downarrow$	80			ns	
T_{DVW}	DAL (CDP) Set up to $\overline{WE}\uparrow$	200			ns	
T_{WR}	$\overline{WE}$ Pulse Width	200			ns	
T_{DH}	DAL (CDP) Hold From $\overline{WE}\uparrow$	90			ns	
T_{ACH}	A0, $\overline{CS}$ Hold From $\overline{WE}\uparrow$	0				
HAND-SHAKE						
T_D	KR (DIR)↓, $\overline{KA}$ ($\overline{DIA}$)↓ From $\overline{WE}\downarrow$ KR (DIR)↑, $\overline{KA}$ ($\overline{DIA}$)↑ From $\overline{WE}\uparrow$ DOR↓, $\overline{DOA}$↓ From $\overline{RE}\downarrow$ DOR↑, $\overline{DOA}$↑ From $\overline{RE}\uparrow$		300	450	ns	C_{LOAD} = 50PF

NOTE: All output timing specifications reflect the following: High Output 2.0V
Low Output 0.8V

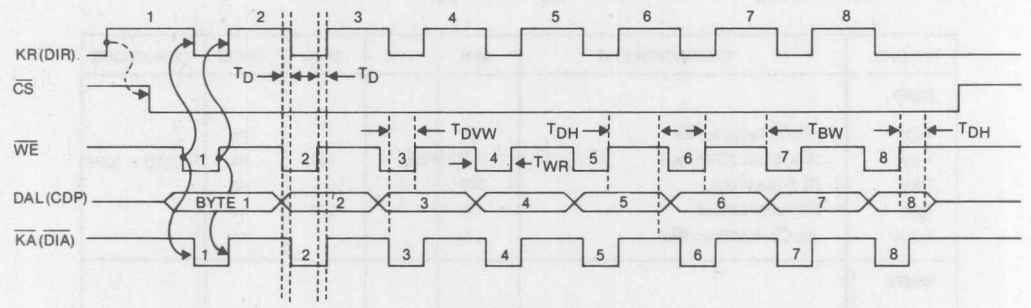
2001/2002-30 3MHz CLOCK

AC CHARACTERISTICS

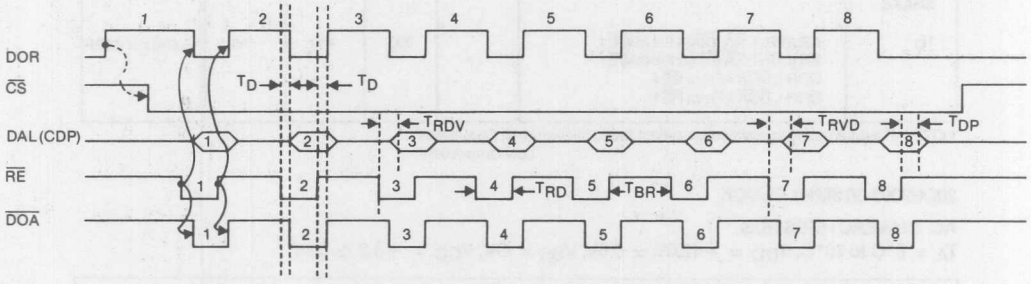
T_A = 0°C to 70°C, V_{DD} = +12.0V ± 0.6V, V_{SS} = OV, V_{CC} = +5.0 ± .25V

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNITS	CONDITIONS
READ						
T_{ACS}	A0, $\overline{CS}$ Set up to $\overline{RE}\downarrow$	50			ns	
T_{RDV}	$\overline{RE}\downarrow$ to DAL (CDP) Valid			220	ns	C_{LOAD} = 50PF
T_{RD}	$\overline{RE}$ Pulse Width	300			ns	
T_{DF}	$\overline{RE}\uparrow$ to DAL Float	20		130	ns	
T_{ACH}	A0, $\overline{CS}$ Hold From $\overline{RE}\uparrow$	0			ns	
WRITE						
T_{ACS}	A0, $\overline{CS}$ Set up to $\overline{WE}\downarrow$	50			ns	
T_{DVW}	DAL (CDP) Set up to $\overline{WE}\uparrow$	130			ns	
T_{WR}	$\overline{WE}$ Pulse Width	175			ns	
T_{DH}	DAL (CDP) Hold From $\overline{WE}\uparrow$	60			ns	
T_{ACH}	A0, $\overline{CS}$ Hold From $\overline{WE}\uparrow$	0				
HAND-SHAKE						
T_D	KR (DIR)↓, $\overline{KA}$ ($\overline{DIA}$)↓ From $\overline{WE}\downarrow$ KR (DIR)↑, $\overline{KA}$ ($\overline{DIA}$)↑ From $\overline{WE}\uparrow$ DOR↓, $\overline{DOA}$↓ From $\overline{RE}\downarrow$ DOR↑, $\overline{DOA}$↑ From $\overline{RE}\uparrow$		150	300	ns	C_{LOAD} = 50PF

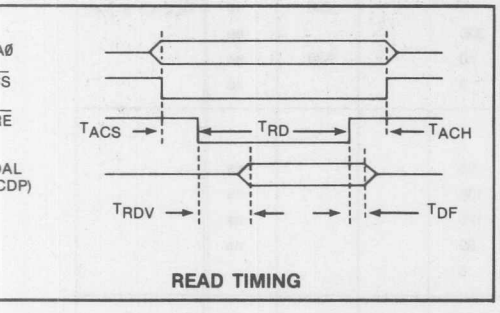
NOTE: All output timing specifications reflect the following: High Output 2.0V
Low Output 0.8V



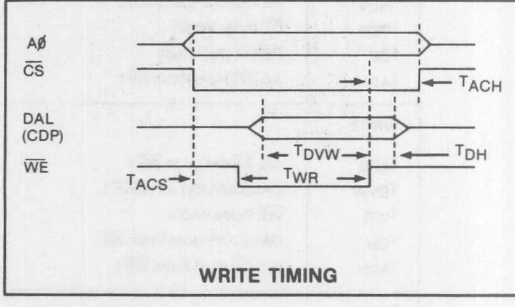
TYPICAL KEY OR DATA REGISTER LOAD



TYPICAL DATA REGISTER READ & TIMING



READ TIMING



WRITE TIMING

MISCELLANEOUS TIMING

1. CLOCK INPUT

FREQUENCY MAX.	FREQUENCY MIN.	PULSE WIDTH MIN
500KHz	100KHz	500nsec
2 MHz	100KHz	250nsec
3 MHz	100KHz	165nsec

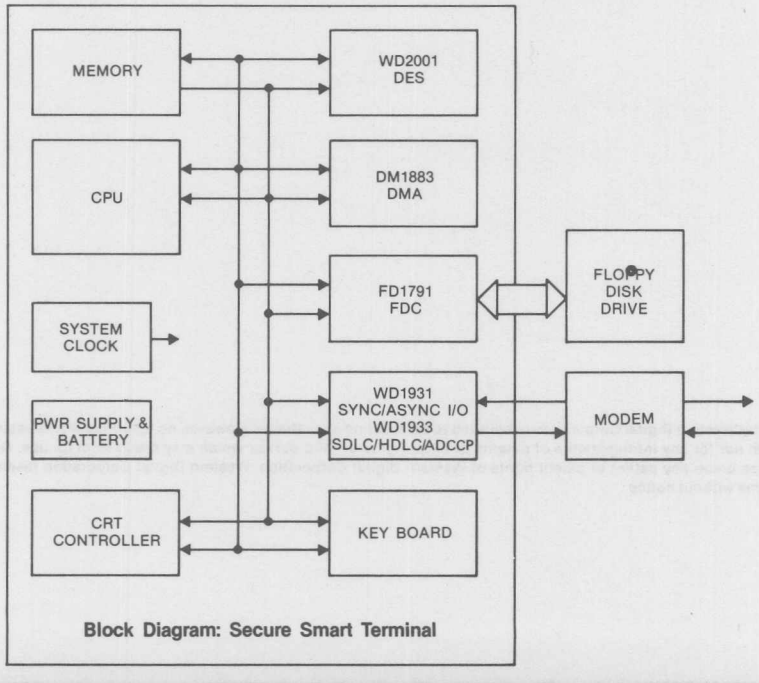
2. MASTER RESET PULSE WIDTH: 10 Clock Periods
3. Time between consecutive $\overline{RE}$ or $\overline{WE}$ pulses:
   $T_{BR} = T_{BW} = 2$ CLOCK PERIODS MINIMUM
4. ACT, $\overline{E}$/D, KEOE OUTPUTS
   These pins will be valid within 2 CLK↓ + 450 nsec from $\overline{WE}$ ↑ of a COMMAND REGISTER write operation.
5. $\overline{KPE}$ OUTPUT
   This pin will be active within 2 CLK ↓ + 450 nsec from $\overline{WE}$ ↑ of a write of a KEY WORD byte that results in a parity error.
6. $\overline{CRPS}$, $\overline{DPS}$, E/D INPUTS require a 300 ns set-up time.
7. The initial KR activation will be valid within 3 CLK ↓ + 450 nsec from $\overline{WE}$ ↑ of a write operation that programs a '1' into the COMMAND REGISTER ACTIVATE bit (or 2 CLK ↓ + 450 nsec from ACT input ↑, if $\overline{CRPS}$ = 0).
8. The initial DIR activation will be valid within 2 CLK ↓ + 450 nsec from $\overline{WE}$ ↑ of the 8th write into the KEY REGISTER.
9. The initial DOR activation will be valid within 49 CLK ↓ + 450 nsec from $\overline{WE}$ ↑ of the 8th write into the DATA REGISTER.
10. When reading the DATA REGISTER (in response to DOR), subsequent data bytes are made available internally to the DAL (CDP) output buffers within 2 CLK ↓ + 450 nsec from $\overline{RE}$ ↑

NOTE: All output timings assume C_{LOAD} = 50 PF

TYPICAL APPLICATION

Shown below is a block diagram for a floppy disk based DES secure smart terminal. The Direct Memory Access (DMA) controller optimizes data transfer operations for not only the floppy but also for file encryption and decryption operations. Secure features for the terminal include: secure file storage on floppy disks, optical clear/secure transmission via the communications I/O and battery backup of the Terminal ID key.

Tampering with the Terminal by unauthorized persons either through the key board power supply interrupt interlock or attempting to open the service panel results in memory scrambling and terminal ID key destruction. Finally, a hardware option was also included to allow the use of the pin compatible WD1933 device in place of the WD1931 for bit oriented SDLC, HDLC, or ADCCP protocols.



Block Diagram: Secure Smart Terminal

See page 429 for ordering information.

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WD2001/2 Applications Note
"One Bit Cipher Feedback In A Synchronous System"

INTRODUCTION

The WD2001/2 Data Encryption device interfaces easily to both microcomputer and hard-wired logic circuits. This Applications Note provides suggestions for the implementation of a synchronous circuit to perform system timing in a one bit cipher feedback application.

SYSTEM TIMING CONSIDERATIONS

The synchronous operation of a digital circuit often leads to both minimal hardware count and simple, easy to understand timing relationships. In addition, the concern over individual device characteristics become non-critical through the use of a worst case design approach. Common problems such as race conditions and temperature sensitivity can be virtually eliminated by synchronizing all logical events to a well defined clock edge.

WD2001/2 TIMING REQUIREMENTS

The WD2001/2 may be operated from a 2 MHZ clock. This provides a fundamental time period of 500 nSec that easily fits into the timing requirements for the device. For example, the minimum pulse width for a read (RD) or write (WR) pulse is 450 nSec.

Generation of the RD or WR pulse can be directly obtained from a synchronous device that transitions at each edge of the synchronous clock (SYNCLK). Figure 1 illustrates the timing relationship between SYNCLK and RD or WR.

Once the timing relationship is understood, the implementation becomes quite straightforward. The circuit of Figure 2 suggests a possible method of RD or WR generation.

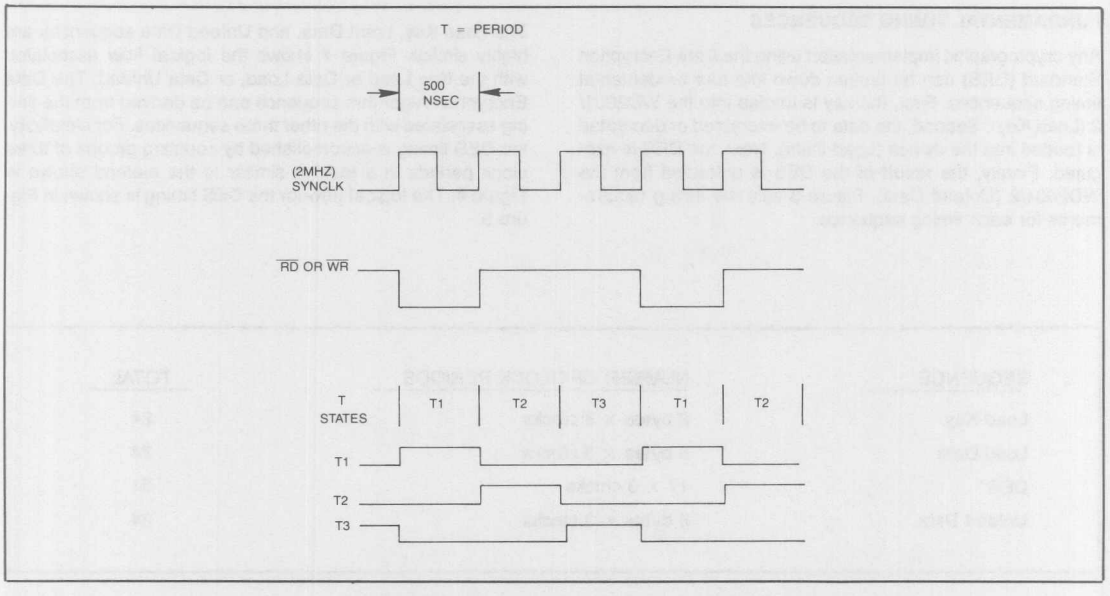
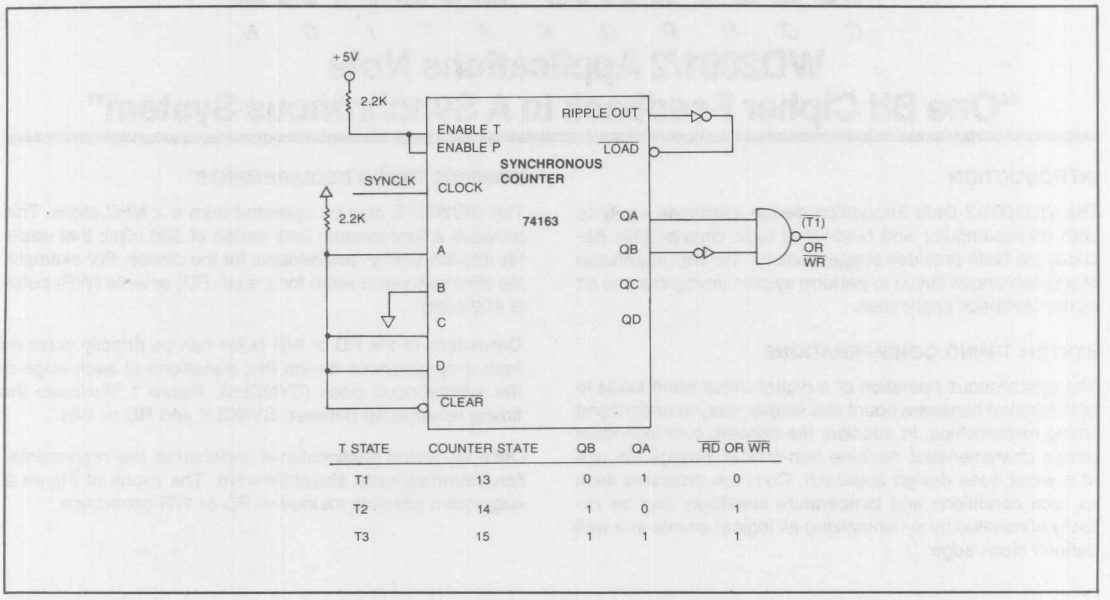


Figure 1 SYNCLK, RD, AND WR TIMING RELATIONSHIPS.



T STATE	COUNTER STATE	QB	QA	RD OR WR
T1	13	0	1	0
T2	14	1	0	1
T3	15	1	1	1

Figure 2 RD AND WR TIMING GENERATION

FUNDAMENTAL TIMING SEQUENCES

Any cryptographic implementation using the Data Encryption Standard (DES) can be broken down into four fundamental timing sequences. First, the key is loaded into the WD2001/2 (Load Key). Second, the data to be encrypted or decrypted is loaded into the device (Load Data). Next, the DES is executed. Finally, the result of the DES is unloaded from the WD2001/2 (Unload Data). Figure 3 lists the timing requirements for each timing sequence.

The Load Key, Load Data, and Unload Data sequences are highly similar. Figure 4 shows the logical flow associated with the Key Load or Data Load, or Data Unload. The Data Encryption Algorithm sequence can be derived from the timing associated with the other three sequences. For simplicity, the DES timing is accomplished by counting groups of three clock periods in a fashion similar to the method shown in Figure 4. The logical flow for the DES timing is shown in Figure 5.

SEQUENCE	NUMBER OF CLOCK PERIODS	TOTAL
Load Key	8 bytes × 3 clocks	24
Load Data	8 bytes × 3 clocks	24
DES	17 × 3 clocks	51
Unload Data	8 bytes × 3 clocks	24

Figure 3 FUNDAMENTAL TIMING SEQUENCES

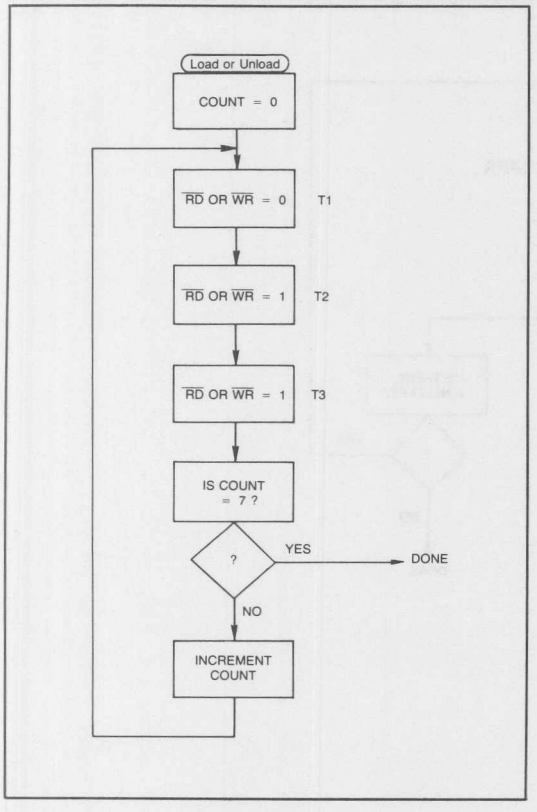


Figure 4 KEY LOAD, DATA LOAD, AND DATA UNLOAD FLOW

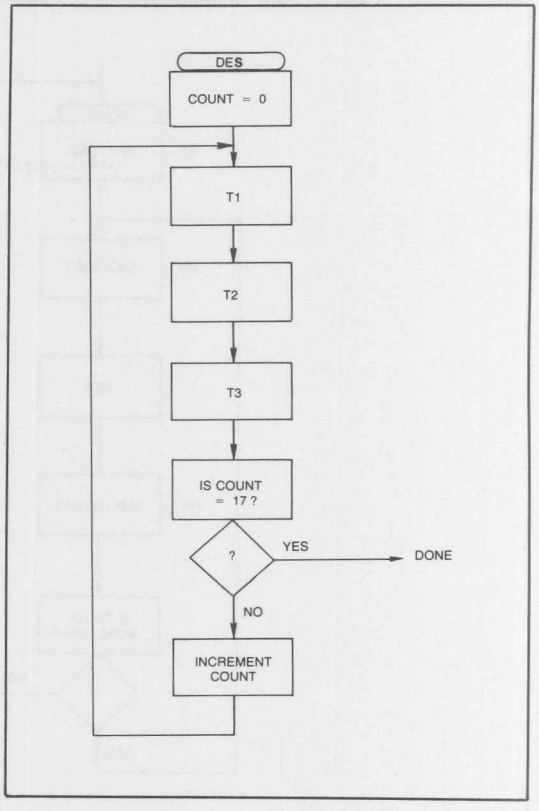


Figure 5 DES LOGICAL FLOW

SYSTEM TIMING OVERVIEW

The normal operation of a cryptographic system would require three classes of input/output (I/O) operations with the WD2001/2. First, the key is loaded (Key Load) through eight consecutive write cycles. Second, the data to be encrypted or decrypted is loaded (Load Data) in a similar fashion. After the Data Encryption standard is completed, the data is unloaded (Unload Data) through eight consecutive read cycles. Typically, the Key Load sequence would occur much less frequently than the Load Data or Unload Data sequences.

The flow diagram of Figure 6 shows the relationship between the four fundamental timing sequences defined previously, and also highlights the three I/O operations. Note that the Key Load sequence is outside of the tight loop.

Using the four fundamental timing sequences as logical building blocks, a functional block diagram of system timing can be designed. Figure 7 illustrates the overall system timing functions.

An implementation of the functions shown in Figure 7 is suggested in Figure 8. Note that all timing transitions are synchronous with the rising edge of SYNCLK.

Figure 9 details the timing of the Load Key sequence, and is similar to the Load Data, Unload Data, and DES sequences also.

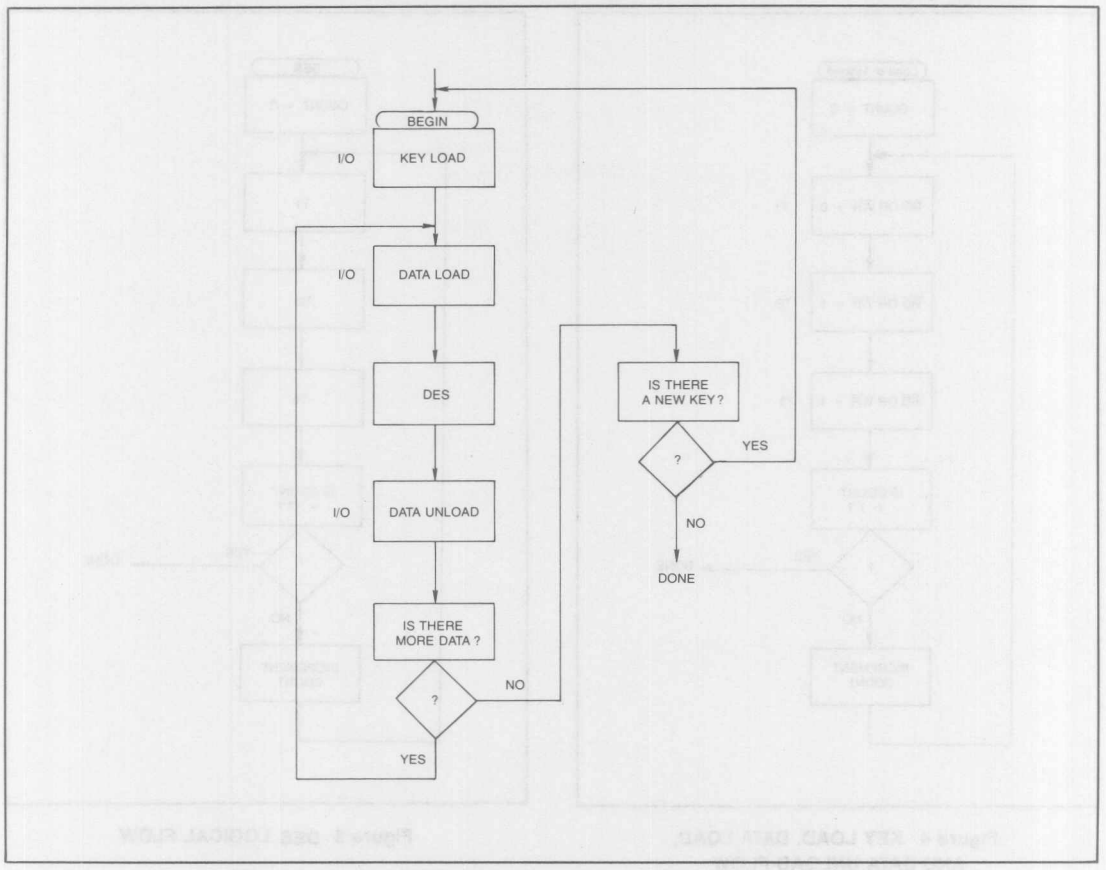


Figure 6 FUNDAMENTAL TIMING SEQUENCES INTERRELATIONS

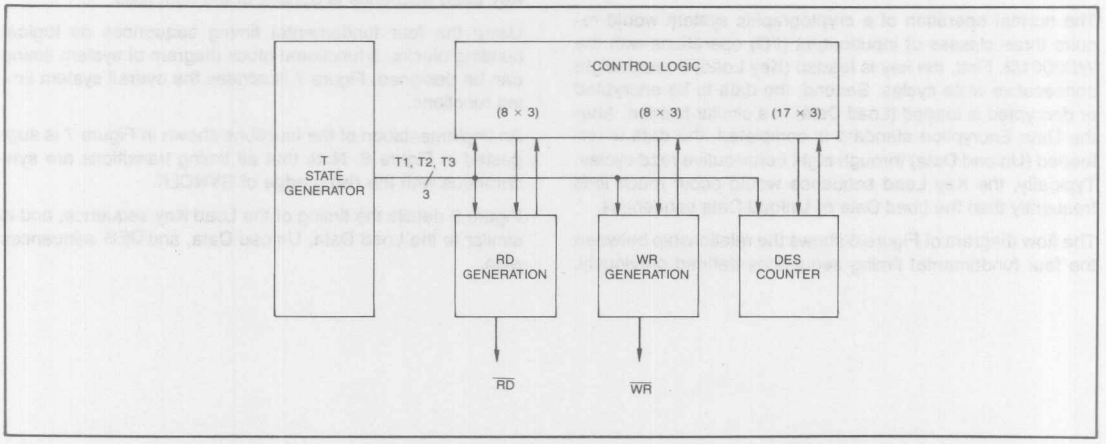
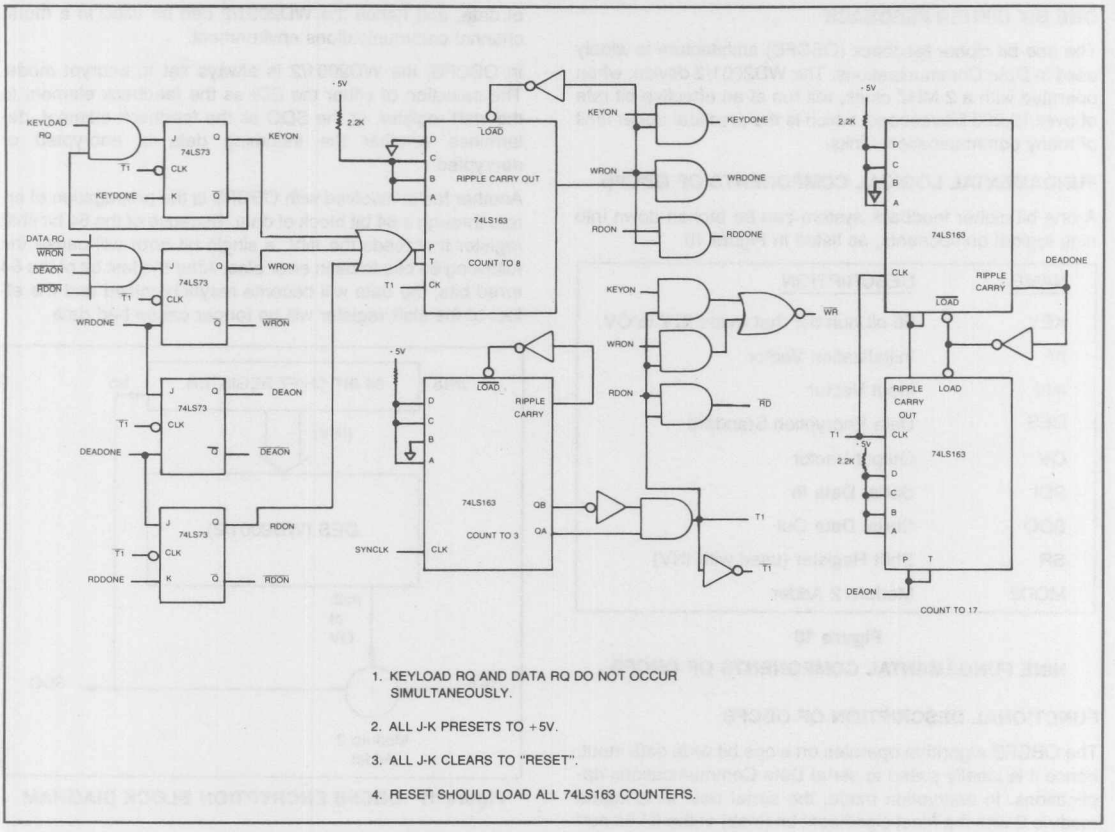


Figure 7 SYSTEM TIMING BLOCK DIAGRAM



1. KEYLOAD RQ AND DATA RQ DO NOT OCCUR SIMULTANEOUSLY.
2. ALL J-K PRESETS TO +5V.
3. ALL J-K CLEARS TO "RESET".
4. RESET SHOULD LOAD ALL 74LS163 COUNTERS.

Figure 8 SYSTEM TIMING IMPLEMENTATION

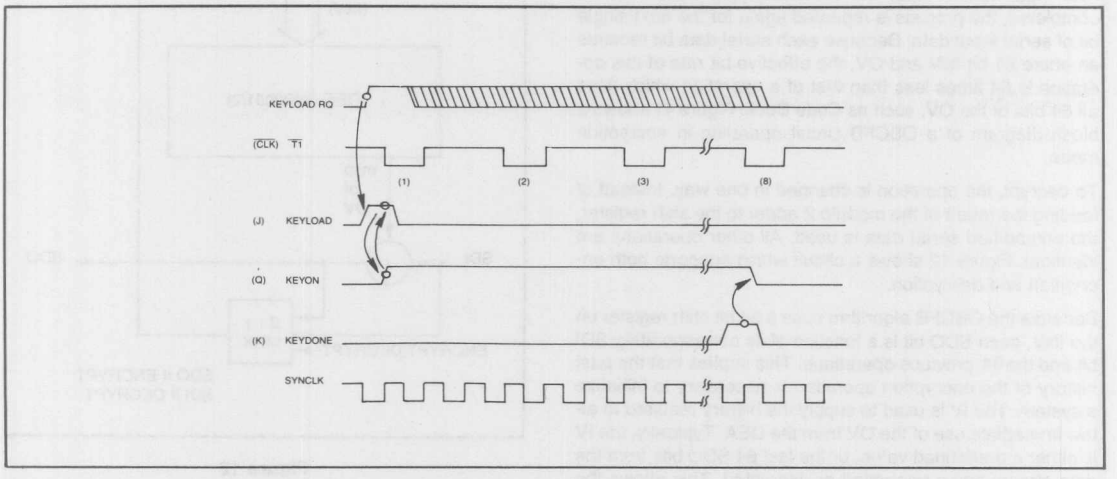


Figure 9 SINGLE KEYLOAD SEQUENCE

ONE BIT CIPHER FEEDBACK

The one bit cipher feedback (OBCFB) architecture is widely used in Data Communications. The WD2001/2 device, when operated with a 2 MHZ clock, will run at an effective bit rate of over 19,200 bits/second, which is the practical upper limit of many communications links.

FUNDAMENTAL LOGICAL COMPONENTS OF OBCFB

A one bit cipher feedback system can be broken down into nine logical components, as listed in Figure 10.

NAME	DESCRIPTION
KEY	56 bit number that maps INV to OV
IV	Initialization Vector
INV	Input Vector
DES	Data Encryption Standard
OV	Output Vector
SDI	Serial Data In
SDO	Serial Data Out
SR	Shift Register (used with INV)
MOD2	Modulo 2 Adder

Figure 10

NINE FUNDAMENTAL COMPONENTS OF OBCFB

FUNCTIONAL DESCRIPTION OF OBCFB

The OBCFB algorithm operates on a one bit wide data input, hence it is ideally suited to serial Data Communications applications. In encryption mode, the serial data in is added modulo 2 with the most significant bit (msb) of the 64 bit output vector. The result of this operation is then fed into the least significant bit (lsb) of a 64 bit shift register, and also is used as the serial data output. The shift register is then shifted from the lsb to the msb, and the result becomes the next input vector. After the Data Encryption Standard is completed, the process is repeated again for the next single bit of serial input data. Because each serial data bit requires an entire 64 bit INV and OV, the effective bit rate of this operation is 64 times less than that of a operation which uses all 64 bits of the OV, such as Code Book. Figure 11 shows a block diagram of a OBCFB circuit operating in encryption mode.

To decrypt, the operation is changed in one way. Instead of feeding the result of the modulo 2 adder to the shift register, the unmodified serial data is used. All other operations are identical. Figure 12 shows a circuit which supports both encryption and decryption.

Because the OBCFB algorithm uses a 64 bit shift register on the INV, each SDO bit is a function of its corresponding SDI bit and the 64 previous operations. This implies that the past history of the encryption operation is necessary to initialize a system. The IV is used to supply the history required to allow immediate use of the OV from the DEA. Typically, the IV is either a predefined value, or the last 64 SDO bits from the data stream being encrypted or decrypted. This allows the encryption process to be accomplished with discrete blocks of data, and hence the WD2001/2 can be used in a multichannel communications environment.

In OBCFB, the WD2001/2 is always set to encrypt mode. The selection of either the SDI as the feedback element to the shift register, or the SDO as the feedback element, determines whether the incoming data is encrypted or decrypted.

Another factor involved with OBCFB is the propagation of errors through a 64 bit block of data. Because of the 64 bit shift register that feeds the INV, a single bit error will cause the following 63 bits to be in error also. After the last bit of the 64 erred bits, the data will become resynchronized and the effect of the shift register will no longer cause bad data.

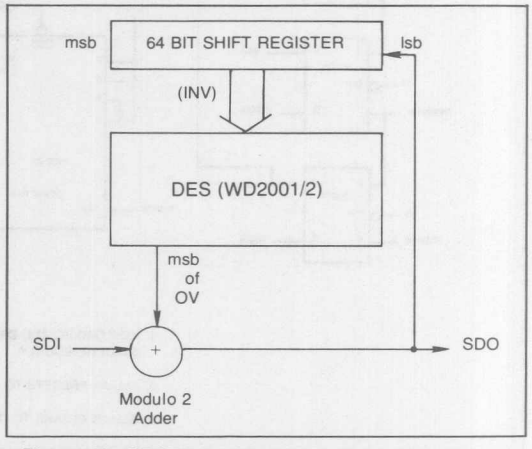


Figure 11 OBCFB ENCRYPTION BLOCK DIAGRAM

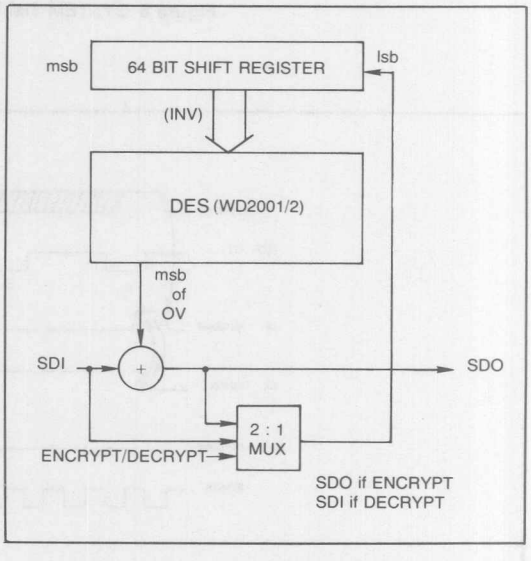


Figure 12

OBCFB ENCRYPTION/DECRYPTION BLOCK DIAGRAM

ONE BIT CIPHER FEEDBACK IMPLEMENTATION

Since the WD2001/2 is a byte input/output oriented device, the implementation of a OBCFB circuit can be accomplished without the 64 bit shift register shown in Figures 11 and 12. Through the use of a 9 bit wide FIFO, a "virtual" 64 bit shift register can be built. Figure 13 illustrates this with a Western Digital FR1502 FIFO and some common TTL logic.

Once the modulo 2 adder, the encrypt/decrypt selector, and the shift register are defined, the overall circuit can be generated by combining these pieces along with the logic shown in Figure 8. The overall block diagram of the one bit cipher feedback system is given in Figure 14.

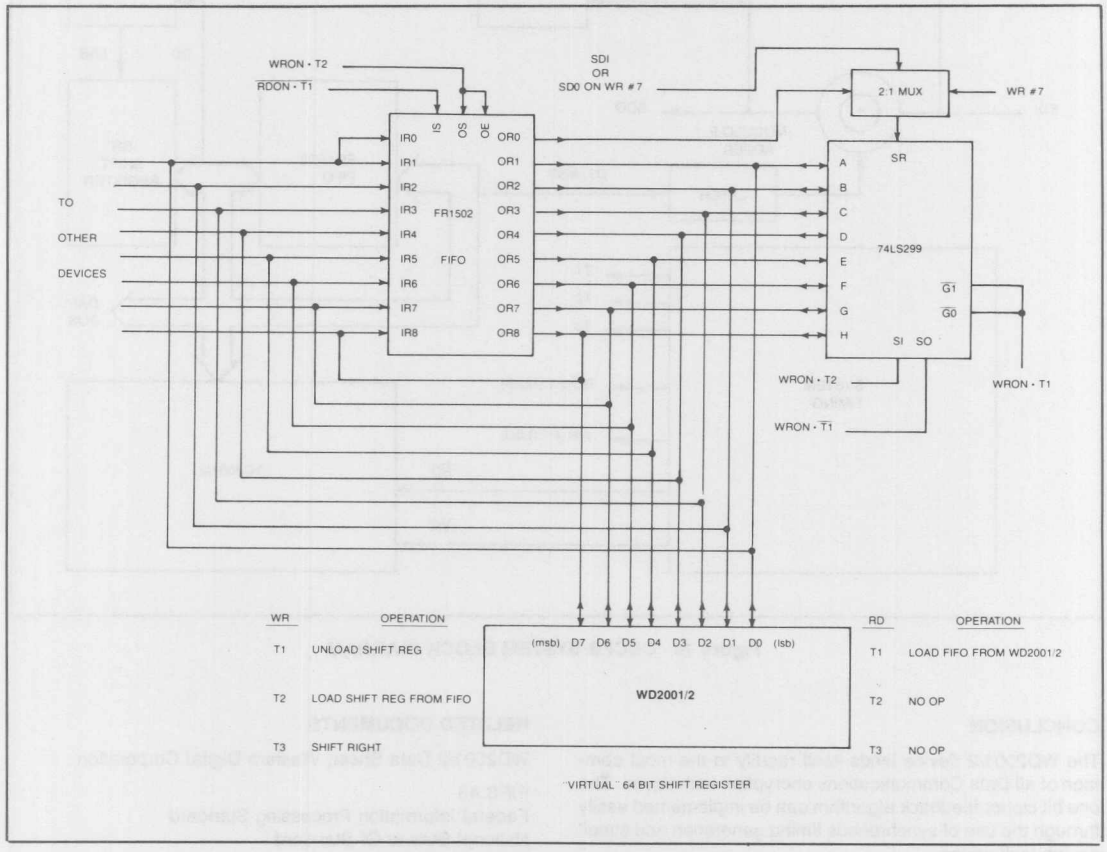


Figure 13 "VIRTUAL" 64 BIT SHIFT REGISTER

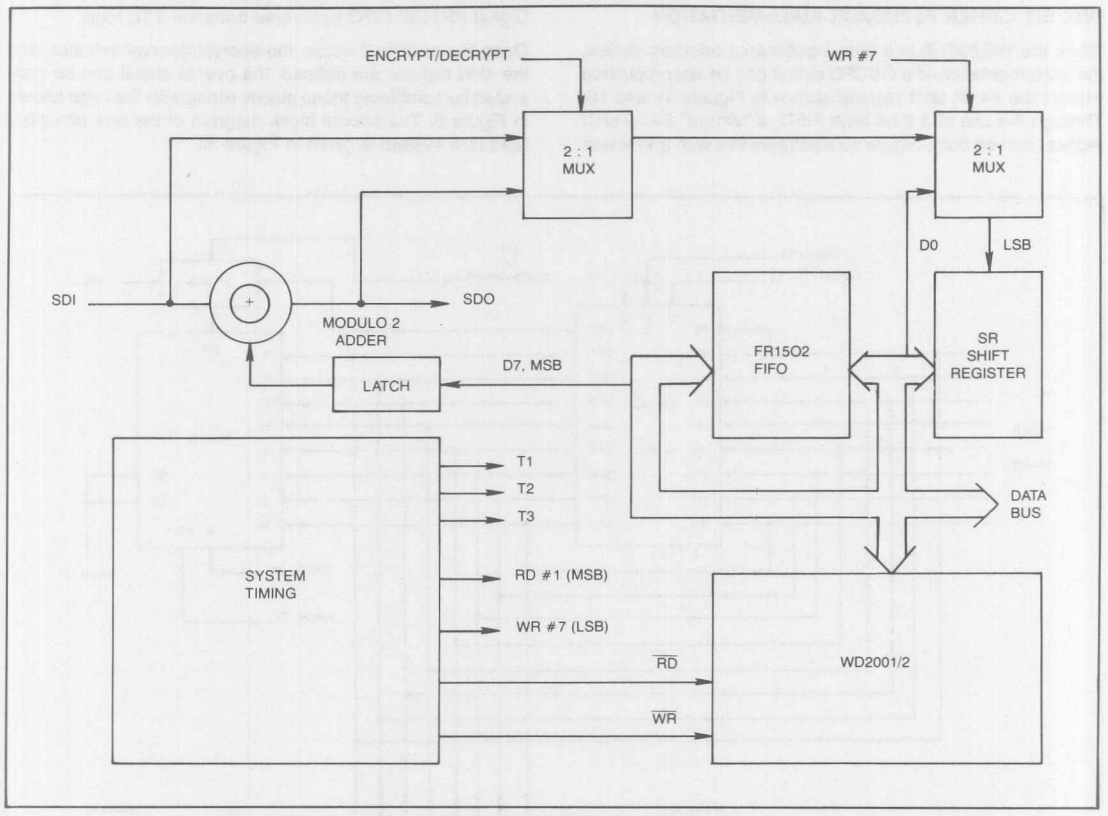


Figure 14 OBCFB SYSTEM BLOCK DIAGRAM

CONCLUSION

The WD2001/2 device lends itself readily to the most common of all Data Communications encryption techniques. The one bit cipher feedback algorithm can be implemented easily through the use of synchronous timing generation and circuit design techniques.

RELATED DOCUMENTS

WD2001/2 Data Sheet, Western Digital Corporation

FIPS 46
Federal Information Processing Standard
National Bureau Of Standard
Department of Commerce

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Cipher Feedback Cryptography Technical Note

CIPHER FEEDBACK CRYPTOGRAPHY

The United States Government in proposed Federal Standard 1026 describes three different approved ways of using the National Bureau of Standard's Data Encryption Standard (DES): Electronic Codebook; Cipher Feedback; and Cipher Block Chaining. Western Digital's WD2001 and WD2002, as delivered, implement the DES in Electronic Codebook Mode. This Technical Note will describe how to build an "N" bit Cipher Feedback (CFB) circuit using the WD2001.

WHAT IS CIPHER FEEDBACK?

Cipher feedback cryptography produces, as a function of previous cipher text, a pseudorandom bit stream which is added modulo 2 to the plain text to produce the next cipher text.

DES IN CIPHER FEEDBACK (CFB)

Obviously, both the receiver and transmitter must start their cryptographic operation with the same cryptographic keys to be able to acquire and maintain crytographic synchronization, i.e. produce the same pseudorandom bit stream at the same point in time.

For DES this means that both the 64 bit cryptographic variable (56 bit key) and the initial input to the algorithm must be identical at both ends. The initial input to DES in CFB is called the Initializing Vector (IV). Its format and generation are described in detail in Federal Standard 1026.

The functional description of using the WD2001 in CFB mode below assumes that communication synchronization has been achieved; that identical decrypted IV's and cryptographic keys are available to both the transmit and receive ends of the link; that encryption is to be a 1 bit cipher feedback; and that the plain text character size (1 in the example) equals the transmitted character size (Method A in proposed Federal Standard 1026).

ENCRYPTION

At time 0, the 64 bit cryptographic variable is loaded into the WD2001 with the key load sequence. A 64 bit block consisting of not more than 16 leading 0's and the 48 bit (or longer) IV is loaded into a 64 bit shift register (R) and into the input register, as if it were data, and encrypted. The WD2001 will automatically encrypt the IV under control of the cryptovariable and present a 64 bit block, 8 bits at a time as output. This output is stored in a shift register(S) with the most significant bit (MSB), to the left and the least significant bit on the right.

The MSB of S is added modulo 2 to the first bit of plain text to produce the first cipher bit. The contents of R are shifted 1 bit to the left and the just created cipher bit is inserted as the least significant bit (LSB) in R. The cipher bit is now available for buffering, transmission, etc.

The new contents of R are now loaded into the WD2001 as data, encrypted, and the new output placed in S.

The above procedure is repeated until the entire message text is encrypted, one bit at a time.

DECRYPTION

Decryption is accomplished in a similar manner: the IV is stored in R; loaded into the WD2001 as data; ENCRYPTED (even though the operation on the message text is to be decrypted); the results stored in S; and R shifted 1 bit to the left. Now, because the unit is receiving cipher rather than creating it, the first received bit is placed in the LSB of R. This cipher bit is also added, modulo 2, to the leftmost bit in S to reproduce the original plain text.

NOTES

Of particular significance is that the DES chip is in the ENCRYPT mode for CFB cryptography regardless whether the operation is to be performed to create cipher text or to recreate plain text. This is because the DES is being used to generate a pseudorandom bit stream. It is the exclusive OR operating on that bit stream and the received text which accomplishes the actual encryption/decryption of data.

S was nominally defined to be 64 bits long. It need be no longer than the number of text bits to be exclusive OR'd at one setting of the pseudorandom stream. In the example it was one bit. In reality it could be any character or block size from 1 to 64 bits long.

The convention used in this note is to organize a shift register with the MSB to the left. In practice, what is important is to use the MSB of S for the MOD 2 addition and to shift the R register content, so that the MSB is dropped and the cipher bit becomes the LSB. It is also important to perform the shift and generate a new pseudorandom block after each character has been encrypted or decrypted.

OTHER CIPHER FEEDBACK METHODS

Cipher Feedback can be done for any feedback size of 1 through 64 bits. One bit cipher feedback has the overall advantage of being transparent to the data being protected.

CHARACTERISTICS OF CFB

CFB has two properties which must be considered when selecting it for data encryption: 1) error extension and 2) self synchronization. Both of these properties exist because the encryption process synchronizes on the received cipher to produce the pseudorandom bit stream.

In the case of DES in one bit CFB, a one bit error in the received cipher message will affect the next 64 pseudorandom blocks—it will take 64 iterations to shift the one "bad" bit out of the 64 bit register above. If 8 bit CFB is used, then only 8 blocks will be affected, but that will still represent 64 bits used to decrypt incoming data.

In the same way, receiving 64 consecutive good bits of cipher will have filled the data-in register on the receiver end with the same 64 bits of data as in the transmit unit and proper decryption can again take place, assuming both ends have the same cryptographic key. This is what is meant by self-synchronizing.

APPLICATIONS OF CFB

In the data communications world error extension and self-synchronization are not important because of the excellent conditions of the lines and the protocols and error correcting codes used to insure proper receipt of data. In some applications, these properties of CFB cryptography can be turned to the user's benefit. This is especially true in situations where the data stream contains highly redundant information, where an incorrect recovery of 64 bits is hardly noticed—particularly when compared with the overall communications benefit of having the cryptography automatically resynchronize itself.

WD2001 CHARACTERISTICS IN CFB

The WD2001 is rated as having 1.304 megabits per second throughput when driven by a 2 MHZ clock. This figure is based on processing 64 bits of data at each operation. Using the WD2001 in an 8 bit cipher feedback circuit will reduce that to 163 kilobits per second. A 1 bit cipher feedback circuit would further reduce effective throughput to 20.385 kilobits per second. This is true of any DES implementation. The algorithm is designed to process 64 bits of plain (cipher) text at a time to produce 64 bits of cipher (plain) text; cipher feedback is designed to operate on a basic character size and shift after that character has been encrypted. In the 1 bit case, the user "throws away" 63/64ths throughput capacity for each encryption.

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PRELIMINARY

WD2412 Time of Day Clock

FEATURES

- SELF CONTAINED TIMEBASE USING COMMON BAUD RATE CRYSTAL
- SOFTWARE SELECTABLE EXTERNAL 50 AND 60 Hz TIMEBASES
- PROVIDES HOURS, MINUTES, SECONDS, DAY, MONTH, DATE, AND YEAR
- TIME OF DAY IS AVAILABLE IN 12 AND 24 HOUR BCD AND BINARY
- BINARY TIME IS INTERNALLY CALCULATED FROM BCD TIME
- INTERRUPT AT ABSOLUTE TIME OF DAY OR TIME AND DATE
- INTERRUPT AT RELATIVE TIME
- AUTO RELOAD FOR PERIODIC INTERRUPTS
- PERIODIC INTERRUPTS CAN BE SET FROM 0.1 SEC TO 1 DAY
- TIME, DATE AND INTERRUPT REGISTERS MAY BE READ ON THE FLY
- TIME, DATE OR USER CAN BE DISPLAYED ON 6 DIGIT BY 7 SEGMENT DISPLAY
- AM, PM, DATE, AND TIME DISPLAY MODE INDICATORS
- DISPLAYED TIME CAN BE IN 12 OR 24 HOUR FORMATS
- POWER FAIL FLAG
- INPUTS AND OUTPUTS ARE TTL/CMOS COMPATIBLE
- SINGLE +4.5 TO +6.3 VOLT SUPPLY
- 28 PIN CERAMIC OR PLASTIC PACKAGE
- TEMPERATURE RANGES: 0° TO +70°C, −40° TO +85°C

GENERAL DESCRIPTION

The WD2412 Time of Day clock (TDC) is a complete timekeeping system offering hours, minutes, seconds, day of week, month, date and year. Time of day is available in both 24 and 12 hour BCD and straight binary formats. The BCD calendar automatically corrects for leap years up to the year 2100. The WD2412 can be programmed to provide relative or absolute real time interrupts with resolutions to a tenth of a second. Absolute interrupts can be based on time or time and date. The relative interrupt down counter can be read on the fly and reloads itself after an interrupt. 12 or 24 hour time of day, date, or user registers can be output to an external 6 digit by 7 segment display. Also TIME, DATE, AM and PM status indicators are provided. A flag is available to inform the host system that a catastrophic power failure has occurred. The WD2412 includes an 8 bit bi-directional bus so that it may be easily interfaced to most popular microcomputers. It is fabricated on a single NMOS LSI chip including all bus interface logic and crystal timebase oscillators. All inputs and outputs are TTL compatible.

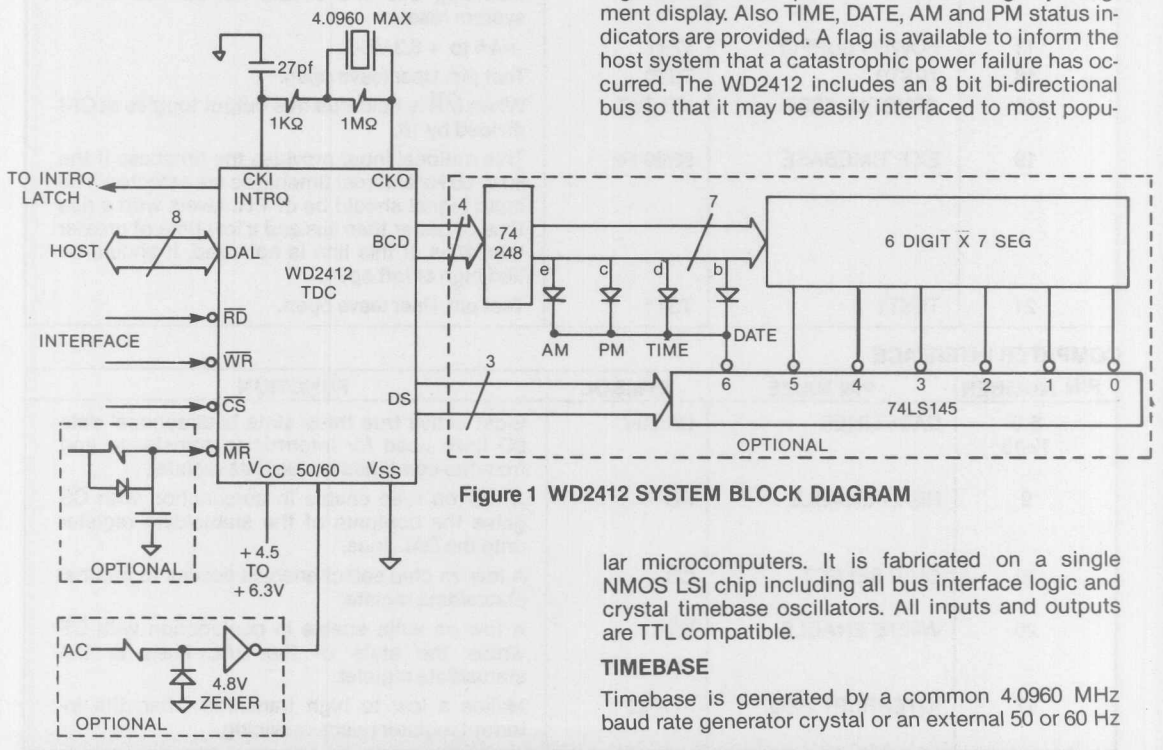


Figure 1 WD2412 SYSTEM BLOCK DIAGRAM

TIMEBASE

Timebase is generated by a common 4.0960 MHz baud rate generator crystal or an external 50 or 60 Hz

signal. On power up, the timebase defaults to the internal crystal, but a software command can be issued to the WD2412 to change its timebase over to 50 or 60 Hz or back to crystal again. Due to the fact that the 50/60 Hz timebase is not synchronized to the crystal oscillator, there may be a slight timebase error incurred when switching from internal to external timebases or back again. This timebase error is guaranteed not to exceed 0.1 second per timebase switch. When operating the WD2412 from an external timebase, it is not necessary to provide a crystal oscillator. Internal timing needs of the WD2412 can be satisfied by injecting a 4 MHz TTL level signal into the CKI terminal.

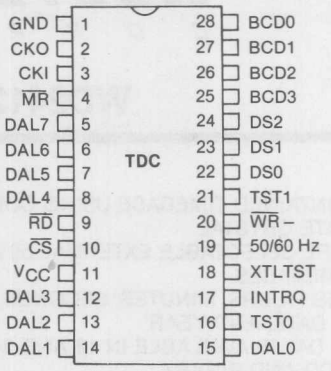


Figure 2

PIN DESIGNATION

PIN DESIGNATIONS

PIN NUMBER	PIN NAME	SYMBOL	FUNCTION
1	POWER SUPPLY	V_{DD}	Ground
2	CLOCK OUT	CKO	Crystal oscillator output.
3	CLOCK IN	CKI	Crystal oscillator input.
4	MASTER RESET	MR	A logic low on this input clears all internal logic after power up. If rise time of power supply is less than 1 mS, then the external RC is optional. Normally, this line should not be tied to the system reset.
11	POWER SUPPLY	V_{CC}	+4.5 to +6.3 VDC
16	TEST0	TST0	Test pin. User leave open.
18	CRYSTAL TEST	XTLTST	When $\overline{MR}$ is held true this output toggles at CKI divided by 16.
19	EXT. TIMEBASE	50/60 Hz	This optional input provides the timebase if the 50 or 60 Hz external timebases are selected. The input signal should be of TTL levels with a rise time of better than 1μs and a low time of greater than 20μs. If this line is not used, it should be tied high or left open.
21	TEST1	TST1	Test pin. User leave open.

COMPUTER INTERFACE

PIN NUMBER	PIN NAME	SYMBOL	FUNCTION
5-8 12-15	DATA LINES	DAL 0-7	Eight active true three state bi-directional data I/O lines used for information transfer to and from the combined status/data register.
9	READ ENABLE	$\overline{RD}$	A low on read enable in conjunction with $\overline{CS}$ gates the contents of the status/data register onto the DAL lines.
10	CHIP SELECT	$\overline{CS}$	A low on chip select enables access to internal status/data register.
20	WRITE ENABLE	$\overline{WR}$	A low on write enable in conjunction with $\overline{CS}$ writes the state of the DAL lines to the status/data register.
17	INTERRUPT REQ.	INTRQ	Makes a low to high transition when the interrupt register needs servicing.

OPTIONAL DISPLAY INTERFACE

PIN NUMBER	PIN NAME	SYMBOL	FUNCTION
22-24	DIGIT SELECT	DS 0-2	Digit select for multiplexed display.
25-28	BCD OUT	BCD 0-3	BCD data for multiplexed display.

COMMAND DESCRIPTION

The WD2412 will accept and execute 24 commands. Command words should only be loaded onto the status/data register when the command ready status word appears on the status/data register. The command ready byte is EEH. Whenever a data transfer takes place, the receiving device (either the TDC or the host) must acknowledge the transfer by sending a FFH. For ease of discussion, commands are divided into three types.

Type I Commands

Type I commands set internal flags and operating modes. They are all considered completed after transfer of the command.

E0H DISPLAY OFF
E1H DISPLAY 12 HOUR TIME
E2H DISPLAY 24 HOUR TIME
E3H DISPLAY DATE
E4H DISPLAY USER
E5H SELECT CRYSTAL TIMEBASE
E6H SELECT EXTERNAL 50 Hz TIMEBASE
E7H SELECT EXTERNAL 60 Hz TIMEBASE
E8H DISABLE INTERRUPTS

COMPUTER DIALOG WITH TDC FOR TYPE I COMMANDS

STATUS 1	COMPUTER	←	TDC
if TDC ready:			
COMMAND	COMPUTER	→	TDC

Type II Commands

Type II commands set internal registers. They are all followed by three bytes of data. They are considered completed after transfer of data. All type II commands are non interruptable.

The commands are:

E9H SET 12 HOUR BCD TIME (BIN and BCD24 also set)
EAH SET 24 HOUR BCD TIME (BIN and BCD12 also set)
EBH SET DATE
ECH SET DAY OF WEEK
EDH SET USER
EFH SET ABSOLUTE 12 HOUR TIME INT (Interrupts are enabled)
F0H SET ABSOLUTE 24 HOUR TIME INT (Interrupts are enabled)
F1H SET ABSOLUTE DATE INTERRUPT (Interrupts are enabled)
F2H SET RELATIVE INTERRUPT (Interrupts are enabled)

COMPUTER DIALOG WITH TDC FOR TYPE II COMMANDS

STATUS 1	COMPUTER	←	TDC
if TDC ready:			
COMMAND	COMPUTER	→	TDC
STATUS 2	COMPUTER	←	TDC
if TDC ready:			
BYTE 1	COMPUTER	→	TDC
STATUS 2	COMPUTER	←	TDC
if TDC ready:			
BYTE 2	COMPUTER	→	TDC
STATUS 2	COMPUTER	←	TDC
if TDC ready:			
BYTE 3	COMPUTER	→	TDC

Type III Commands

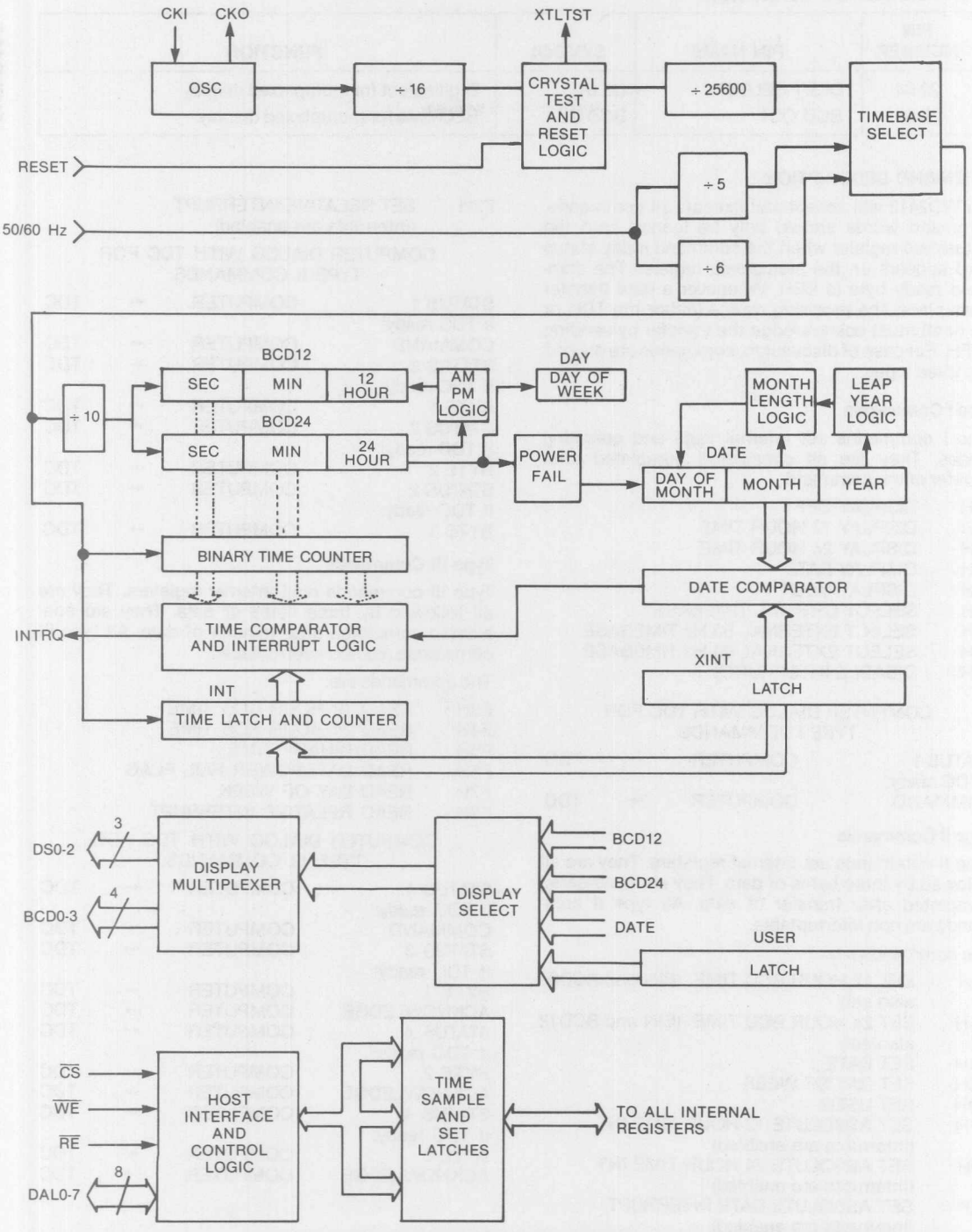
Type III commands read internal registers. They are all followed by three bytes of data. They are considered completed after transfer of data. All type III commands are non interruptable.

The commands are:

F3H READ 12 HOUR BCD TIME
F4H READ 24 HOUR BCD TIME
F5H READ BINARY TIME
F6H READ DATE/POWER FAIL FLAG
F7H READ DAY OF WEEK
F8H READ RELATIVE INTERRUPT

COMPUTER DIALOG WITH TDC FOR TYPE III COMMANDS

STATUS 1	COMPUTER	←	TDC
if TDC ready:			
COMMAND	COMPUTER	→	TDC
STATUS 3	COMPUTER	←	TDC
if TDC ready:			
BYTE 1	COMPUTER	←	TDC
ACKNOWLEDGE	COMPUTER	→	TDC
STATUS 4	COMPUTER	←	TDC
if TDC ready:			
BYTE 2	COMPUTER	←	TDC
ACKNOWLEDGE	COMPUTER	→	TDC
STATUS 4	COMPUTER	←	TDC
if TDC ready:			
BYTE 3	COMPUTER	←	TDC
ACKNOWLEDGE	COMPUTER	→	TDC



WD2412 FUNCTIONAL BLOCK DIAGRAM

Master Reset

Upon receipt of a Master Reset, the WD2412 defaults to the following values:

BCD24	00:00:00 (Midnight)
BCD12	12:00:00 AM
BIN	0
DATE	00/00/00
DAY	0 (Sunday)
RELATIVE INT	0
TIMEBASE	Crystal
DISPLAY	Off
INTERRUPTS	Disabled
POWER FAIL FLAG	Set

Power Fail Flag

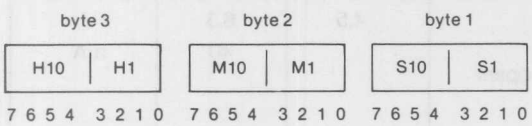
When power is restored to the WD2412, it initiates a master reset. As part of this, the Power Fail Flag is set. Normally, at the end of a day, the DAY and DATE registers are incremented. When the Power Fail Flag is set, the DATE register remains at 00/00/00 to indicate that the power failed although the DAY register is still incremented. Elapsed time since WD2412 power up can be determined by reading any time of day register in conjunction with the DAY register.

ORGANIZATION

The WD2412 includes eight 3-byte user addressable registers. These registers are 12 hour BCD Time of Day (BCD12), 24 hour BCD Time of Day (BCD24) Binary Time of Day (BIN), Date (DATE), Day (DAY), User (USR), Time of Day Absolute and relative interrupt register (INT) are extended (Date Absolute) interrupted register (XINT).

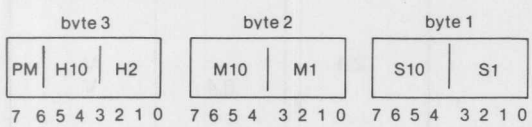
BCD24 Register

This read/write register holds the present time of day in a 24 hour BCD format. Data are arranged in a packed BCD format with two digits per byte.



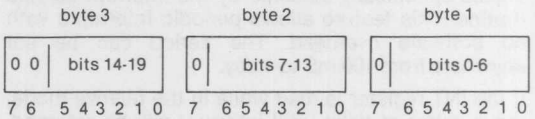
BCD12 Register

This read/write register holds the present time of day in a 12 hour BCD format. Data are arranged in a packed BCD format with two digits per byte. An AM/PM indicator is available on the most significant bit of the most significant byte. This bit is reset for AM and set for PM.



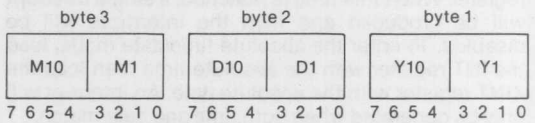
Bin Register

This read only register also holds the present time of day, but in a straight binary format. The format is in one-tenth second ticks since midnight. The value of this 20 bit register can vary from 0 through 863,999 decimal. Data is arranged in a seven bit per byte format with the most significant bit of the byte always set to zero.



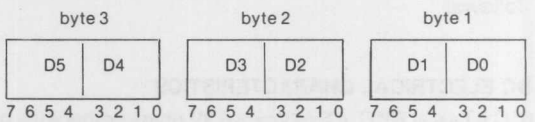
Date Register

This read/write register holds the present date in a BCD format. Again, data is arranged in a packed BCD format with two digits per byte.



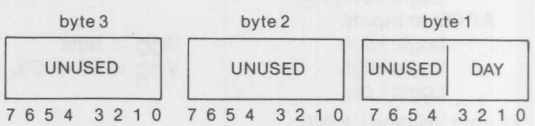
User Display Register

This write only register is used for user programmable outputs to the optional six digit display. Valid characters are 0-9 and blank. Blanks are entered as 10's.



Day Register

This read/write register holds the day of the week as a binary integer ranging in value from 0 to 6. Sunday is usually considered 0, but this is a completely arbitrary designation. For software simplicity, set day and read day are standard Type II and Type III commands respectively. On set day, the unused fields can be set to anything that won't interfere with the command protocol. On read day, the unused fields are zeroed.



INT and XINT Registers

These registers have three modes, depending on how they are set. In the relative mode, a binary countdown value is loaded into the INT register and an interrupt is generated when this value is decremented to zero. When the terminal value is reached, the register is automatically re-loaded, unless specifically disabled by the interrupt service routine. This feature allows periodic interrupts with no software overhead. The period can be set anywhere from 100 mS to 1 day.

If the INT register is read while in the relative mode, the number of ticks until interrupt will be returned. The data pattern is in the same format as in the BIN register.

In the absolute time mode, a time of day in the same format as the BCD24 register is loaded into the INT register. When this time is matched, a single interrupt will be produced and then the interrupts will be disabled. To enter the absolute time/date mode, load the INT register with the absolute time then load the XINT register with the absolute date. An interrupt will only be generated when both time and date match.

OPTIONAL DISPLAY

The WD2412 can interface to a seven segment by six digit display and four status indicators. 12 or 24 hour time, date, or user defined numeric message can be displayed. Four status indicators are provided as follows:

NAME	SEG	DESCRIPTION
AM	e	Lit only when displaying 12 hour time
PM	c	Lit only when displaying 12 hour time
TIME	d	Lit when displaying 12 or 24 hour time
DATE	b	Lit when displaying date

ABSOLUTE MAXIMUM RATINGS

Voltage at Any Pin Relative to GND. . . -0.5V to $+7$V
Ambient Operating Temperature
(Note 1) . . . . . 0°C to +70°C
Ambient Storage Temperature
Ceramic . . . . . -65°C to $+150$°C
Plastic. . . . . -55°C to $+125$°C
Lead Temperature (Soldering, 10 sec.) . . . . . 300°C
Power Dissipation . . . . . 0.75 Watt at 25°C
0.4 Watt at 70°C

Absolute maximum ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications are not ensured when operating the device at absolute maximum ratings.

NOTE 1: An extended temperature range WD2412 is available which will operate within an ambient temperature range of -40°C to $+85$°C.

DC ELECTRICAL CHARACTERISTICS

$0°C \leq T_A \leq +70°C$, $4.5V \leq V_{CC} \leq 6.3V$ unless otherwise noted.

PARAMETER	CONDITIONS	MIN	MAX	UNITS
Operating Voltage (V_{CC})		4.5	6.3	V
Operating Supply Current	V_{CC} = 5V, T_A = 25°C (all inputs and outputs open)		40	mA
Input Voltage Levels				
CKI Input Levels				
Crystal Input				
Logic High (V_{IH})		2.0		V
Logic Low (V_{IL})			0.4	V
All Other Inputs				
Logic High	V_{CC} = Max	3.0		V
Logic High	V_{CC} = 5V ± 5%	2.0		V
Logic Low			0.8	V
Output Voltage Levels				
Standard Output				
TTL Operation	V_{CC} = 5V ± 5%			
Logic High (V_{OH})	I_{OH} = 100 μA)	2.4		V
Logic Low (V_{OL})	I_{OL} = -1.6 mA		0.4	V
THREE-STATE Output Leakage Current		-10	+10	μA

AC ELECTRICAL CHARACTERISTICS

PARAMETER	CONDITIONS	MIN/MAX	UNITS
Read Operation (Figure 4)			
Chip Select Stable Before RD — t_{CSR}	C_L = 50pf; V_{CC} = 5V ± 5%	50 min	ns
Chip Select Hold Time for RD — t_{RCS}		5 min	ns
RD Pulse Width — t_{RR}		300 min	ns
Data Delay from RD — t_{RD}		250 max	ns
RD to Data Floating — t_{DF}		200 max	ns
Write Operation (Figure 3)			
Chip Select Stable Before WR — t_{CSW}		20 min	ns
Chip Select Hold Time for WR — t_{WCS}		20 min	ns
WR Pulse Width — t_{WW}		300 min	ns
Data Set-Up Time for WR — t_{DW}		200 min	ns
Data Hold Time for WR — t_{WD}		40 min	ns

Figure 5 INPUT/OUTPUT TIMING DIAGRAM (CRYSTAL ÷ 16)

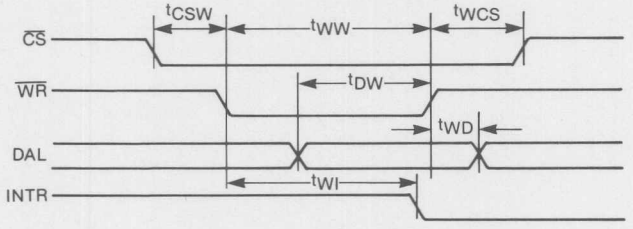


Figure 3 WRITE OPERATION TIMING

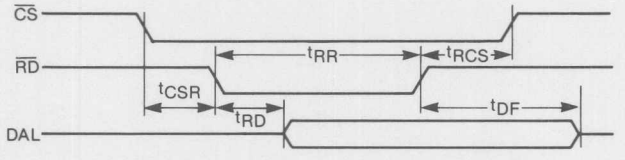


Figure 4 READ OPERATION TIMING

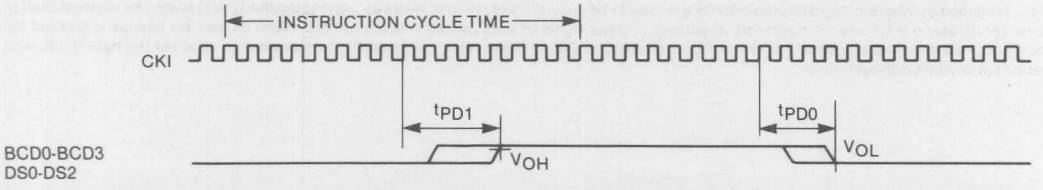


Figure 5 INPUT/OUTPUT TIMING DIAGRAM (CRYSTAL ÷ 16)

See page 429 for ordering information.

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WD2412 Time of Day Clock Application Guide

USES FOR TDC CHIP

The WD2412 is designed for computer applications that require an easy to use, bus oriented time of day clock. Some of the WD2412 more obvious applications are:

- Real Time Data Collection (Data Loggers)
- Point of Sale (Cash Registers, Store Traffic Monitoring)
- Automatic Teller (Time and Date of Transaction)
- Small Business Computer (Payroll, Transaction Dating)
- Word Processing (Automatic Dating of Form Letters)
- Data Entry (Form Fill-In)
- Taxi Meter
- Flight Recorder
- Large Scale Heating and Cooling Control and Scheduling
- Demand Billing (Electric Company Meters)
- Postal Meters
- Traffic Signals
- Home Computers
- Computerized Instruments
- Process Control

OPTIONAL DISPLAY

To minimize the time it takes to execute commands, the display will be shut off momentarily during the execution of commands. This is to allow the internal microsequencer high priority access to the internal registers. Normally no display degradation will be experienced even during command execution.

ILLEGAL ACCESS LOCKOUT

To insure that the time or date do not inadvertantly get set during host system power outages or system crashes, the WD2412 features Illegal Access Lockout. In order to issue any command to the WD2412, the proper protocol must be observed. All Type II instructions (writes to WD2412) use a holding latch for the parameters sent to the WD2412. The contents of the holding latch will not be transferred to any internal register unless the entire three byte transfer occured without error.

BUS TIMER

If the host system is turned off while any data or command transfer to the WD2412 is taking place, the WD2412 may be left waiting for a data transfer acknowledge forever. The host may also be waiting for the command ready byte. To break this deadlock, the WD2412 includes a bus timer. If the next step in the data transfer protocol does not occur within approximately one second, the WD2412 will switch to a command ready state by writing the command ready byte (EEH) to the I/O port.

INTERRUPTS

The WD2412 includes an INTerrupt ReQuest (INTRQ) line that generates an 8 μS pulse for each interrupt. Normally the low to high transition of the INTRQ line will have to be latched by an external D-type latch. The method of acknowledging the interrupt is left up to the system designer.

The WD2412 has four mutually exclusive interrupt modes. They are recurring, relative, time absolute, and time/date absolute.

Recurring Interrupts

To generate recurring interrupts, load the INT register using the Set Relative Interrupt command. The parameter loaded into the INT register should be the number of 0.1 second ticks minus one until interrupt. The period of interrupts can be varied from 0.1 second (0) to 1 day (863,999 decimal). After an interrupt has been received, the INT register is automatically re-loaded and the count down continues. To stop recurring interrupts issue a Disable Interrupts command.

The contents of the INT countdown register may be examined at any time using the Read Relative Interrupt command. The number in this register is equal to the number of ticks until interrupt plus one.

Relative Interrupts

This mode is a variation of Recurring Interrupts. To generate a time relative interrupt, load the INT register using the Set Relative Interrupt command. After an interrupt has been received, the user should execute a Disable Interrupt command to supress further interrupts. The INT register may be read using the Read Relative Interrupt command.

Time Absolute Interrupt

This mode interrupts at an absolute time match, much like an alarm clock. To enable this interrupt, set the time to interrupt using the Set Absolute 12 Hour Time Interrupt command or the Set Absolute 24 Hour Time command. After the interrupt is produced, interrupts are disabled.

Time/Date Absolute Interrupt

This mode interrupts at an absolute time and date match. To enable this interrupt, set the absolute time interrupt in the normal manner then issue a Set Absolute Date command. After the interrupt is produced, interrupts are disabled.

MASTER RESET

In most applications the circuit on the Master Reset line (MR-) is not optional. The internal reset is based on a special circuit that charges up a small capacitor and then dumps its charge into a larger capacitor. The rate in which the small capacitor is charged and dumped is determined by the clock on the CKI line. This 'charge nibbler' circuit is dependent on the rise time of the clock power supply.

If the power supply rise time is between 1 μS and 1 mS, then the internal circuit may be used. Otherwise construct a RC circuit that will keep the MR- line below 0.7 times the power supply voltage (typically 3.5 V) for at least 15 μS after the power supply has stabilized.

TIMEBASES

The WD2412 has two distinct types of timebases. It allows the use of the 4.096 Mhz internal crystal oscillator (using an external crystal) or an external 50 or 60 Hz timebase. The low time for the 50/60 Hz timebase must be 15 μS or longer.

The crystal oscillator is good for applications that do not have access to the 50/60 Hz line frequency. Its primary advantage is power line independence. Its primary disadvantage is a relatively poor long term stability. The crystal is the default timebase.

The 50/60 Hz timebase option is ideal for applications that have access to the 50/60 line frequency on a continual basis. Typically, the long term stability of the 50/60 Hz line is on the order of about a second or two per year.

A small keep alive power supply can be constructed to run the WD2412 and the schmitt trigger waveform shaper. An easy way to skirt UL approval would be to use a miniature plug type power supply putting out low voltage AC. At the clock board the power can be rectified and filtered for the WD2412 and the 50/60 Hz can be run though a resistor-zener network and then into a schmitt trigger.

SAMPLE ASSEMBLY LANGUAGE DRIVER

One of the advantages of the WD2412 is it's simple software interface. There is only one combined I/O port so port indexing schemes are not needed. All commands are grouped into only three types so all software drivers can be written to be very general purpose. In these following 8080 assembly language examples, function number is carried in the B register. The time or date to be read or written is located in a string of three bytes indexed by the HL register pair.

```
;Type I command for the Western Digital WD2412
;Command is located in register B
CLOCK EQU  64H        ;Port address of WD2412
TYPE1:
WAIT1: IN   CLOCK      ;Is clock ready to
       CPI  OEEH       ;accept a command?
       JNZ  WAIT1      ;Not ready; keep looping . . .
       MOV  A,B        ;If ready, get command
       OUT  CLOCK      ;and output it to clock.
       RET             ;Done. That wasn't too
                       hard!
```

```
;Type II command for the Western Digital WD2412
;Command is located in register B
;Register pair HL indexes string to set TDC
;(Write 3 bytes)
TYPE2: CALL TYPE1      ;Issue command.
       CALL WAIT2      ;Write first byte.
       CALL WAIT2      ;Write second byte.
WAIT2: IN   CLOCK      ;Write third byte.
       INR  A          ;Is status ready? (FFH)
       JNZ  WAIT2      ;No, jump and wait.
       MOV  A,M        ;Otherwise get a byte from
                       memory
       OUT  CLOCK      ;and output it to clock.
       INX  H          ;Index next memory
                       location.
       RET
```

```
;Type III command for the Western Digital WD2412
;Command is located in register B
;Register pair HL indexes string to read TDC
;(Read 3 bytes)
TYPE3: CALL TYPE1      ;Issue command.
WAIT3: IN   CLOCK      ;Check to see if TDC
       CMP  B          ;accepted command.
       JZ   WAIT3      ;Loop if command still
                       latched.
       CALL INACK      ;Read first byte (status
                       already checked).
       CALL WAIT4      ;Read second byte.
WAIT4: IN   CLOCK      ;Read third byte.
       INR  A          ;Is status ready? (FFH)
       JZ   WAIT4      ;No, keep on looping.
INACK: IN   CLOCK      ;Otherwise read clock data.
       MOV  M,A        ;Store it in memory.
       MVI  A,OFFH     ;Issue acknowledge flag
       OUT  CLOCK      ;to clock.
       INX  H          ;Increment memory pointer.
       RET
```

SAMPLE MICROSOFT BASIC DRIVER

The following Basic subroutines can be used to set or read the clock. Commands are passed in variable C. A three element array, T, holds the set or read data vector.

```
 10    REM Type I command
 20    P = 100:REM port number
 30    IF INP(P)<>238 THEN 30
 40    OUT P,C
 50    RETURN
 60    REM Type II command
 70    GOSUB 20
 80    FOR X = 0 TO 2
 90    IF INP(P)<>255 THEN 90
100    OUT P,T(X)
110    NEXT
120    RETURN
130    REM Type III command
140    GOSUB 20
150    IF INP(P) = C THEN 150
160    X = 0
170    GOSUB 230
180    FOR X = 1 TO 2
190    IF INP(C) = 255 THEN 190
200    GOSUB 230
210    NEXT
220    RETURN
230    T(X) = INP(C)
240    OUT C,255
250    RETURN
```

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CORPORATION

FR1502 First-In/First-Out Buffer Register

FEATURES

- 40 CHARACTERS BY 9 BITS
- EXPANDABLE CHARACTER AND BIT SIZE (CASCADE CAPABILITY)
- DC TO 1 MHz ASYNCHRONOUS I/O ACCESS
- INPUT/OUTPUT READY STATUS FLAGS
- THREE STATE OUTPUTS
- SEPARATE INPUT AND OUTPUT ENABLES
- DIRECTLY TTL AND DTL COMPATIBLE
- MASTER RESET
- NO EXTERNAL CLOCKS REQUIRED
- AVAILABLE IN REL-PAC (F) OR CERAMIC (E) PACKAGES

APPLICATIONS

POINT OF SALE TERMINALS

DATA TRANSMISSION BUFFER

LINE PRINTER INPUT BUFFER

KEY-TO-TAPE/KEY-TO-DISC EQUIPMENT

CARD/TAPE READERS

AUTO DIALERS

CRT BUFFER MEMORY

CONTROL STACK SILO ORIENTED MACHINES

COMPUTER/TERMINALS I/O INTERFACE BUFFER

TELEPRINTER BUFFER

GENERAL DESCRIPTION

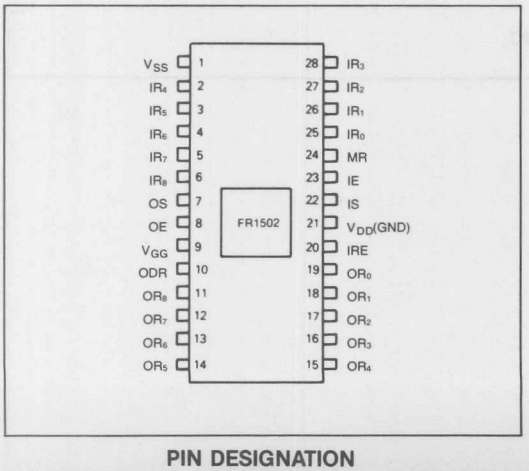
The FIFO (First-In/First-Out) Storage Chip is an asynchronous memory organized in a nine-bit by forty-character stack. Characters are loaded at the top of the stack and then "sink" to the bottom of the stack, or to the level of previously entered data, without external clocks being applied. As a character is taken from the bottom of the stack, all of the previously loaded characters will automatically propagate toward the output (bottom of stack).

Data can be entered whenever the INPUT REGISTER EMPTY line is high by strobing INPUT STROBE. The INPUT ENABLE line must also be high while strobing. The INPUT STROBE resets INPUT REGISTER EMPTY and latches the input data. As soon as this data is latched, INPUT REGISTER EMPTY will again go high and additional data can be loaded.

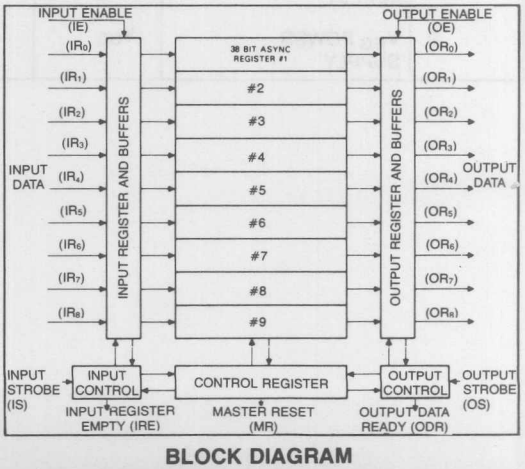
When data reaches the FIFO output, the OUTPUT DATA READY line will go high. The data is then valid at the outputs (providing the OUTPUT ENABLE line is high). The falling edge of the OUTPUT STROBE causes the OUTPUT DATA READY line to go low and to shift new data into the output register. When the new data is available, the OUTPUT DATA READY signal again goes high.

The FIFO output data lines are in high impedance state whenever the OUTPUT ENABLE line is low.

The logic conventions and internal delays designed into the FIFO allow direct expansion of the memory without external hardware (Cascade Mode).



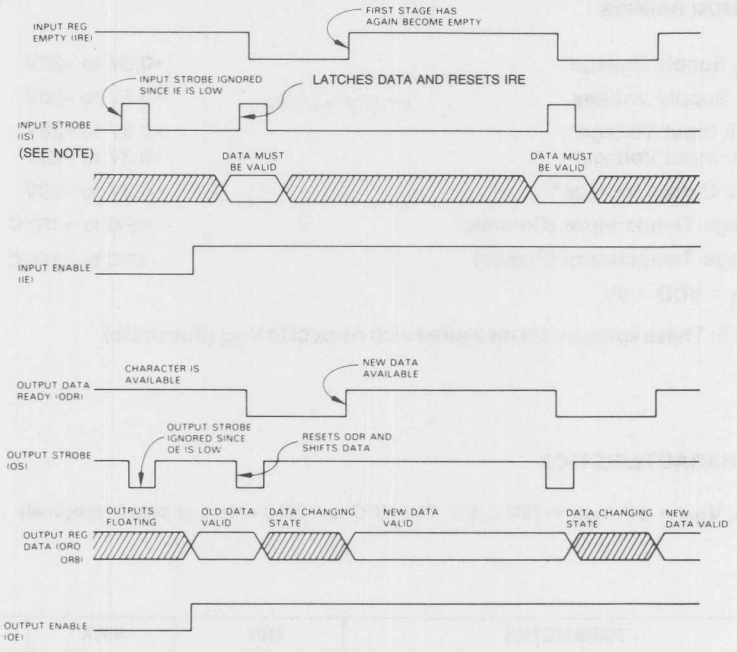
PIN DESIGNATION



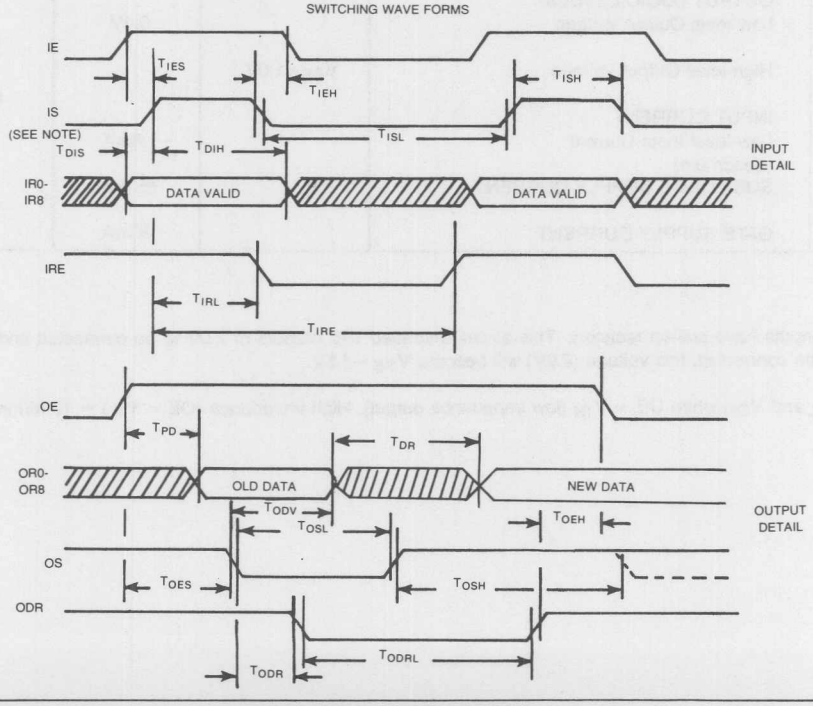
BLOCK DIAGRAM

INTERFACE SIGNALS DESCRIPTIONS

PIN NUMBER	SIGNAL NAME	SYMBOL	FUNCTION
25-28, 2-6	INPUT REGISTER	IR0-IR8	Input datalines. These are input (but not latched) to the FIFO independently of the INPUT ENABLE or INPUT STROBE.
20	INPUT REGISTER EMPTY	IRE	When high, indicates that data can be loaded into the FIFO. It is reset to a low by falling edge of the Input Strobe.
22	INPUT STROBE	IS	Latches INPUT DATA in the FIFO on rising edge.
24	MASTER RESET	MR	When high, clears the FIFO control registers. This leaves the OUTPUT REGISTER DATA (OR0-OR8) in an undefined state, sets INPUT REGISTER EMPTY (IRE) to high and resets OUTPUT DATA READY (ODR) to low.
19-11	OUTPUT REGISTER DATA	ORO-OR8	Three state data outputs. When OE is low, the outputs are in the high impedance state. When OE is high, these lines present the previous latched data in a first-in/first-out manner.
10	OUTPUT DATA READY	ODR	ODR is high when data is latched and available at the data output lines. Is reset to low by the falling edge of OUTPUT STROBE (OS) if OUTPUT ENABLE (OE) is high.
7	OUTPUT STROBE	OS	A falling edge of this signal resets the OUTPUT DATA READY (ODR) line and then shifts the data one step towards the output if OUTPUT ENABLE (OE) is high.
23	INPUT ENABLE	IE	When high, enables the input control logic. At any state of IE or IS, the INPUT DATA will be transferred into the FIFO, but can not be latched unless IE is high.
8	OUTPUT ENABLE	OE	When low, OE puts the output lines (OR0-OR8) in high impedance state. When high, the output lines present the output data.
1	V_{SS} POWER SUPPLY	V_{SS}	+5VDC
21	V_{DD} POWER SUPPLY	V_{DD}	0 Volt—GND
9	V_{GG} POWER SUPPLY	V_{GG}	−12VDC



SWITCHING CHARACTERISTICS



SWITCHING WAVE FORMS

ABSOLUTE MAXIMUM RATINGS

V_{GG} Supply Voltage	+0.3V to -20V
V_{DD} Supply Voltage	+0.3V to -20V
Clock Input Voltage*	+0.3V to -20V
Logic Input Voltage*	+0.3V to -20V
Logic Output Voltage*	+0.3V to -20V
Storage Temperature (Ceramic)	−65°C to +150°C
Storage Temperature (Plastic)	−55°C to +125°C

*V_{GG} = VDD = 0V

NOTE: These voltages are measured with respect to V_{SS} (Substrate)

ELECTRICAL CHARACTERISTICS

(V_{SS} = +5V ± 5%; V_{DD} = 0V; V_{GG} =-12V ± 5%; TA = 0°C to +70°C unless otherwise specified)

SYMBOL	PARAMETER	MIN	MAX	CONDITIONS
	INPUT LOGIC LEVELS			
V_{IL}	Low-level Input Voltage		0.8V	V_{SS} = 4.75V
V_{IH}	High-level Input Voltage	V_{SS}−1.5V		(NOTE 1)
	OUTPUT LOGIC LEVELS			(NOTE 2)
V_{OL}	Low-level Output Voltage		0.4V	V_{SS} = 5.25V I_{OL} = −1.6mA
V_{OH}	High-level Output Voltage	V_{SS}−1.0V		V_{SS} = 4.75V I_{OH} = +200 uA
	INPUT CURRENT			
I_{IL}	Low-level Input Current (each pin)		−1.6mA	V_{SS} = 5.25V V_{IN} = 0.4V
I_{SS}	SUBSTRATE SUPPLY CURRENT		65 mA	V_{SS} = 5.25V V_{GG} = −12.6V
I_{GG}	GATE SUPPLY CURRENT		−30mA	V_{IN} = 0.4V

NOTE 1: All inputs have pull-up resistors. This allows unloaded TTL outputs of 2.0V to be connected and operate properly. When connected, this voltage (2.0V) will become V_{SS} −1.5V.

NOTE 2: V_{OL} and V_{OH} when OE = V_{IH} (low impedance output). High impedance (OE = V_{IL}) ≈ 10 Mohm.

SWITCHING CHARACTERISTICS — See "Switching Waveforms"

(V_{SS} = +5V, V_{DD} = 0V, V_{GG} = −12V, T_A = 0°C to +70°C, C_{LOAD} = 10 pf)

SYMBOL	PARAMETER	MIN	MAX	CONDITIONS
T_{IES}	Input Enable Setup Time	0 ns		
T_{IEH}	Input Enable Hold Time	0 ns		
T_{DIS}	Data Input Setup Time	0 ns		
T_{DIH}	Data Input Hold Time	250 ns		
T_{IRL}	Input Register Load Time		250 ns	
T_{IRE}	Input Register Empty Time		800 ns	
T_{ISL}	Input Strobe Low Time	450 ns		
T_{ISH}	Input Strobe High Time	150 ns		
T_{OES}	Output Enable Setup Time	50 ns		
T_{OEH}	Output Enable Hold Time	50 ns		(NOTE 1)
T_{OSL}	Output Strobe Low Time	150 ns		
T_{ODR}	Output Data Ready Time		200 ns	
T_{DR}	Data Reset Time		600 ns	
T_{PD}	Output Propagation Delay Time		250 ns	
T_{ODRL}	Output Data Ready Low		600 ns	
T_{OSH}	Output Strobe High Time	500 ns		
T_{ODV}	Output Data Valid Time		200 ns	
T_R	Maximum Ripple Time		10 μs	(NOTE 2)
T_B	Maximum Bubble Time		25 μS	(NOTE 3)
T_{MR}	Master Reset Pulse Time	500 ns		
f_D	Maximum Data Rate		1 MHz	(NOTE 4)

NOTE 1: $T_{rise} = T_{fall} = 10nS$.

NOTE 2: Ripple Time—time required for a single data character to propagate from the input to the output of an empty FIFO (IS strobing edge to ODR rising edge).

NOTE 3: Bubble Time— time required for a "hole" to propagate from the output to the input of a full FIFO (falling edge of OS to rising edge of IRE).

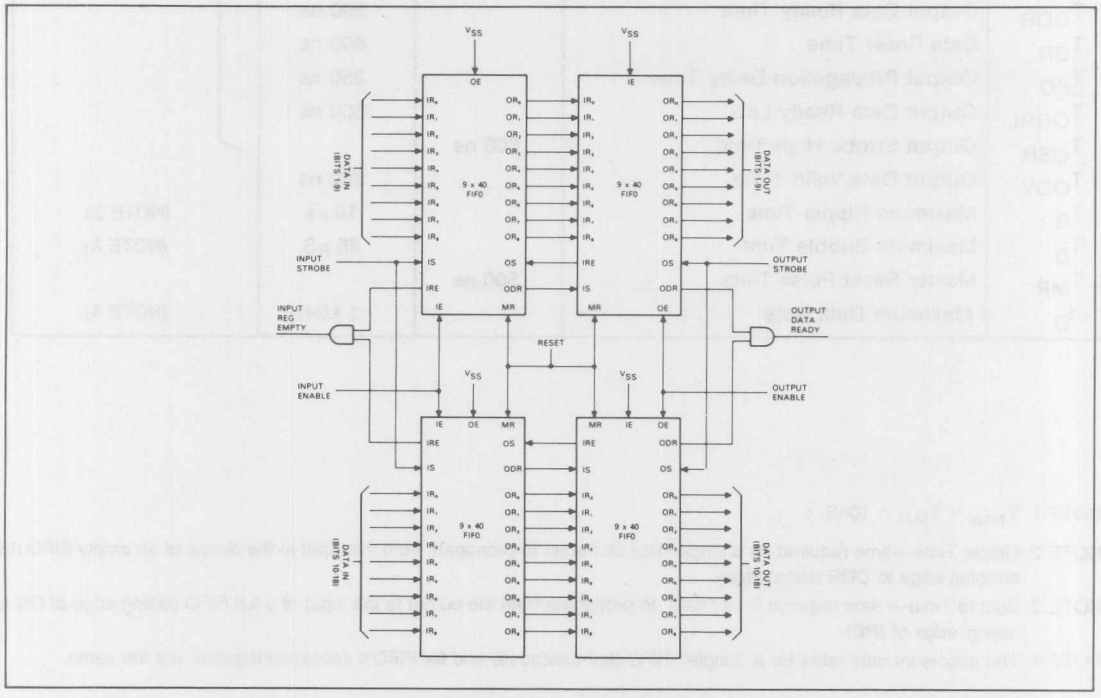
NOTE 4: The maximum data rates for a "single" FIFO (not cascaded) and for FIFO's cascaded together are the same.

GENERAL NOTE: All A.C. test points are at 0.8V or 2.0V.

ORDERING INFORMATION

T_A = O°C to +70°C

PART NO.	PACKAGE TYPE	CASCADABLE	MAX. DATA RATE
E-10	CERAMIC	YES	1.0 MHz
F-10	PLASTIC	YES	1.0 MHz
E-11	CERAMIC	NO	500 KHz
F-11	PLASTIC	NO	500 KHz



EXPANSION EXAMPLE

FR1502E/F-10

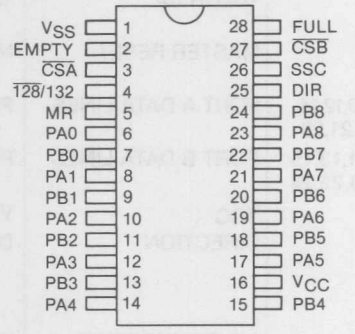
See page 429 for ordering information.

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WD1510—00, -01, -02, -03 LIFO/FIFO Buffer Register

FEATURES

- WORD LENGTH SELECTABLE: 128 OR 132
- 9 BIT WORD WIDTH
- DC TO 650 KHZ (–00), 1 MHz (–01), 1.5 MHz (–02), 1.8 MHz (–03)
- EMPTY AND FULL FLAGS
- THREE-STATE DATA LINES
- 5-VOLT ONLY
- NO EXTERNAL CLOCKS REQUIRED
- TTL COMPATIBLE ON ALL INPUTS AND OUTPUTS
- 28 PIN PLASTIC OR CERAMIC DIP
- CASCADABLE WITH WD1511 SUPPORT CHIP
- FULLY ASYNCHRONOUS DUAL PORT OPERATION



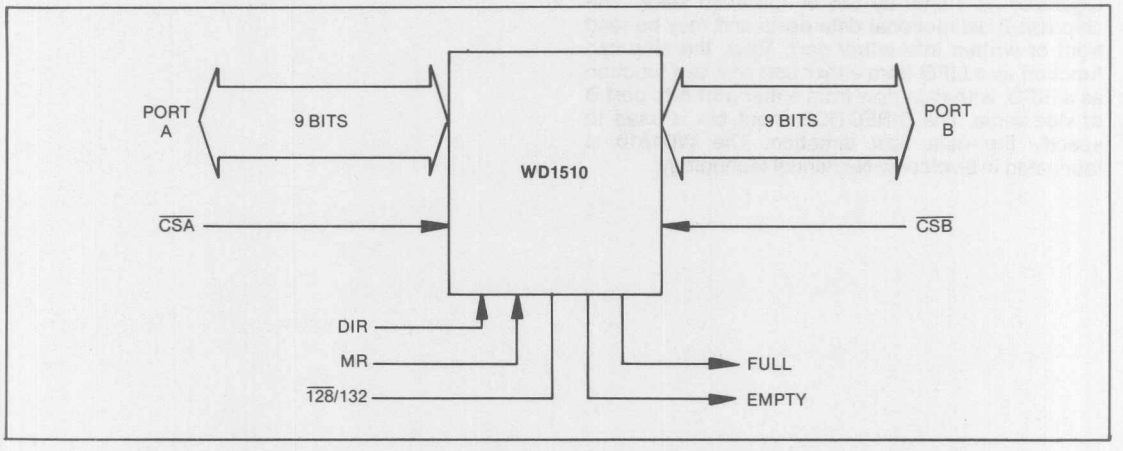
PIN DESIGNATION

DESCRIPTION

The WD1510 is an MOS/LSI Memory Buffer which is organized as a 9-bit by 128 or 132 word stack. The chip has 2 bidirectional data ports and may be read from or written into either port. Thus, the chip can function as a LIFO from either port or it can function as a FIFO, with data flow from either port A to port B or vice versa. The DIRECTION input pin is used to specify the data flow direction. The WD1510 is fabricated in 5-volt only N-channel technology.

PIN DESCRIPTION

PIN NUMBER	NAME	SYMBOL	FUNCTION
1	VSS	VSS	Ground
2	EMPTY	EMPTY	Indicates when there is no data in the buffer
3	CHIP SELECT PORT A	$\overline{CSA}$	Used to select Port A for either a Read or Write operation
4	128 OR 132	$\overline{128}$/132	Used to set word length. When low word length = 128, when high word length = 132
5	MASTER RESET	MR	When pulsed will clear the buffer and set the EMPTY pin
6,8,10,12,14, 17,19,21,23	PORT A DATA LINES	PA0-PA8	Bidirectional DATA Port for reading or writing
7,9,11,13,15 18,20,22,24	PORT B DATA LINES	PB0-PB8	Bidirectional DATA Port for reading or writing
16	V_{CC}	V_{CC}	+5 volts ± .25V
25	DIRECTION	DIR	When low DIR specifies that Port A may be read from and Port B may be written into. When high DIR specifies that Port A may be written into and Port B may be read from.
26	NO CONNECTION	NC	No connection (not for customer use).
27	CHIP SELECT PORT B	$\overline{CSB}$	Used to select Port B for either a Read or Write Operation
28	FULL	FULL	Indicates that all 132 or 128 words of memory are loaded with data



OPERATION

The WD1510 contains a 132 x 9 buffer which may be programmed for 128 x 9 operation. Setting the $\overline{128}$/132 pin to a Logic 0 enables the EMPTY and FULL lines to be activated when 128 bytes are read or written. When the $\overline{128}$/132 line is set to a Logic 1 or left open, the 132 byte operation is enabled. This line contains an internal pull-up resistor of approximately 5KΩ.

When the Master Reset Line (pin 5) is set to a Logic 1, all internal counters are reset and the EMPTY Flag is set. Prior to reading or writing data, the DIRECTION Line (pin 25) must be set to select the desired operation:

DIR	PORT A	PORT B
1	WRITE	READ
0	READ	WRITE

To operate the device in the FIFO mode, both Ports must be used. If the DIRECTION Line is set to a Logic 1, then data is written into Port A and read out of Port B. Reading/Writing to the two ports can be done asynchronously.

In the LIFO mode only one port is used. For example, if using Port A, the DIRECTION Line is set to a Logic 1 to enter data, and is reset to a Logic 0 to read data.

Reading or writing is performed by setting the appropriate $\overline{CS}$ (Chip Select) Line to a Logic 0. After the specified hold time has expired, data may be entered or read on the rising edge of $\overline{CSA}$ or $\overline{CSB}$. In a Read mode, data is valid as long as $\overline{CS}$ remains active. Both Ports return to the high impedance state when $\overline{CS}$ is returned to a Logic 1.

The EMPTY Line (Pin 2) and the FULL Line (Pin 28) are used as status or interrupt lines to determine the status of the buffer. When both EMPTY and FULL are at a Logic 0, the buffer contains 1 thru 127 bytes ($\overline{128}$/132 = 0) or 1 thru 131 bytes ($\overline{128}$/132 = 1).

ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS

V_{CC} with respect to V_{SS} (Ground) ..... +7V
Max Voltage on any Pin with respect to V_{SS} ..... −0.5V to +7V
Operating Temperature ..... 0°C to 70°C
Storage Temperature
Plastic ..... −55°C to +125°C
Ceramic ..... −65°C to +150°C

OPERATING CHARACTERISTICS (DC)

TA = 0°C to 70°C, V_{SS} = 0V, V_{CC} = +5V ± .25V

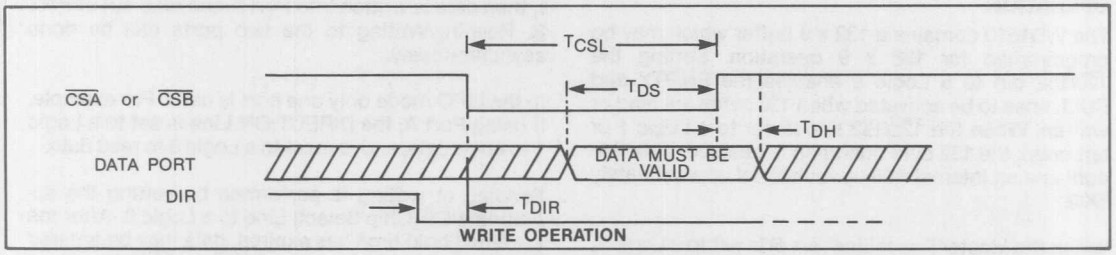
SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNITS	CONDITIONS
I_{LI}	Input Leakage			10	μA	$V_{IN} = V_{CC}$
I_{LO}	Output Leakage			10	μA	$V_{OUT} = V_{CC}, V_{SS}$
V_{IH}	Input High Voltage	2.2			V	
V_{IL}	Input Low Voltage			0.8	V	
V_{OH}	Output High Voltage	2.4			V	$I_O = -100\mu A$
V_{OL}	Output Low Voltage			.4	V	I_O = 1.6 mA
I_{CC}	Power Supply Current		125	200	mA	All outputs open

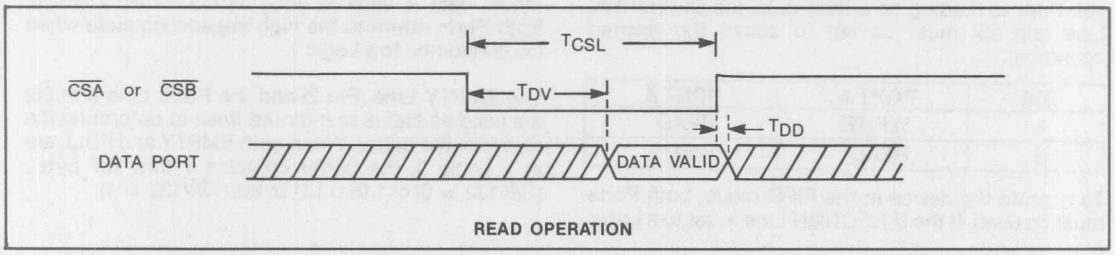
A.C. TIMING CHARACTERISTICS

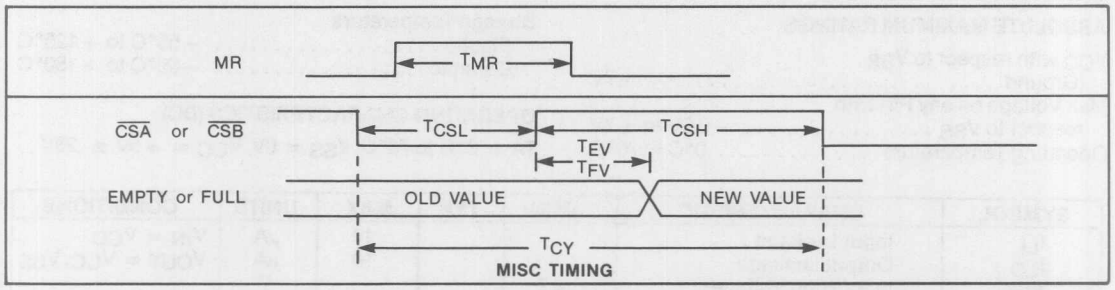
TA = 0°C to 70°C, V_{SS} = 0V, V_{CC} = +5V ± .25V, V_{OH} = 2.0V, V_{OL} = 0.8V

SYMBOL	CHARACTERISTICS	WD1510-00*		WD1510-01*		WD1510-02*		WD1510-3*	
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX
T_{MR}	Master Reset Time	400		250		250			
T_{DV}	Data Valid from CS		550		350		300		
T_{DD}	Data Delay from CS		110		85		60		
T_{DH}	Data Hold from CS	150		100		80			
T_{DIR}	DIR Setup Time	1500		1000		834			
T_{EV}	EMPTY Valid from CS		550		350		250		
T_{FV}	FULL Valid from CS		550		350		250		
T_{CSL}	CS Pulse Width Low	600		500		417			
T_{CSH}	CS Pulse Width High	600		500		417			
T_{CY}	CS Cycle Time	1540		1000		834			
T_{DS}	Data Setup Time	80		50		50			
F_{MAX}	Data Transfer Rate		.65		1.0		1.5		1.8

*All values are in nanoseconds with the exception of F_{MAX} = MHz.







CAPACITANCE

T_A = 25°C; V_{CC} = GND = 0V

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT	TEST CONDITIONS
C_{IN}	Input Capacitance		6	10	pF	f_C = 1 MHz
$C_{I/O}$	I/O Capacitance		15	20	pF	Unmeasured pins returned to GND.
C_L	Load Capacitance		50		pF	V_{CC} = 5.0 V

WD1510 CAPACITANCE LEVELS

See page 429 for ordering information.

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ADVANCED INFORMATION

WD1511 LIFO/FIFO Support Device

FEATURES

- CASCADES UP TO 4 ASYNCHRONOUS RAM BASED LIFO'S/FIFO'S
- CONTROLS 2-TO-1 OR 4-TO-1 BUFFERED BUS CONVERSION
- PIN SELECTABLE OPERATING MODES
- LOGICALLY TRANSPARENT TO HOST INTERFACE
- ALL INPUTS AND OUTPUTS TTL COMPATIBLE
- SINGLE +5V SUPPLY
- 20 PIN DUAL-IN-LINE PACKAGE
- DIRECT COMPATIBILITY WITH THE WD1510 LIFO/FIFO

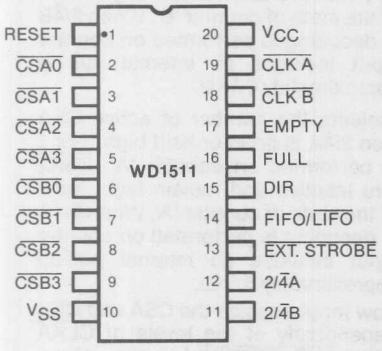
DESCRIPTION

The WD1511 is designed to cascade RAM based FIFO's without resorting to 'bucket brigade' architectures. Cascading is implemented by logically demultiplexing sequential data bytes into two (or four) FIFO's. Data read out of the FIFO's is logically multiplexed, restoring the original order.

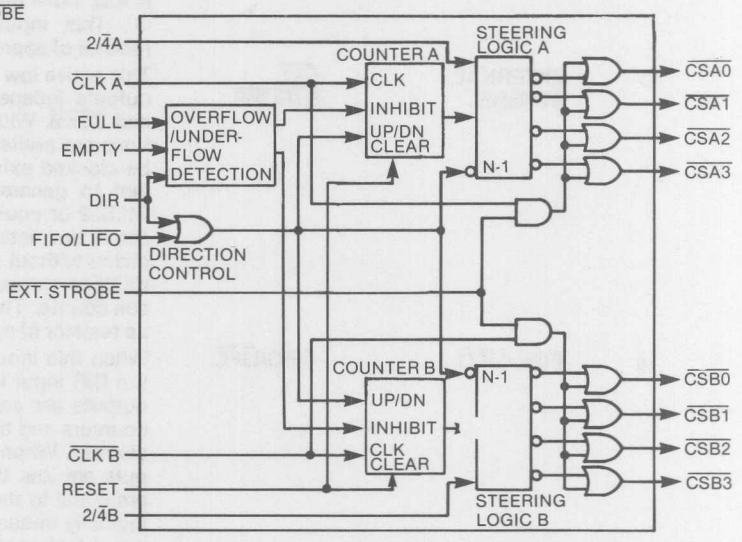
The WD1511 provides all of the necessary data strobe steering logic to demultiplex/multiplex the data stream for both FIFO and LIFO applications. This technique is also employed in implementing 2-to-1 or 4-to-1 bus conversion.

Normally, data strobes are routed through the WD1511. However, in applications where data hold times are critical, grounding the $\overline{\text{EXT. STROBE}}$ pin makes it possible to reduce propagation delays by gating the strobes externally to the WD1511.

The WD1511's cascading technique reduces the duty factor for each FIFO device and may make higher throughput possible.



PIN DESIGNATION



FUNCTIONAL BLOCK DIAGRAM

ORGANIZATION

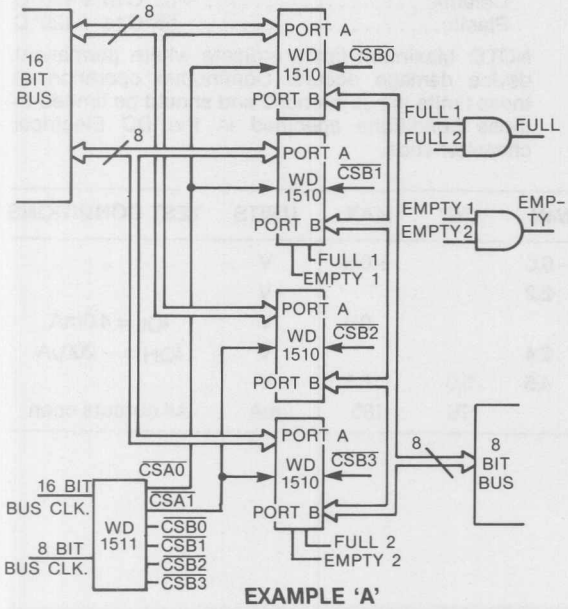
The WD1511 is organized as a pair of synchronous up/down Gray counters with fully decoded outputs. Clocking occurs on low-to-high transitions of the clock inputs. FULL and EMPTY FIFO status inputs are gated with DIR to inhibit counting during FIFO overflow or underflow. A logic one on either DIR or FIFO/$\overline{\text{LIFO}}$ causes the counters to increment when clocked and the decoders to decode for N. A logic zero on both the DIR and FIFO/$\overline{\text{LIFO}}$ inputs causes the counters to decrement when clocked and the decoders to decode for N-1. A2/$\overline{4}$ and B2/$\overline{4}$ determine the number of active discrete outputs for each decoder. A logic one on $\overline{\text{EXT. STROBE}}$ causes both decoders' active low outputs to be "OR-ED" with the counter clocks. Reset forces the counters to asynchronously clear.

WD1511 PIN DEFINITIONS

PIN NUMBER	PIN NAME	SYMBOL	FUNCTION
1	RESET	RESET	Active high input. Asynchronously clears counter A and counter B.
2, 3, 4, 5	CHIP SELECT 'A' OUTPUTS	CSA0-CSA3	Active low, 1-of-4 CSA steering logic outputs. $\overline{\text{CLKA}}$ or $\overline{\text{EXT. STROBE}}$ must be low to enable the active output.
6, 7, 8, 9	CHIP SELECT 'B' OUTPUTS	CSB0-CSB3	Active low, 1-of-4 CSB steering logic outputs. $\overline{\text{CLKB}}$ or $\overline{\text{EXT. STROBE}}$ must be low to enable the active output.
10	V_{SS}	V_{SS}	Ground
11	2/$\overline{4}$B	2/$\overline{4}$B	This input selects the number of active CSB outputs. When 2/$\overline{4}$B is open or held high, 1-of-2 decoding is performed on counter 'B'; $\overline{\text{CSB2}}$ and $\overline{\text{CSB3}}$ are inactive and remain high, independently of the state of counter 'B'. When 2/$\overline{4}$B is low, 1-of-4 decoding is performed on counter 'B'. This input includes an internal pull-up resistor of approximately 6.5KΩ.
12	2/$\overline{4}$A	2/$\overline{4}$A	This input selects the number of active CSA outputs. When 2/$\overline{4}$A is open or held high, 1-of-2 decoding is performed on counter 'A'; $\overline{\text{CSA2}}$ and $\overline{\text{CSA3}}$ are inactive and remain high, independently of the state of counter 'A'. When 2/$\overline{4}$A is low, 1-of-4 decoding is performed on counter 'A'. This input includes an internal pull-up resistor of approximately 6.5KΩ.
13	EXTERNAL STROBE	$\overline{\text{EXT. STROBE}}$	This active low input enables the CSA and CSB outputs independently of the levels of $\overline{\text{CLKA}}$ and $\overline{\text{CLKB}}$. With $\overline{\text{EXT. STROBE}}$ low, several options are available; the chip select outputs can be clocked externally with a 74LS02 or equivalent to generate active high data strobes; a 74LS32 or equivalent can be used to generate active low data strobes; WD1511's can be cascaded without additive propagation delays; the WD1511 can be used as a dual, 4-output Johnson counter. This input includes an internal pull-up resistor of approximately 6.5KΩ.
14	FIFO/$\overline{\text{LIFO}}$	FIFO/$\overline{\text{LIFO}}$	When this input is open or held high, or when the DIR input is high, the active steering logic outputs are equal to the current states of the counters and the counters will increment when clocked. When both the FIFO/$\overline{\text{LIFO}}$ and DIR inputs are low, the active steering logic outputs are equal to the current states of the counters, logically minus one, and the counters will decrement when clocked. This input includes an internal pull-up resistor of approximately 6.5KΩ.

PIN NUMBER	PIN NAME	SYMBOL	FUNCTION
15	DIRECTION	DIR	This input determines which counter shall be inhibited when the full or empty inputs are active. It is also gated with the FIFO/$\overline{\text{LIFO}}$ input to control steering logic decoding and provide counter up/down control.
16	FULL	FULL	This active high input is used to prevent the data pointers (chip selects) from being invalidated during overflow conditions. When both the FULL and DIR inputs are high, counter 'A' is inhibited or frozen at its current count. When FULL is high and the DIR input is low, counter 'B' is inhibited. This input must be held low if unused.
17	EMPTY	EMPTY	This active high input is used to prevent the data pointers (chip selects) from being invalidated during underflow conditions. When both the EMPTY and DIR inputs are high, counter 'B' is inhibited or frozen at its current count. When EMPTY is high and the DIR input is low, counter 'A' is inhibited. This input must be held low if unused.
18	CLOCK B	$\overline{\text{CLK B}}$	This input clocks counter 'B' on the low-to-high transition. The active 1-of-4 CSB output is enabled when either CLKB or EXT. STROBE is low.
19	CLOCK A	$\overline{\text{CLK A}}$	This input clocks counter 'A' on the low-to-high transition. The active 1-of-4 CSA output is enabled when either $\overline{\text{CLKA}}$ or $\overline{\text{EXT. STROBE}}$ is low.
20	V_{CC}	V_{CC}	+5VDC ±5%

16 x 256 TO 8 x 512 BIDIRECTIONAL FIFO BUFFER

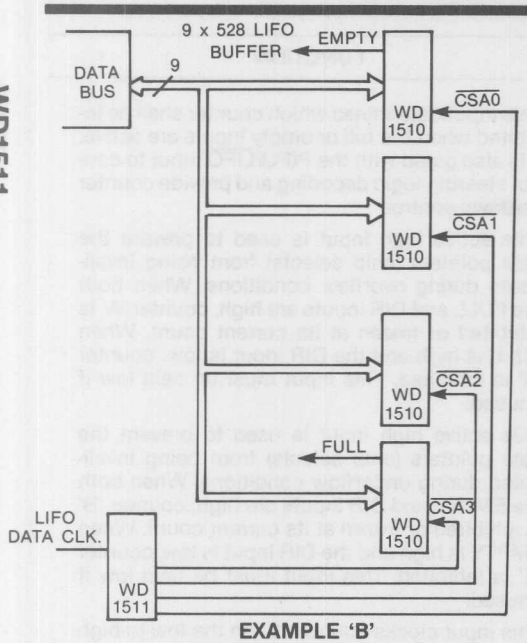


EXAMPLE 'A'

Example 'A' shows the WD1511 used to convert a 16 bit data bus to an 8 bit data bus. With the availability of 4 steering logic outputs, the implementation shown also utilizes the cascade feature providing a 256x16 to 512x8 FIFO Buffer. By placing a logic high on 2/$\overline{4B}$ of the WD1511, decoding would be reduced to 1 of 2 allowing a reduced buffer of 128x16 to 256x8.

A key feature of this implementation is the ability to obtain a speed enhancement for both sides of the data bus. As shown with the WD1510-01, the 8 bit data may be read out at a 2MHz rate. This is due to the FIFO's T_{CSH} time being met during the access times of the other devices. Another key feature with a WD1510 implementation is the completely asynchronous 16 and 8 bus clocks, thereby allowing bidirectional reads and writes asynchronously.

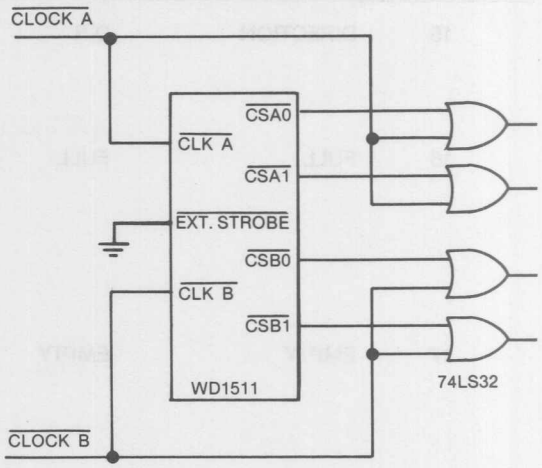
The basic system shown is easily modified to provide many variations. Some of these are: 16 to 16 bit FIFO, 264x18 to 512x9 conversion, 512x9 to 512x9 FIFO, all of which can be bidirectional.



EXAMPLE 'B'

Example 'B' illustrates the simplicity in implementing four WD1510s cascaded for a 528x9 LIFO. This circuit provides the same speed enhancement as Example 'A'. With the WD1510-01, a 2MHz byte rate transfer can be obtained.

It also is easily modified to provide many reduced variations such as 256x8 or 9, or 512x8 or 9.



EXAMPLE 'C'

Example 'C' is shown with $\overline{\text{EXTSTROBE}}$ enabled. This feature reduces the propagation delay of the WD1511 to zero. This feature is required for systems unable to meet data hold times. It is also recommended for use where WD1511s are cascaded for large buffer size applications.

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Ambient Temperature Under Bias ..... 0 to 70°C
Voltage On Any Pin With Respect to Ground (V_{SS}) ..... −0.5 to +7V
Power Dissipation 0.5W

Storage Temperature
Ceramic ..... −65°C to +150°C
Plastic ..... −55°C to +125°C

NOTE: Maximum limits indicate where permanent device damage occurs. Continuous operation at these limits is not intended and should be limited to those conditions specified in the DC Electrical characteristics.

DC ELECTRICAL CHARACTERISTICS

T_A = 0 to 70°C; V_{CC} = 5.0V ± 10%; V_{SS} = 0V

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	TEST CONDITIONS
V_{IL}	Input Low Voltage	−0.5		+0.8	V	
V_{IH}	Input High Voltage	2.2			V	
V_{OL}	Output Low Voltage			0.4	V	I_{OL} = 4.0mA
V_{OH}	High Level Output Voltage	2.4			V	I_{OH} = −200μA
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	
I_{CC}	Supply Current		70	100	mA	All outputs open

See page 429 for ordering information.

WD2501 X.25 Packet Network Interface (LAP)

FEATURES

- Packet switching controller, compatible with CCITT recommendation X.25, level 2, LAP (WD2501)
- Programmable primary timer (T1) and retransmission counter (N2)
- Programmable A-field which provides a wider range of applications than defined by X.25. These include: DTE-to-DTE connection, multipoint and loop-back testing.
- Direct memory access (DMA) transfer: two channels; one for transmit and one for receive. Send/receive data accessed by indirect addressing method. Sixteen output address lines.
- Zero bit insert and delete
- Automatic appending and testing of FCS field
- Computer bus interface structure: 8 bit bi-directional data bus. CS, WE, RE and four input address lines
- DC to 1.1 MBPS data rate
- TTL compatible
- 48 pin dual in-line packages
- Higher bit rates available by special order

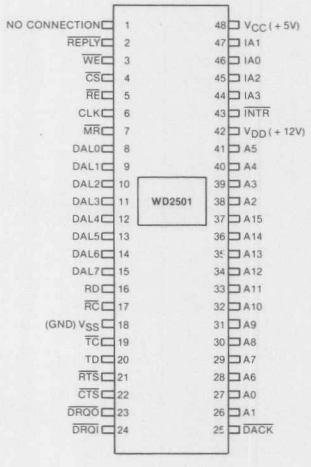
APPLICATIONS

X.25 PACKET SWITCHING CONTROLLER
PART OF DTE OR DCE
PRIVATE PACKET NETWORKS
LINK LEVEL CONTROLLER

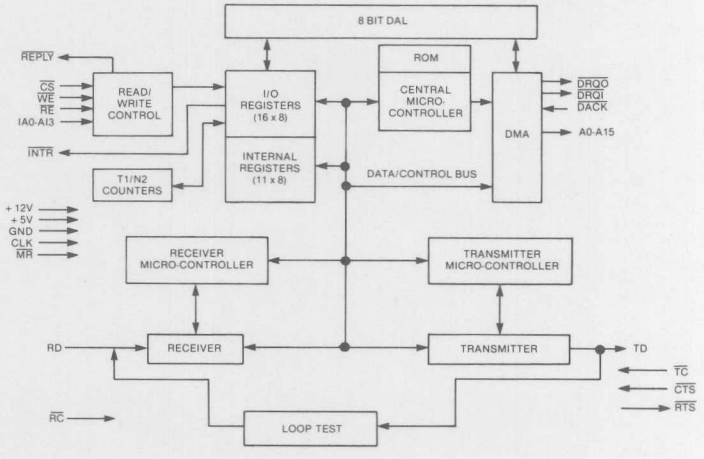
GENERAL DESCRIPTION

The WD2501 is a MOS/LSI device which handles bit-oriented, full-duplex serial data communications with DMA, which conforms to CCITT X.25 with programmable enhancements.

The device is fabricated in N-Channel silicon gate MOS technology and is TTL compatible on all inputs and outputs.



PIN ASSIGNMENTS



WD2501 BLOCK DIAGRAM

WD2511 X.25 Packet Network Interface (LAPB)

FEATURES

- Packet switching controller, compatible with CCITT recommendation X.25, level 2, LAPB (WD2511)
- Programmable primary timer (T1) and retransmission counter (N2)
- Programmable A-field which provides a wider range of applications than defined by X.25. These include: DTE-to-DTE connection, multipoint and loop-back testing.
- Direct memory access (DMA) transfer: two channels; one for transmit and one for receive. Send/receive data accessed by indirect addressing method. Sixteen output address lines.
- Zero bit insert and delete
- Automatic appending and testing of FCS field
- Computer bus interface structure: 8 bit bi-directional data bus. CS, WE, RE and four input address lines
- DC to 1.1 MBPS data rate
- TTL compatible
- 48 pin dual in-line packages
- Higher bit rates available by special order

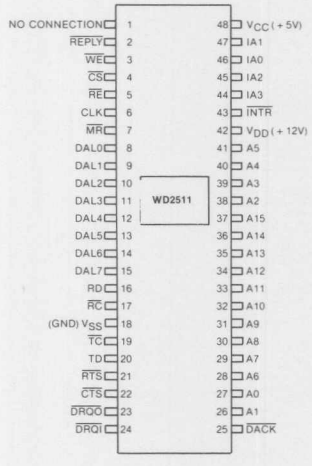
APPLICATIONS

X.25 PACKET SWITCHING CONTROLLER
PART OF DTE OR DCE
PRIVATE PACKET NETWORKS
LINK LEVEL CONTROLLER

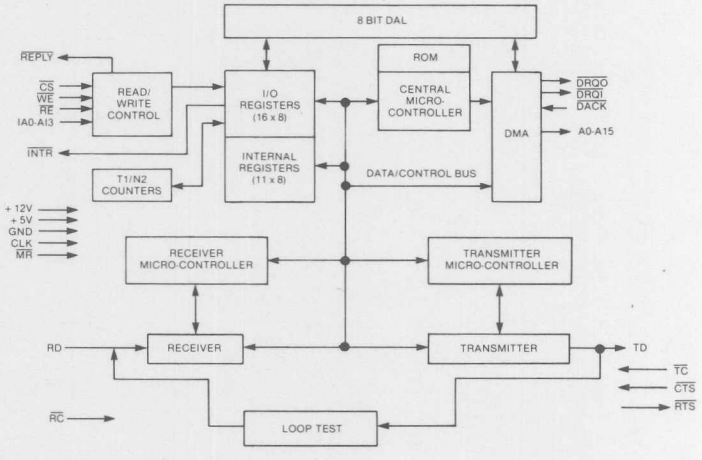
GENERAL DESCRIPTION

The WD2511 is a MOS/LSI device which handles bit-oriented, full-duplex serial data communications with DMA, which conforms to CCITT X.25 with programmable enhancements.

The device is fabricated in N-Channel silicon gate MOS technology and is TTL compatible on all inputs and outputs.



PIN DESIGNATION



BLOCK DIAGRAM

PRELIMINARY

WD2520 Signalling Link Controller

FEATURES

- Performs most of the controls of the Signalling Link Control for Signalling System No. 7.
- Selectable window sizes (8, 32, 128).
- Dual channel DMA for full-duplex operation.
- Unique memory access method for buffer management.
- All formatting of bit-oriented control included: Zero bit insertion and deletion. Automatic appending and testing of flags and FCS fields.
- Automatic control of sequence numbers FSN and BSN, and of control bits FIB and BIB.
- Selectable "Basic" error correction method or the preventive cyclic retransmission error correction method.
- 48-pin dual in-line package. Pin compatible with the WD2501 and WD2511 X.25 link level controllers.
- DC to 1.1M bit/sec transmit-receive rate. (Higher bit rates available.)
- TTL compatible.

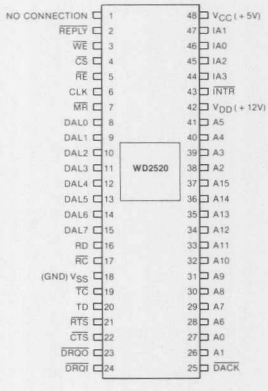
APPLICATIONS

TELEPHONE SIGNALLING
SATELLITE LINKS
PBX SWITCHING/ROUTING
HIGH RELIABILITY COMMUNICATIONS

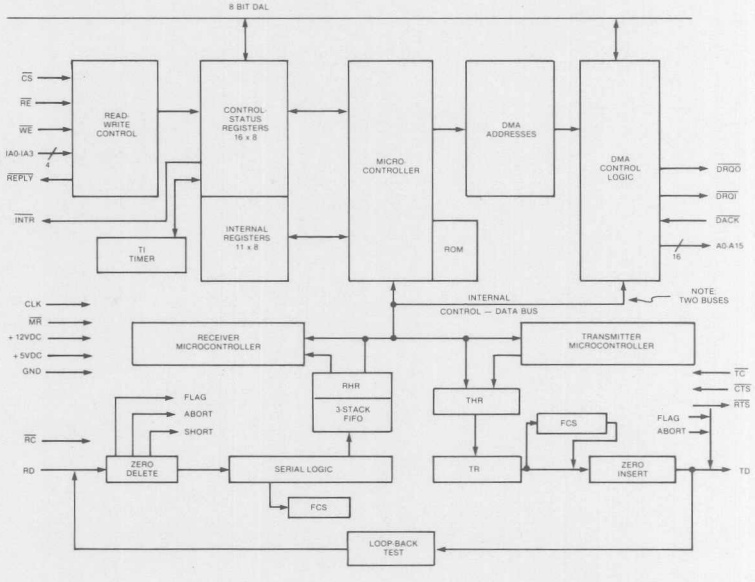
GENERAL DESCRIPTION

Signalling System Number 7 is an international standard for common channel signalling systems, and is used within digital telecommunications networks for call control, remote control, management and maintenance signalling.

The flexible nature of the device allows more general application in systems that have long round-trip delays; notably satellite systems. As with other members of the Western Digital family of Protocol Controllers, all real-time protocol functions are fully handled by the WD2520. Thus, high speed, high efficiency communications are easily integrated into new and existing designs.



PIN DESIGNATION



WD2520 BLOCK DIAGRAM

PRELIMINARY

WD2840 Local Network Token Access Controller

FEATURES

- Broadcast Medium Oriented (Coax, RF, CATV, IR, etc.)
- Up to 254 nodes
- Dual DMA/Highly efficient Memory Block Chaining
- Token based protocol
- Acknowledge option on each datagram
- Adjustable fairness, stations may be prioritized
- Frame format similar to industry standard HDLC
- Supports Global Addressing
- Diagnostic Support: Self-Tests, System and Network
- TTL Compatible

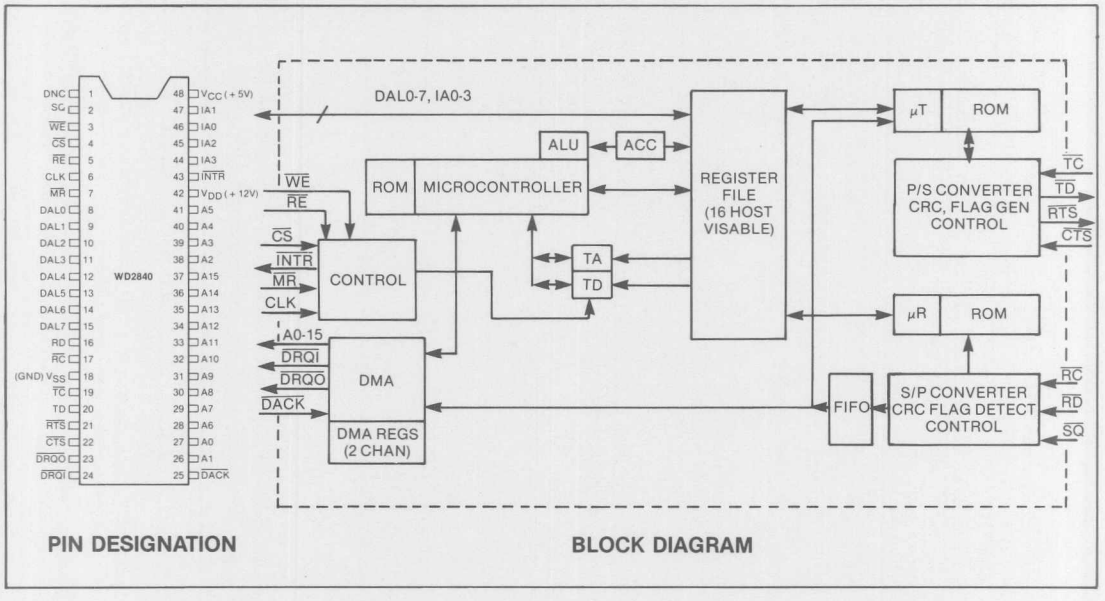
APPLICATIONS

The WD2840 is a general purpose Local Network Token Controller applicable to virtually all types of multi-point communications applications. The token protocol allows the sharing of one bus by up to 254 nodes. WD2840's will be designed into process control equipment, micro-computers, mini-computers, personal computers, proprietary micro-processor based applications, intelligent terminals, front-end processors, and similar equipment.

The great advantage for the design engineer is the ease with which he can implement a local network function. The WD2840 handles autonomously all major communications tasks as they relate to the local network function.

GENERAL DESCRIPTION

The WD2840 is a MOS/LSI device intended for local network applications, where reliable data communications over a shared medium is required. The device uses a buffer chaining scheme to allow efficient memory utilization. This scheme minimizes the host CPU time requirements for handling packets of data. The WD2840 frees the host CPU from extensive overhead by performing network initialization, addressing, coordination, data transmission, acknowledgements and diagnostics.



PIN DESIGNATION **BLOCK DIAGRAM**

Figure 1.1

WD2511 LSI circuit simplifies packet-network connection

48-pin chip replaces entire board and thousands of lines of software

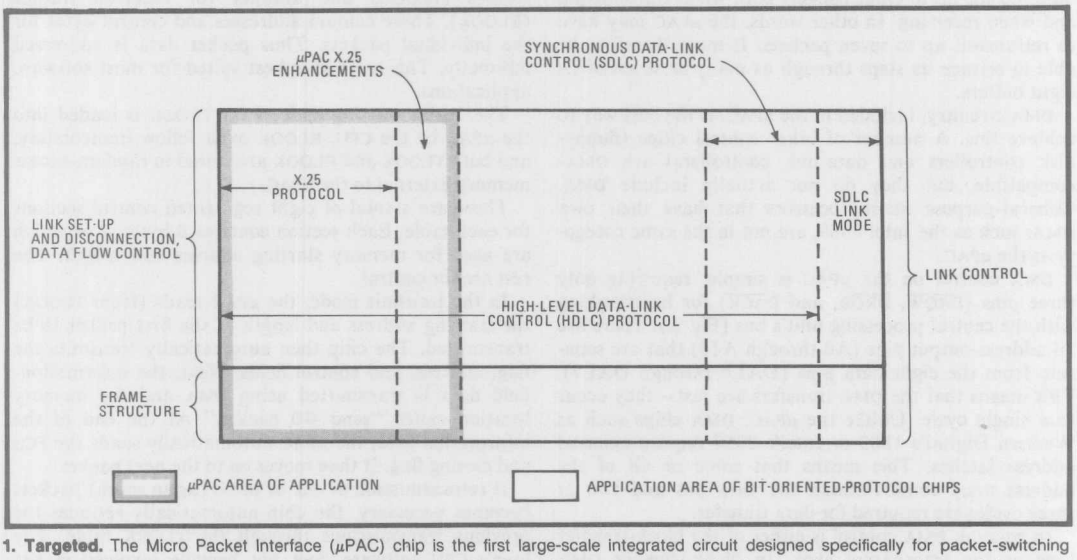
by Geary L. Leger, *Western Digital Corp., Newport Beach, Calif.*

☐ Packet-switching data-communications technology can now claim its first dedicated large-scale integrated circuit. Called the Micro Packet Network Interface chip, or μPAC for short, it is a complete X.25 Level 2 controller with on-chip bidirectional direct-memory-access facilities. This n-channel silicon-gate MOS chip in a 48-pin package replaces a board full of electronics.

The μPAC goes way beyond the functions performed by the bit-oriented-protocol (BOP) control chips currently in widespread use. It includes the circuitry of a BOP chip. But it handles many other operations, eliminating the need for separate DMA circuits and associated address latches, timing chips, and the system software (more than 1,000 lines of code) required until now to perform Level 2 control of the link between a data terminal and a node of a packet-switching network. It has an 11-K read-only memory and the equivalent of three microprocessors: one to handle data-transmission operations, another for dealing with received data, and a third central processor to coordinate all chip functions. Sample quantities of the controller will be available from Western Digital Corp. in the first quarter of 1980.

The data-link controllers already on the market (Western Digital 1933, Signetics 2652, Intel 8273, Zilog SIO, and others) handle BOP frame structure in a broad range of applications. For example, the WD 1933 can be used with the High-level Data Link Control (HDLC) and Synchronous Data-Link Control (SDLC) protocols, including the SDLC loop mode. This chip and others like it handle zero-bit insertion and deletion, the frame-check sequence (FCS), and the flags that define the beginning and end of a data frame.

The μPAC trades some of this protocol flexibility for the sake of greatly enhanced usefulness within its area of application (Fig. 1). It is restricted to the Level 2 packet-switching protocol defined in Recommendation X.25 from the Consultative Committee for International Telephony and Telegraphy (CCITT), a protocol developed from HDLC. But other BOP chips do not set up, disconnect, or reset the link; they do not automatically retransmit up to seven information frames (I frames); nor do they have a timer for retransmission control. These are



1. Targeted. The Micro Packet Interface (μPAC) chip is the first large-scale integrated circuit designed specifically for packet-switching applications. The application range of other chips that handle bit-oriented frame structure is wider, but the μPAC does much more in its area.

TABLE 1: COMPARISON OF FEATURES OF BIT-ORIENTED-PROTOCOL CHIPS

HDLC/ADCCP protocol feature	X.25 Level 2	Bit-oriented-protocol chips	μPAC
Basic bit-oriented frame structure	yes	yes	yes
Retransmission of up to 7 I frames (modulo 8)	yes	no	yes
Asynchronous response mode	yes, LAP	no	yes, 2501
Asynchronous balanced node	yes, LAPB	no	yes, 2511
Control of S, U frames	yes	no	yes
Link set-up, disconnect, and reset procedures	yes	no	yes
Time-out recovery	yes, T1/N2	no	yes, T1/N2
Multipoint operation	no	no	yes
Normal response mode (NRM)	no	no	no
Level 2 modulo 128	FS	no	no

FS = item for further study by the CCITT

all features of the μPAC chip (see Table 1).

Two versions of the μPAC will be made available. One, the WD 2501, uses the Link-Access Procedure (LAP) defined in the first version of X.25. The WD 2511 is for networks using the Link-Access Procedure, Balanced (LAPB) added to X.25 subsequently. The two chips differ only in the program stored in ROM. They are pin-compatible and interchangeable without hardware or software modifications. Both may be used either in a terminal (DTE, data-terminal equipment) or in a network node (DCE, data-circuit–terminating equipment).

Direct memory access

Because of the HDLC feature that allows up to seven packets (I frames) to be outstanding (transmitted but unacknowledged) at any time, the μPAC has information-field data (the I field of an information frame) buffered for up to eight packets both when transmitting and when receiving. In other words, the μPAC may have to retransmit up to seven packets. It must therefore be able to retrace its steps through as many as seven of its eight buffers.

DMA circuitry, included in the μPAC, is the best way to achieve this. A number of other control chips (floppy-disk controllers and data-link controllers) are DMA-compatible, but they do not actually include DMA. General-purpose microprocessors that have their own DMA, such as the Intel 8089, are not in the same category as the μPAC.

DMA control on the μPAC is simple, requiring only three pins ($\overline{\text{DRQW}}$, $\overline{\text{DROR}}$, and $\overline{\text{DACK}}$) for handshaking with the central processing unit's bus (Fig 2.). There are 16 address-output pins (A0 through A15) that are separate from the eight data pins (DAL0 through DAL7). This means that the DMA transfers are fast—they occur in a single cycle. Unlike the μPAC, DMA chips such as Western Digital's 1883 or Intel's 8257 require external address latches. This means that some or all of the address must come through the data bus and two or three cycles are required for data transfer.

In general, DMA control is either of the block-transfer type or the transparent type. In block-transfer DMA control, the DMA controller transfers several bytes of data while the CPU is disabled from using the bus. If transparent, the DMA control is imbedded in the CPU's clock cycle in such a way that the transfers are invisible, or transparent, to the CPU. Since the μPAC must be able to transmit and receive data on two DMA channels at once (for full-duplex operation), the only logical choice for the μPAC is transparent DMA, since block-transfer DMA would restrict operation to half-duplex.

All Level 2 data is appended and checked automatically by the μPAC. The I-field data is accessed via DMA channel. All supervisory frames (S frames) and unnumbered frames (U frames) are automatically transmitted and checked by the μPAC. The user's CPU operates only on the I field of I frames.

Keeping track of packets

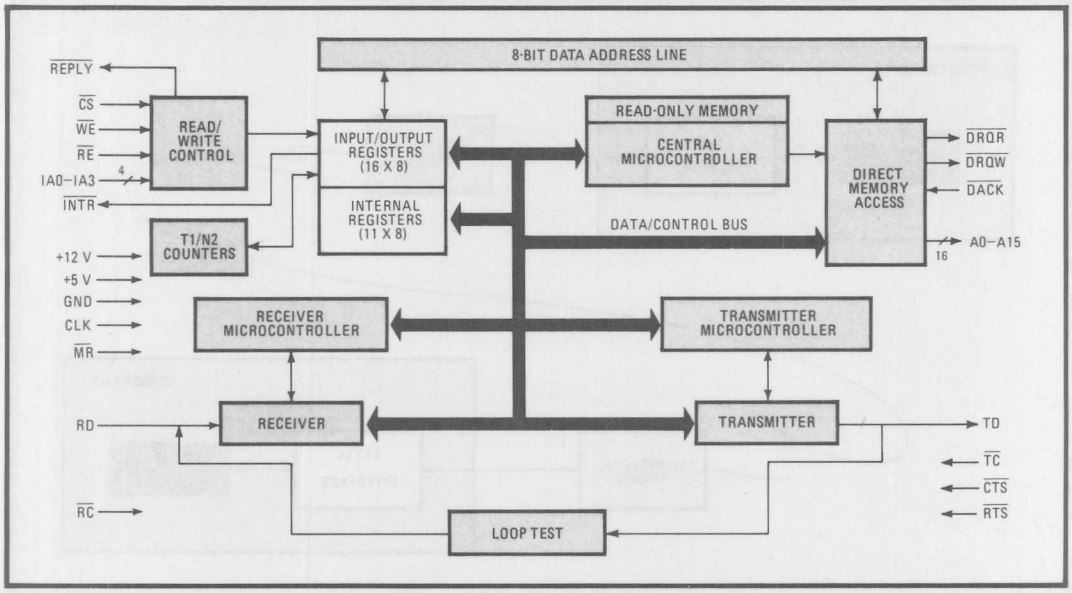
The DMA uses two lookup tables—one for transmitted frames (TLOOK) and another for received frames (RLOOK). These contain addresses and control bytes for the individual packets. Thus packet data is addressed indirectly. This method is best suited for most software applications.

The 16-bit starting address for TLOOK is loaded into the μPAC by the CPU. RLOOK must follow immediately, and both TLOOK and RLOOK are stored in random-access memory external to the μPAC.

There are a total of eight segmented control sections for each table. Each section contains 8 bytes, 4 of which are used for memory starting address and length. The rest are for control.

In the transmit mode, the μPAC reads (from TLOOK) the starting address and length of the first packet to be transmitted. The chip then automatically transmits the flag, address, and control fields. Next, the information-field data is transmitted using DMA and the memory location called "send #0 packet." At the end of the information field, the μPAC automatically sends the FCS and closing flag. It then moves on to the next packet.

If retransmission of one or more (up to seven) packets becomes necessary, the chip automatically retraces the previous transmissions through the TLOOK table. The user's CPU software does not become involved in the retransmission. An error counter is incremented.



2. Inside the μPAC. The Level 2 controller has its own timer and direct-memory-access circuitry and is the logical equivalent of three microprocessors. Routines stored on the chip allow it to relieve the network user's central processor of a large software overhead burden.

Each received frame is checked for correct address and FCS fields and for type of control field. If the frame is an I frame, the I field is placed in the assigned memory location using a method similar to that used in transmission. After the packet is received error-free and in proper sequence, an interrupt is generated and the μPAC is ready for the next packet, which will be placed in the next location.

Ten 8-bit error counters follow RLOOK in the external RAM. These counters do not cause an error interrupt, but maintain a running count of error activity. The contents of the counters include: the number of frames received with FCS error; the number of times T1 (the time minimum set for a timer that allows retransmission of an unacknowledged packet) ran out; and the number of packet retransmissions.

Control bits are included in TLOOK, RLOOK, and the μPAC to ensure orderly transfer of data blocks. For example, the control bits are designed to prevent what is known as "deadly embrace," a situation in which the μPAC and the user's computer are waiting for one another to start.

Self-testing

Self-testing features are critical to proper operation. The μPAC does a comparison test, an internal RAM register test, and a loop-back test. All three are suitable for use during manufacturing and inspection. The internal RAM and loop-back tests are also useful for system diagnostics and troubleshooting.

The comparison test requires a device known to be good or a stored list of known good responses. The program location counter (PLC) for the main ROM is halted so it may be incremented under external control.

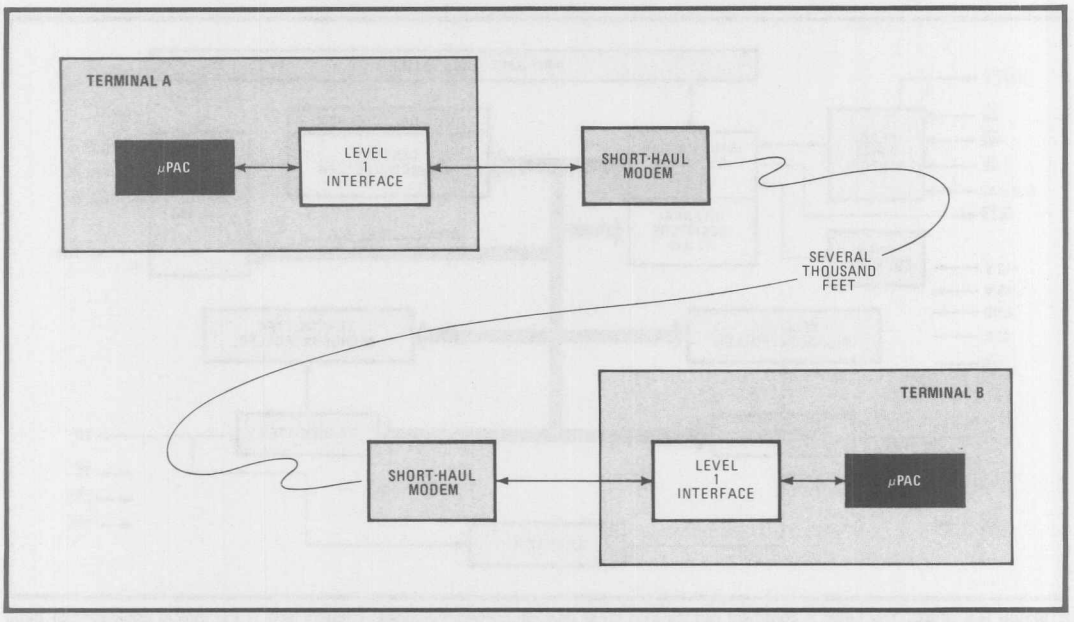
TABLE 2: MICRO PACKET INTERFACE CHIP (μPAC) TERMINOLOGY

ABM	asynchronous balanced mode
ARM	asynchronous response mode
CMDR	command reject (U frame, LAP only)
DISC	disconnect (U frame)
DM	disconnect mode (U frame, LAPB only)
FRMR	frame reject (U frame, LAPB only)
REJ	reject (S frame)
RNR	receiver not ready (S frame)
RR	receiver ready (S frame)
SABM	set asynchronous balanced mode (LAPB only)
SARM	set asynchronous response mode (LAP only)
UA	unnumbered acknowledgement (U frame)

All jumps stored in ROM are disabled so that each location of the PLC may be counted. As the PLC is incremented, the responses of the output pins and status registers are compared to the known good responses.

There are 11 8-bit registers in the μPAC that are not directly accessible by the user's CPU, which complicates testing somewhat. The internal RAM register test provides a means of checking these registers. The contents of register A are placed in six even internal registers and the contents of register B in five odd internal registers. The 11 registers are then added together without carry and the result is placed in status registers. This test is initiated by a control bit in the μPAC. The loop-back test is discussed later.

For the purposes of discussing link establishment procedures, it will be assumed that there is a 2501 μPAC at each end of the link. In practice, the 2501 can



3. Off the network. The μPAC is also useful in non-network applications that use bit-oriented protocols. It provides full-duplex capability, does error detection and recovery, and gives systems the option of hooking directly to a packet-switching network at some future date.

communicate with any device meeting X.25 Level 2 specifications.

When a link is set up, it is said to be in the information-transfer phase. This means that the terminal and node will accept and transmit I and S frames. When a link is logically disconnected, only U frames—DISC, SARM, or UA (disconnect, set asynchronous response mode, and unnumbered acknowledge; see Table 2)—will be accepted or transmitted.

Link supervision

A link-connect frame is not the same as a link-reset frame. A link in the information-transfer phase may be reset in one direction by a SARM transmission. A link is up after both ends send a SARM command and receive a UA response.

Since a SARM can be either a command to reset or set up a link, misinterpretation by the receiver of a SARM is possible. This could happen when a link is established if one end momentarily loses power. When that end tries to bring the link up by sending a SARM, the other end may interpret the command as a link-reset.

There are two ways to get around this problem. Suppose a terminal or node attempting to bring a link up sends a SARM command and receives a UA. After time T1, if the station does not receive SARM, it assumes that the other end considered the link up. It will then disconnect the link by sending DISC and receiving a UA, and attempt to set up a link a second time.

The other way around the problem is the method used by the 2501. The 2501 will always send DISC and receive a UA before attempting to bring the link up. This will assure a logically disconnected link so that it may attempt to set one up. Immediately after the link is up, the 2501 generates an interrupt.

It is possible to recover a single error on a packet with μPAC control. The error makes the received FCS bad, so B does not recognize A's first transmission of frame 1. When B receives frame 2, something is wrong since the last successfully received packet was frame 0. Thus, at the next opportunity, B sends a REJ (reject—an S frame) asking A to retransmit frame 1. This opportunity comes after B completes sending its frame 2.

When A receives the REJ frame, it is sending frame 3. There is no need to continue with frame 3, so A aborts transmission of frame 3 and goes back and retransmits frame 1. After retransmitting frame 1, A will retransmit frames 2 and 3. Finally, A will continue transmitting other frames.

Loop-back

A loop-back condition exists when a station receives the same serial information it has transmitted. In the loop-back test, the serial-transmit output is connected to the serial-receive input in order to test the transmitter and receiver channels. Each station has both primary and secondary functions, so there are two logical primary-to-secondary associations on a terminal-to-node link, and each association is identified by a different address field. This makes loop-back testing impossible when a strict X.25 connection is made. Commands will have the A field of a response and vice versa. One way around this is to make the A fields of the two associations equal for the duration of the loop-back test. (The A fields are programmable in the μPAC.)

Another problem with loop-back testing is the actual

detection of the condition and the detection of the condition's removal. There is no simple way around this problem, and the μPAC gives only limited assistance.

First, detecting the existence of a loop-back condition is the responsibility of the CPU driving the μPAC. If the CPU sees that a link cannot be brought up, or if a link is up and suddenly has excessive link resets and CMDRs (command reject, a U frame), the CPU could assume the presence of a loop-back condition. After making the two A fields the same, if a disconnected link is successfully brought up, then the loop-back condition exists.

To detect the removal of this condition, a particular control bit (RRT1) in the μPAC may be used. It causes the μPAC to send an RR (receiver ready, an S frame) or an RNR (receiver not ready, also an S frame). These frames are sent at T1 intervals as long as the μPAC is not commanded to send a packet. As long as the μPAC receives those S frames, the loop-back condition exists. However, if the μPAC fails to receive an S frame for a time equal to T1 × N2, an interrupt is generated, signalling that the loop-back condition has been removed.

Modified X.25

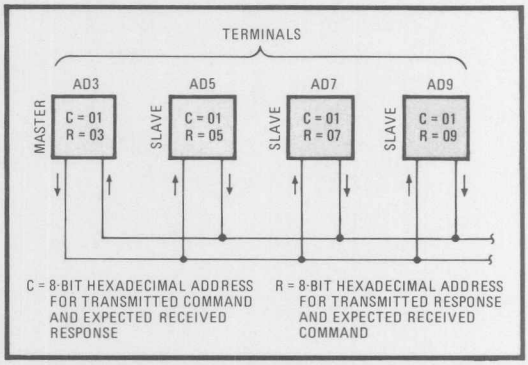
The original design intention was to use the μPAC in a strict X.25 terminal-to-node application, the only application covered by X.25. However, by taking advantage of the terminal-node symmetry of the μPAC (the fact that it can be used in both DTE and DCE), other applications are possible that use its built-in features.

For instance, the user does not need to develop the software for error recovery since this is a μPAC feature. For another, using a μPAC makes it possible to connect a non-packet terminal to an X.25 link at a future time. And lastly, the chip's protocol is bit-oriented. It has a number of advantages over older, character-oriented protocols, such as code transparency, full-duplex capability, flexibility, and modularity [*Electronics*, Jan. 18, 1979, p. 137].

One possible application is the connection of two terminals at Levels 1 and 2 (Fig. 3). How much of Level 3 is used would depend upon the individual application; the more of Level 3 used, the better standardized the interface is. One of the terminals in Fig. 3 could be a terminal concentrator (a Packet Assembly/Disassembly facility, or PAD, as defined by Recommendations X.3, X.28, and X.29) on a factory floor, and the other could be a host computer in a data-processing center.

Modified X.25 could also be used in a multipoint system (Fig. 4). Idle terminals in this type of system must transmit an "idle" sequence, not continuous flags. The terminal addresses (AD3, AD5, AD7, and so on) correspond to the transmitted response A field. The transmitted command A field is the same for all terminals and is chosen to be hexadecimal 01 in this case. All A fields are selected with odd values (least-significant bit transmitted first) to conform to the extended-address format of the Advanced Data-Communication Control Procedures (ADCCP).

Two terminals on the multipoint line may establish and discontinue communications by exercising X.25 procedures for setting up and disconnecting a link. But only two terminals can communicate at any one time.



4. Multipoint line. The programmed features of the μPAC chip enhance the flexibility of a system comprising one master terminal and up to 128 slave terminals. Hardware and software savings are possible when the μPAC is used in this off-network context.

Suppose that AD3 wishes to communicate with AD7. AD3 will first make sure that its receiving line is idle (a status bit in the μPAC). Next, AD3 will change its transmitted command and response A fields to be the reverse of AD7 (command field is set to 07, response field is set to 01). Then AD3 will initiate link establishment by setting a control bit, called "active," in the μPAC. Once the link has been established (the μPAC generates an interrupt when the link is first set up), AD3 and AD7 may exchange I frames. To discontinue the session, either AD3 or AD7 will set the mandatory-disconnect control bit in its μPAC. This will cause that terminal to initiate a logical-disconnect procedure.

Contention and roll-call methods

The multipoint system may be implemented by either contention or roll-call polling. In the roll-call method, the master terminal will initiate link establishment with one of the slave terminals, communicate with that slave, discontinue the session (disconnecting the link), and go on to the next slave. This process continues until all slaves are polled and then starts over. One advantage of the roll-call method is that the master has tight control over the line for efficient operation.

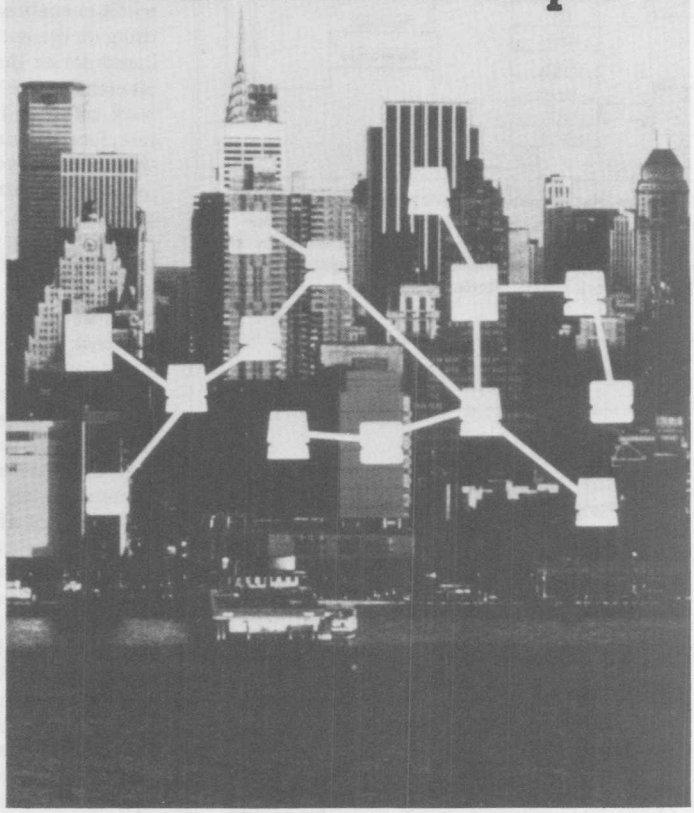
A disadvantage is that slaves must be queried (polled) before sending data, and the more slaves on the line, the longer it takes for the master to poll them. Therefore it is essential that each slave be designed to exchange a relatively small amount of data with the master in a single session, lest it tie up the line for long periods. Large amounts of data should be broken up and exchanged in more than one session. This method is suited to applications where the multipoint line has a high usage.

In the contention method, any terminal may initiate a session at any time. This is similar to a party telephone line and is suited to applications where line usage is low. All sessions are between the master and one of the slaves, but unlike the roll-call method, a slave may initiate the session. The terminal that initiates a session must send an I frame with its unique address immediately after the link is set up. □

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LOCAL NETWORKS

Token passing cashes in with controller chip



Token-passing protocols can upgrade a data-communication system, especially if a dedicated controller relieves the host from token-processing tasks.

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Designers can now implement a distributed-access token-passing systems without worrying about the complex details involved in the communications protocol. Those are taken care of by one LSI chip, called the token-access controller.

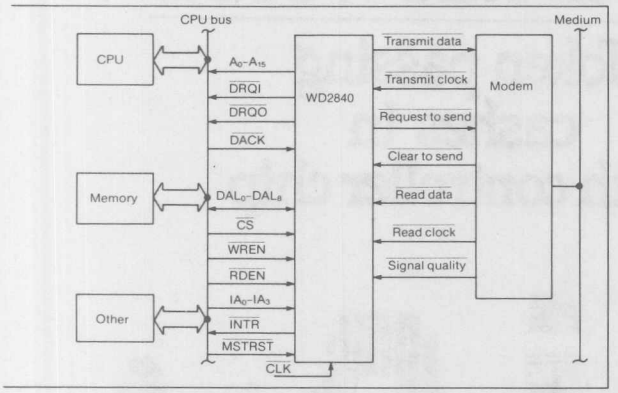
Token passing is one method of sharing a communications path. It enjoys the benefits of distributed-access systems while eliminating the drawbacks of schemes employing carrier-sense multiple access with collision detection (CSMA/CD). Until recently, however, token-passing techniques had little currency because of their need for complex controllers. This need relegated tokens primarily to proprietary uses. (For a complete review of local networks, including token-passing techniques, see "Broad Standards, Many Implementations Are on the Way," ELECTRONIC DESIGN, Sept. 30, p. 87.)

The introduction of Ethernet in 1980 marked the beginning of commercial local networks using distributed-access techniques. A distributed system does not rely on a single device for polling. Early versions of Ethernet were designed to use simple controllers because most of the development work began in the 1970s, before the LSI era. Although CSMA/CD offered a simplified access protocol, users incurred cost, performance, and flexibility penalties. Progress in LSI technology has now given designers the benefits of complexity—increased efficiency and enhanced flexibility—but without high cost.

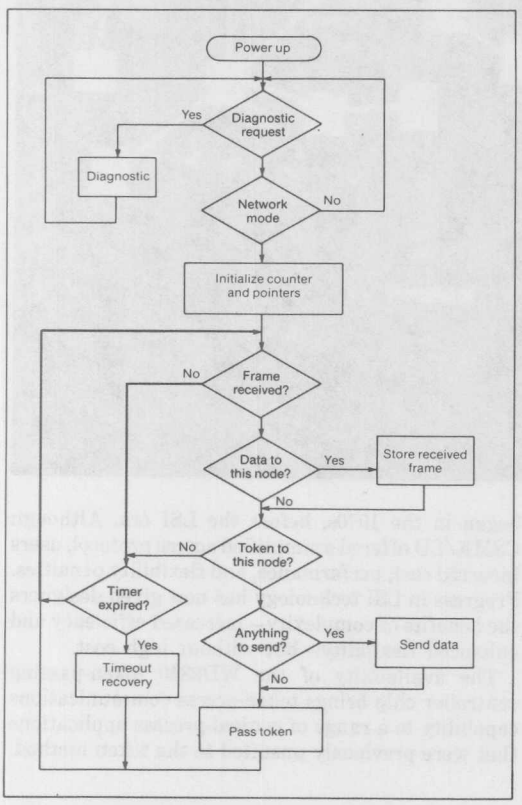
The availability of the WD2840 token-passing controller chip brings token-access communications capability to a range of critical-process applications that were previously unsuited to the token method.

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1. Two interfaces connect the WD2840 token-access controller chip to a local-area network. The network side (medium) is electrically conventional, whereas the host side (CPU) combines both a control and status register and a direct-memory-access interface.



2. After initialization, the token-access controller idles in its "watching" loop (bold lines), waiting for a data frame or token addressed to it. The upper portion of the flow chart shows the steps in the initialization procedure.

What's more, the controller sufficiently reduces system communication costs, encouraging its use with very inexpensive end products.

The controller is designed to connect distributed intelligent devices over a shared broadcast medium —usually coaxial cable, free-air radio, or twisted-pair party line. Shared by all stations through the use of a token-passing protocol, the broadcast medium enables each attached device to hear everything on the network. A station is a microprocessor-based device that incorporates the controller. Complementing the token protocol's efficiency is a high-level, software-friendly DMA (direct memory access) interface contained within the controller. In conjunction with conventional hardware and serial communications interfaces, the DMA interface and token protocol make the WD2840 simple to use.

The primary purpose of a token-access controller is to free the designer from data communications concerns. Once the chip is initialized, for example, the host microprocessor need never bother with the protocol; it merely processes frames addressed to it —the controller filters out all others—and generates messages to send later. In fact, it is the controller that sends messages when a token is received. This decoupling of the functions between the network and any user processing simplifies programming and system timing considerations.

Tasks that affect network performance—such as processing tokens and generating acknowledgments —are performed inside the controller. Thus designers can use any type of host processor in a station (Fig. 1). The circuit interfaces with systems in which a processor is busy with a specific application.

Illustrating that point is the microprocessor found in a CRT terminal. Its duties are to scan the keyboard and perform a limited amount of editing. That leaves enough processing power remaining to drive the controller, which handles data flow only for one specific terminal. If the processor falls behind momentarily, just one terminal is affected; all others in the network continue to operate at full speed. Thus a network of controller chips is not slowed by its weakest link.

Token passing in a system environment

When a token-access controller receives a data frame addressed either to itself or to all broadcast stations—there are 254 stations in a system—it transfers the frame to the host's memory via a DMA operation. If the frame is invalid, the close coupling of protocol handling and DMA operations allows the chip to manage its own housekeeping. For example, if errors are detected through a CRC (cyclic redundancy code) or signal-quality check, the memory space is automatically reclaimed.

On the successful reception of a data frame, the controller sets an interrupt and checks to determine whether an acknowledgment was requested by the sending station. If so, it sends the acknowledgment, adding the receiver status, as well. A typical message might be "Received successfully" or "Encountered DMA problem on this end. Please retry." While the controller evaluates each frame as it looks for its own data message, it simultaneously checks for tokens passed to it. This combined token-and-data frame—in which each part can be directed to a different station—is referred to as piggybacking, a feature that increases system efficiency, since most of the overhead associated with conventional token-passing is eliminated (Fig. 2).

Receipt of a token allows the WD2840 to transmit

A three-controller architecture

A single NMOS LSI chip, the WD2840 token-access controller, comprises three major elements: a fast serial communications subsystem, a two-channel DMA controller, and a microprocessor with internal ROM and RAM.

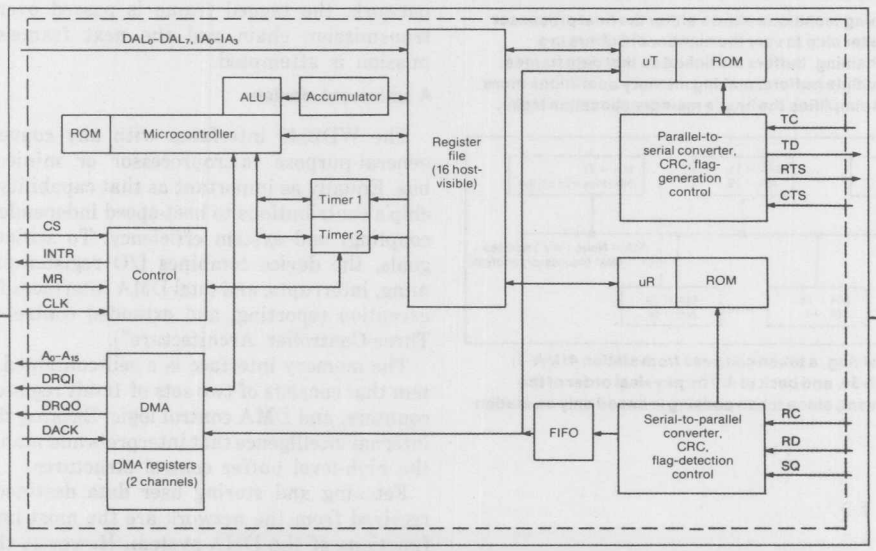
The device's three preprogrammed microcontrollers handle media access and host memory-management functions. This type of architecture facilitates internal parallel processing: for example, prefetching a new buffer address while transmitting or receiving data. Although the token-passing protocol is essentially a half-duplex scheme, separate receiving and transmitting subsystems permit loopback testing.

The primary microcontroller has the capabilities and instruction set of a conventional 8-bit microprocessor, including subroutines, bit manipulation, conditional branching, and arithmetic operations. This part, whose chief task is to implement the token algorithms and maintain the host memory chain, has its firmware located in the internal 1-kbyte ROM. Repetitive and simple operations such as DMA fetching and storing are controlled by the receiving and transmitting microcontrollers.

Two internal timers keep the network independent of the host microprocessor's timing. The first timer is set for a relatively short duration to limit the time it must wait for the required response from a transmission. The second timer has a longer and less critical duration that restricts the period that a network can normally be "idle." Limits on idle time are useful for initialization and some error-recovery operations.

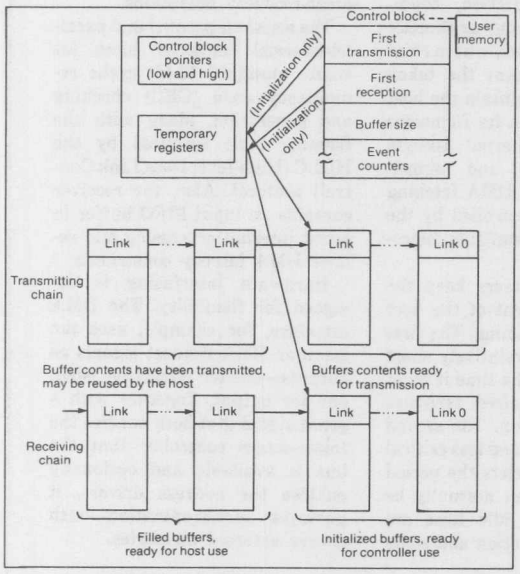
The serial-to-parallel and parallel-to-serial converter block includes standard 16-bit cyclic redundancy code (CRC) checking and generation, along with the framing logic specified by the HDLC (High-level Data Link Control) protocol. Also, the receiver contains an input FIFO buffer to speed internal processing and relieve DMA latency constraints.

Hardware interfacing is designed for flexibility. The DMA interface, for example, uses the familiar DMA request signals as outputs—one for input requested, one for output. Together with a grant signal that both notifies the token-access controller that the bus is available and optionally enables the address drivers, it permits synchronization with slower external memories.

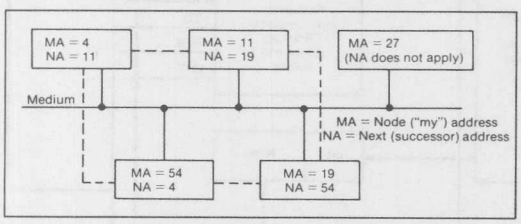


messages that its host has queued. Before transmitting, however, the device checks its internal hold-off register, AHOLT, to determine whether it should defer use of the token on the current cycle. With this optional deference capability, the system designer can bias the intrinsically fair token protocol in favor of selected stations. Those that have more access opportunities have effectively higher priorities.

Key to a token system is the visibility that each station has to network loading conditions. The less often a token is received in a given time, the greater the load on the network. This indication of load data is available to the host as an optional interrupt/token received, and the host can scale down its data over time. Since the host knows the importance of data it sends, it can defer (or set higher delay values in the priority registers) data transmissions of lesser importance to a later time.



3. The chaining technique allows either the host processor or the controller chip to vary the number of buffers in a system. In chaining, buffers are linked so that data frames may span multiple buffers, making memory operations more efficient and simplifies the host's memory allocation tasks.



4. In a logical ring, a token can pass from station 4 (MA-4) to 11, to 19, to 54, and back to 4. The physical order of the ring is irrelevant, since token passing is based only on station addresses.

If transmission proceeds, messages are sent automatically to their appropriate destination addresses, with acknowledgment requests optionally encoded into each frame's header. Such transmissions continue for each frame queued until either a preprogrammed limit or the end of a transmission chain is reached (preprogramming is an optional priority feature). When transmission is complete, the controller passes the token to the next station. After frames having an acknowledge option are transmitted, the transmitting controller awaits a response from the intended receiver. Responses can be positive (indicating that the frame was received correctly), negative, or nonexistent. In the last situation, the receiving station either received the frame incorrectly or was out of service. The waiting period is controlled by an interval timer. If a time out occurs from a no-response condition, the WD2840 automatically retries the transmission.

Automatic retransmissions overcome most network noise glitches quickly and automatically. In this case, the host makes no decisions. If the retry is unsuccessful, the frame is tagged and an interrupt is generated that allows the host to decide the disposition of the frame. To avoid holding up the network, the tagged frame is passed over in the transmission chain and the next frame's transmission is attempted.

A universal device

The WD2840 interfaces with any conventional, general-purpose microprocessor or minicomputer bus. Equally as important as that capability are the chip's contributions to host-speed independence (decoupling) and system efficiency. To achieve these goals, the device combines I/O register programming, interrupts, and dual DMA interfaces for data, exception reporting, and extended control (see "A Three-Controller Architecture").

The memory interface is a self-contained subsystem that consists of two sets of 16-bit registers, byte counters, and DMA control logic. Backing this up is internal intelligence that interprets and manipulates the high-level buffer control structures.

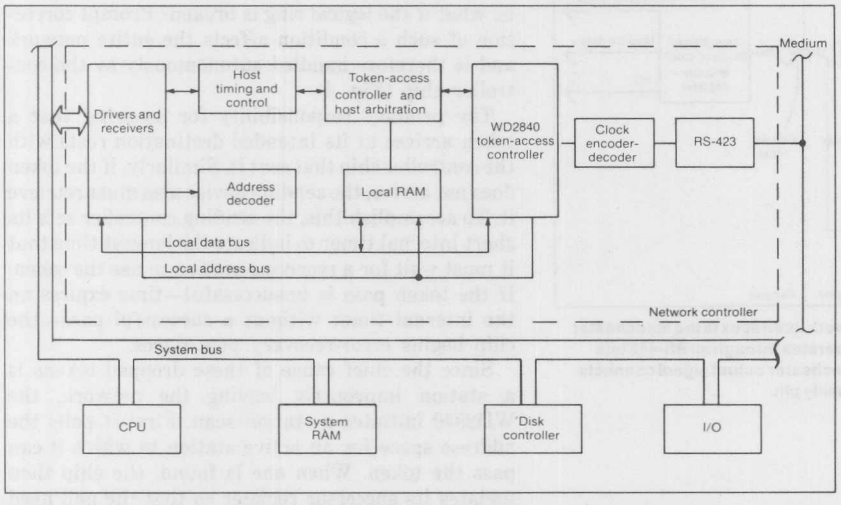
Fetching and storing user data destined for or received from the network are the most important functions of the DMA system. However, these are not simple tasks because of the speed decoupling

needed between the real-time controller and the non-real-time host processes. The WD2840 solves the problem using an open-ended FIFO (first-in, first-out) method of buffer chaining (Fig. 3). In chaining, either the controller or host adds or removes buffers as they consume or generate data, but neither need be concerned about the state of the other.

Though residents of the host's buffer memory, chains are visible to the token-access chip. They are constructed by the host from linked buffers prior to the controller's initialization. Linking the buffers maximizes use of the memory by permitting frames to span multiple buffers, an advantage when most frames are short but long frames must occasionally be accommodated. When receiving a frame, the chip fills the receiving buffer pointed to by an internal register until the frame is complete. If the buffer is filled and the frame is not complete, the device automatically reads the link field of the filled buffer to find the next one available and continues receiving. Of particular importance when interfacing with an existing operating system, this automatic link handling of variable-sized buffers simplifies the host's task of allocating memory.

The transmitting and receiving chains' linked buffers are maintained cooperatively through the use of control fields located in the first buffer of each frame. This header information includes frame status, destination address, and actual frame length in bytes. The length, which determines how many buffers the associated frame spans, is written by the host in the transmitting chain. Each device has its own status bytes and can only read the status of the other device, thus preventing deadlocks.

The control field written by the host is called the frame-control byte and determines what options to put into a frame. An example of a per-frame option is the wait-for-acknowledgment command bit. This bit is tested while the frame is transmitted; if set, it causes the controller to await a response after a frame transmission is complete. The control byte written by the controller is called the frame-status byte. It indicates receiving or transmitting status, including the received "negative acknowledgment,"



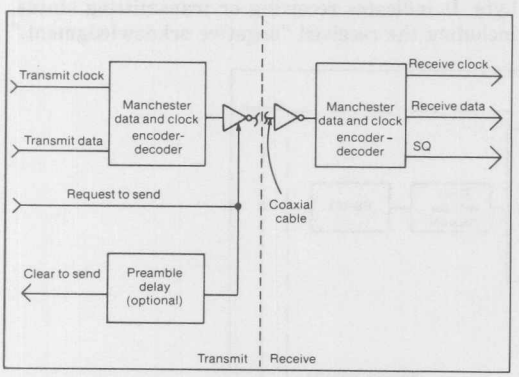
5. A high-performance word-processing application needs a two-ported memory interface between the token-access controller and the local network. This minimizes memory access latency time when the disk controller "hogs" the DMA bus for several consecutive cycles.

if any has been received.

Also contained in the logical memory interface is a series of 8-bit event counters. Located in the host's visible memory in the last section of the WD2840's control block (Fig. 3), they tabulate all noncritical but important network conditions. One such condition is the detection of a transmission error; by the time the host learns of the error, the controller has retransmitted. However, the chip increments the appropriate counter, since the event is valuable to the host for diagnostic purposes.

There are 16 control registers visible to the host (see table). The register file stores initial timer values and such fixed station parameters as station addresses and transmission limits. Included is a pointer to the initial DMA control block, which is used both when initializing the controller and when network exceptions are encountered. The register file also contains locations not visible to the host that are used by the internal controller for scratchpad functions, including the 16-bit pointers to the active receiving and transmitting buffers.

The controller's network (serial) interface accommodates standard modems and clock encoders. The device accepts non-return-to-zero (NRZ) data and permits the transmitting and receiving clocks to be stopped immediately upon completion of a frame if desired. Ordinarily this type of operation is not allowed, as most conventional devices use the clocks to clear the internal shift registers and perform other functions. A pair of request-to-send and clear-to-send signals is available for externally generating preambles for any type of medium.



6. One of the simplest network interfaces is the Manchester encoder-decoder, which operates through an RS-442 bus transceiver. A nonvalid Manchester output signal connects to the controller's signal-quality pin.

Locating errors

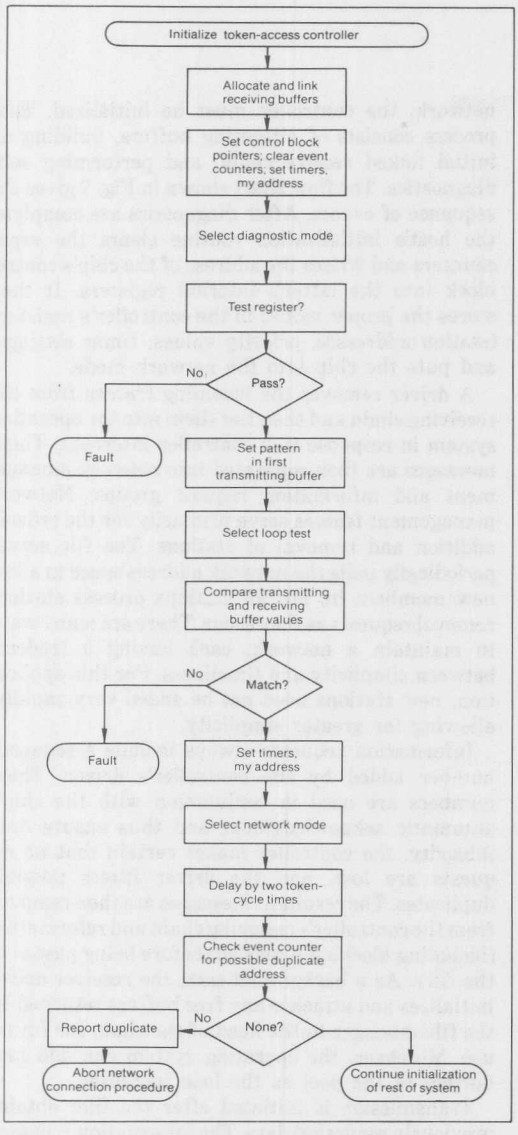
Furnishing the network interface with novel features, the signal-quality input warns the controller that the frame in progress contains an error due to a media, modem, or clock-recovery fault. An example of such a error is the detection of a missed clock transition by a Manchester decoder (see "Manchester II Transfers Data with Integrity, Speed," ELECTRONIC DESIGN, March 19, 1981, p. 233). Coupled with appropriate external logic (optional), this input enhances data integrity beyond that offered by the frame-check sequence included with each transmission.

A common problem in token systems involves the actions necessary if a station is removed or fails; that is, what if the logical ring is broken? Prompt correction of such a condition affects the entire network and is therefore handled autonomously by the controller chip (Fig. 4).

The primary responsibility for assuring that a token arrives at its intended destination rests with the controller chip that sent it. Similarly, if the token does not arrive, the sending device also must retrieve it. To accomplish this, the sending controller sets its short internal timer to indicate the longest time that it must wait for a receiving station to use the token. If the token pass is unsuccessful—time expires on the internal timer without a successful pass—the chip begins error-recovery procedures.

Since the chief cause of these dropped tokens is a station improperly leaving the network, the WD2840 initiates a station scan. First it polls the address space for an active station to which it can pass the token. When one is found, the chip then updates its successor register so that the poll need not be repeated on the next cycle. After the logical ring is restored, the host is informed by means of a new-successor interrupt.

The WD2840 incorporates several types of diagnostics that are necessary in conventional intelligent subsystems and LSI systems. Network-level tests provide confidence and maintainability for the distributed token-access system and its associated medium and modems. System tests validate local interfaces, such as external RAM and the interrupt



7. Initializing the token-access controller is necessary before a host processor can access a local network. The procedure includes buffer allocation, building a linked receiving chain, and performing diagnostic testing.

subsystem, and internal tests validate the chip itself, including the internal controllers and register file. All three diagnostics are used cooperatively.

As a new station powers up—or attaches itself to the network for any reason—it tests itself before transmitting on the network, thus ensuring that any faults do not disrupt the operating network. Self-testing is initiated by the host, which interprets the results. The host must be involved because an LSI device cannot always find and report its own failure.

Network testing occurs continuously. For example, a token-access controller watches for frames transmitted on the network by another station having the chip's own address as its destination. Source stations having the same address are prohibited from a token network. If that occurs, there is usually a hardware failure in the station or a misconfiguration (setting DIP switches incorrectly).

Local networks in word processing

A common application of a distributed network is multiple-user word processing. A typical system consists of a combined file server and print station connected to several remote CRT terminals. Each node contains its own processor and controller, and all communicate via the network. The CRTs are essentially "dumb" terminals having hardware modifications and internal firmware extensions that permit network use. The most critical station is the file server.

CRT terminals can be added or removed from the network while it operates. Either the control chip in each station or the host software configures the network. The choice depends on the speed with which new stations must be admitted and the tolerance of the network to access delays. This application tolerates delays of about 100 ms, so a simple token-access–control polling method is used.

The file server has a two-ported memory interface that minimizes memory access latency resulting from the disk interface's so-called hogging mode. Controllers that retain the DMA bus for several consecutive cycles are in the hogging mode. The two-ported memory is physically located on the network interface module and appears logically in the host processor's address space (Fig. 5).

The host interface matches the timing of the normal microcomputer bus to that of the controller and its local memory. This includes the memory-mapping logic of the host's operating system. Arbitration logic controls access to the local RAM and ensures that simultaneous memory requests by the host and controller do not end in improper memory operations or timing deadlocks. The logic is designed for FIFO-type command priority, with ties awarded to the controller.

The media interface here is implemented in its simplest form: a Manchester encoder-decoder chip and an RS-449 (three-state) bus transceiver (Fig. 6). That device handles its own preamble generation and detection at the start of each frame, so that the clear-to-send pin of the controller is tied directly to its request-to-send pin. Even more, the Manchester part provides a nonvalid Manchester output that is tied to the controller's signal-quality input.

Simple modems of this type are suitable for operation over moderate distances—about 1 km at a 1-Mbit/s transmission rate using twisted-pair cable. Other commercially available modems use more elaborate techniques to increase message reliability and distance or for other types of media.

The software interface with the host's file manager has three phases: initialization, file transmission, and command reception. The controller's initialization and network maintenance routines are included in the operating system. The software receives incoming frames from the WD2840, checks for proper frame sequencing, and builds messages that are compatible with normal operating-system file requests.

Before the operating system can access the network, the controller must be initialized. That process consists of allocating buffers, building an initial linked receive chain, and performing self-diagnostics. The flow chart shown in Fig. 7 gives the sequence of events. After diagnostics are complete, the host's initialization routine clears the event counters and writes the address of the chip's control block into the latter's internal registers. It then stores the proper values in the controller's registers (station addresses, priority values, timer settings) and puts the chip into the network mode.

A driver removes the incoming frames from the receiving chain and then ties them into the operating system in response to a controller interrupt. These messages are then separated into network management and information request groups. Network management frames serve primarily for the orderly addition and removal of stations. The file server periodically polls the network address space to allow new members in, but all stations process station-removal requests as they occur. There are many ways to maintain a network, each having a tradeoff between simplicity and timeliness. For this application, new stations need not be added very rapidly, allowing for greater simplicity.

Information requests always include a sequence number added by the controller's driver. These numbers are used in conjunction with the chip's automatic acknowledgment and thus ensure data integrity: the controller makes certain that no requests are lost, and the driver filters possible duplicates. The resultant messages are then removed from the controller's receiving chain and reformatted (including blocking if needed) before being passed to the filer. As a background task, the receiver driver initializes and attaches any free buffers returned by the file manager to the head of the chain for future use. Moreover, the operating system can add new buffers to the pool as the load increases.

Transmission is initiated after the filer obtains previously requested data. The information is passed to the network data, which then formats it into controller-compatible buffers, adds the correct sequence number and destination address, and finally attaches it to the transmitting chain. As its background task, the transmitting driver periodically checks the chain for buffers that can be returned to the transmission pool. This is an option that can be performed whenever a frame-transmission interrupt occurs. □

A summary of register files

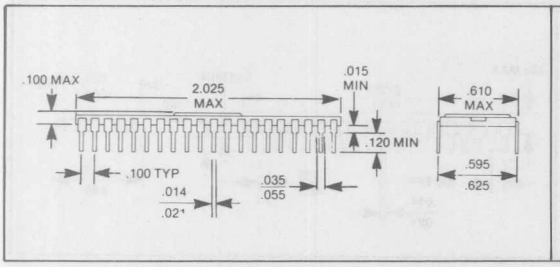
Register	Name	Function
0	CR0	Control register 0
1	CR1	Control register 1
2	SR0	Status register 0
3	IR0	Interrupt register
4	SR1	Status register 1
5	SR2	Status register 2
6	CTR0	Temp counter
7	NA	Next address
8	TA	Acknowledge timer
9	TD	Network dead timer
A	CPBH	Control block pointer (most significant byte)
B	CPBL	Control block pointer (least significant byte)
C	NAR	Next address, request
D	AHOLT	Access hold-off limit
E	TXLT	Transmit limit
F	MA	My address

ORDERING INFORMATION

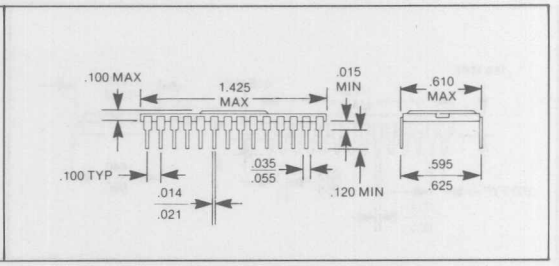
The following listing indicates the available packages for each product. The letter designation refers to the package diagrams, beginning on page 431.

Product	Plastic	Ceramic	CER-DIP
TR1402-00	P	A	
TR1602-00, 01	P	A	
PR1472-00, 01	PL	A	
PT1482-00, 01	PL	A	
FR1502-10, 11	PH	E	
WD1510-00, 01, 02, 03	PH	E	
WD1511	PE	E	
UC1671-00	PL	A	
TR1863-00, 02, 04	P	A	CL
TR1865-00, 02, 04	P	A	CL
WD1931-00	PL	A	
WD1933-00	P	A	CL
WD1933-01	P	A	CL
WD1933-02	P	A	CL
WD1933-03	P	A	CL
WD1933-10	P	A	CL
WD1933-11	P	A	CL
WD1933-12	P	A	CL
WD1933-13	P	A	CL
WD1935-10, 11, 12, 13	P	A	CL
WD1943-00	M	A	CD
WD1943-02	M	A	CD
WD1943-03	M	A	CD
WD1943-04	M	A	CD
WD1943-05	M	A	CD
WD1943-06	M	A	CD
WD1945-00	M	A	CD
WD1945-02	M	A	CD
WD1945-03	M	A	CD
WD1945-04	M	A	CD
WD1945-05	M	A	CD
WD1945-06	M	A	CD
WD1983-01	PH	E	
WD1993-01, 02, 03	PH	E	
WD2001-05, 20, 30	PH	E	
WD2002-05, 20, 30	PH	E	
WD2123-00	P	A	CL
WD2412	PH	AH	
WD8250-00, 20	P	A	CL
WD8275-00, 02	PL	AL	CL
WD8276-00, 02	PL	AL	CL
WD9914-00	PL	AL	CL
WD9918/28/29	PL	AL	CL

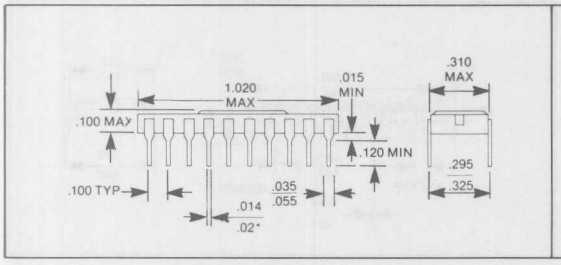
Package Diagrams



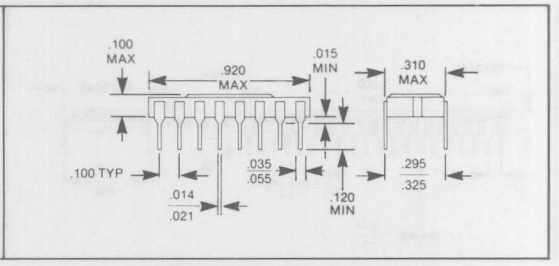
40 LEAD CERAMIC "A" or "AL"



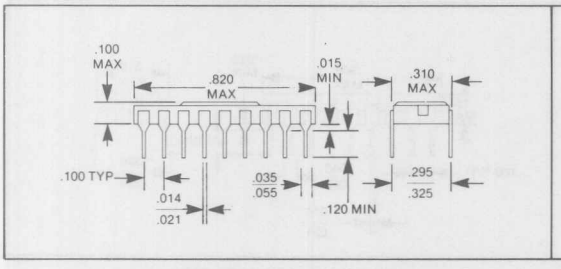
28 LEAD CERAMIC "E" or "AH"



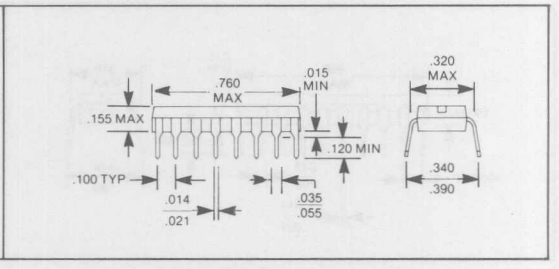
20 LEAD CERAMIC "U" or "AE"



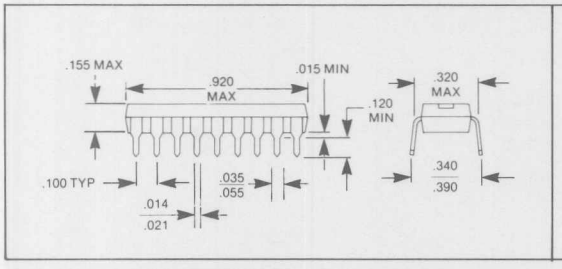
18 LEAD CERAMIC "L" or "AD"



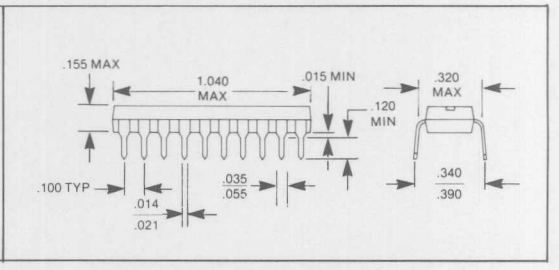
16 LEAD CERAMIC "J" or "AC"



16 LEAD PLASTIC "K" or "PC"

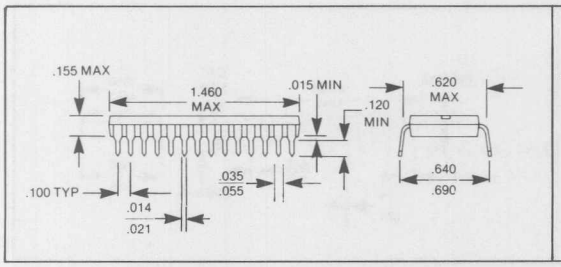


18 LEAD PLASTIC "M" or "PD"

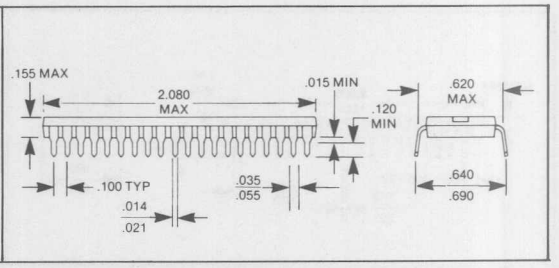


20 LEAD PLASTIC 'V' or "PE"

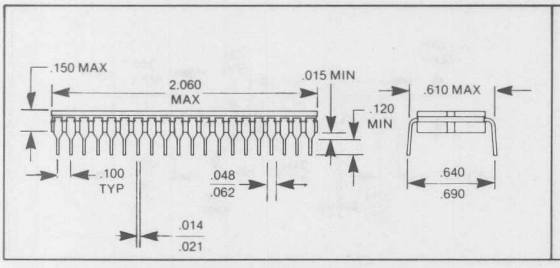
Package Diagrams



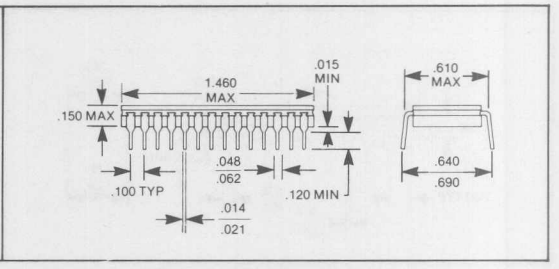
28 LEAD PLASTIC "R" or "PH"



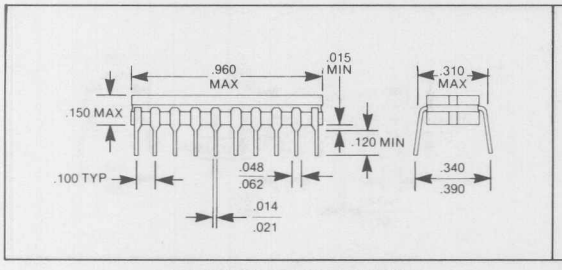
40 LEAD PLASTIC "P" or "PL"



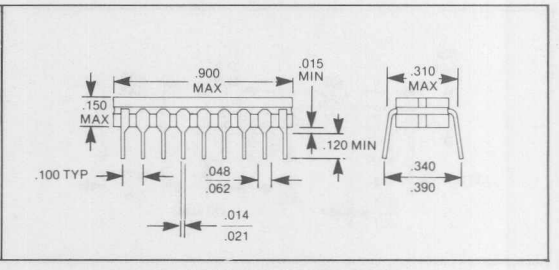
40 LEAD CERDIP "CL"



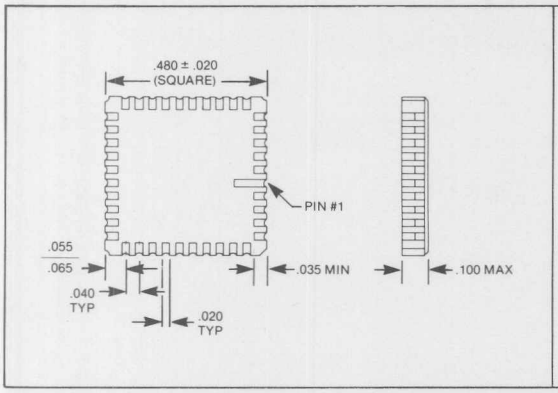
28 LEAD CERDIP "CH"



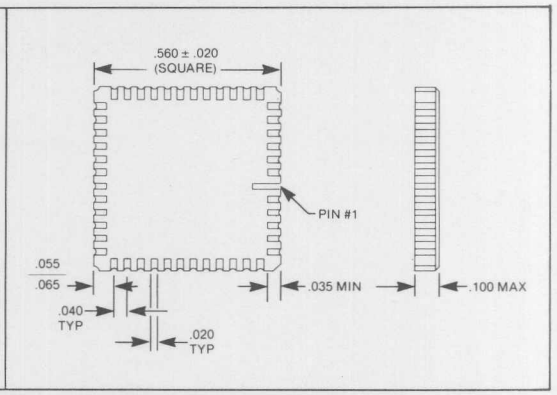
20 LEAD CERDIP "CE"



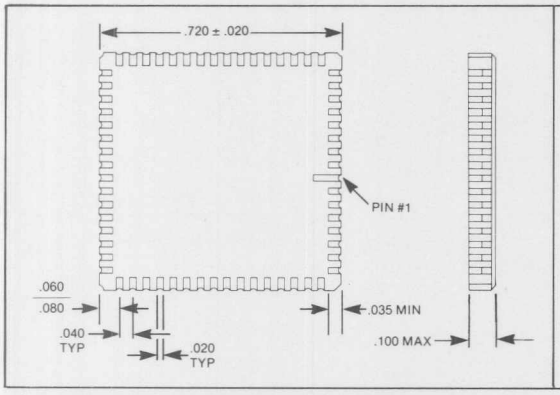
18 LEAD CERDIP "CD"



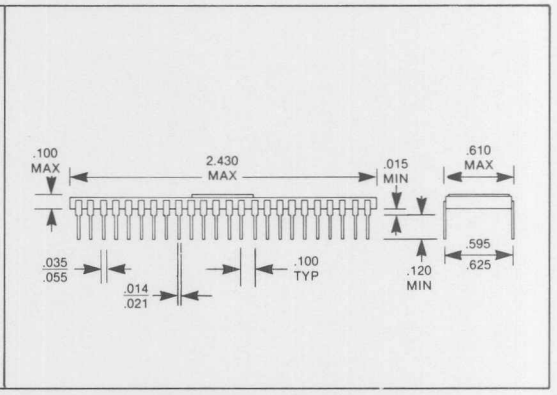
40 LEAD CERAMIC CHIP CARRIER "DL"



48 LEAD CERAMIC CHIP CARRIER "DN"



64 LEAD CERAMIC CHIP CARRIER "DS"



48 LEAD CERAMIC "T" or "AN"

Pin Compatibility Guide

	AMI	GI	HARRIS	INTEL	INTERSIL	NATIONAL	NITRON	SMC	TI
TR1402[5]	S1757 S1883	AY-6-1013						COM2502 COM2502H	$TMS6010_4$
TR1602	S1602	AY-5-1013A				MM5303		COM2017 COM2017H	$TMS6011_4$
TR1863[7]		AY-3-1014A	HD6402		IM64025			COM8052 COM8017	
TR1865[6]		AY-3-1015D						COM8018	
PR1472		AY3-1472B[4]					NC2259		
PT1482		AY-3-1482B[4]					NC2257 NC2260		
UC1671						INS1671		COM1671	
WD8250						INS8250			
WD1983[1]				8251A[1]		INS8251A[1]			
WD1943								COM5016/ 5016T COM8116/ 8116T	
WD1945								COM5036/ 5036T COM8136/ 8136T	
WD4200						COPS420			
WD4210						COPS421			
WD4320						COPS320			
WD4321						COPS321			
WD8275									
WD8276									
WD9914									TMS9914A
WD9918/ 28/29									TMS9918A /28A/29A

NOTES:
1. WD1983 is ASYNC only; INS8251A and 8251A is ASYNC and BISYNC
2. Many frequency selections available. Consult factory for details
3. Pin 10 on BR1941 is a "No Connection"
4. Discontinued product
5. TR1402 is compatible with Signetics 2536
6. TR1865 is compatible with Fujitsu WB8868A and Hughes HCMP1854
7. TR1863 is compatible with RCA CDP1854

Component Products
Terms and Conditions

1. **ACCEPTANCE:** Unless otherwise provided, it is agreed that sales are made on the terms, conditions and warranties contained herein and that to the extent of any conflict, the same take precedence over any terms or conditions which may appear on Buyer's order form. Seller shall not be bound by Buyer's terms and conditions unless expressly agreed to in writing. In the absence of written acceptance of these terms, acceptance of or payment for any of the articles covered hereby shall constitute an acceptance of these terms and conditions.

2. **F.O.B. POINT:** All sales are made F.O.B. point of shipment. Seller's title passes to Buyer and Seller's liability as to delivery ceases upon making delivery of articles purchased hereunder to carrier at shipping point in good condition; the carrier acting as Buyer's agent. All claims for damages must be filed with the carrier. Unless specific instructions from Buyer specify which method of shipment is to be used, the Seller will exercise his own discretion.

3. **DELIVERY:** Shipping dates are approximate only. Seller shall not be liable for any loss or expense (consequential or otherwise) incurred by Buyer if Seller fails to meet the specified delivery schedule because of unavoidable production or other delays. Seller may deliver the articles in installments, Seller shall not be liable for any delay in delivery or for non-delivery, in whole or in part, caused by the occurrence of any contingency beyond the control either of Seller or Seller's suppliers, including, by way of illustration but not limitation, war (whether an actual declaration thereof is made or not), sabotage, insurrection, riot or other act of civil disobedience, act of a public enemy, failure or delay in transportation, act of any government or any agency or subdivision thereof, judicial action, labor dispute, accident, fire, explosion, flood, storm or other act of God, shortage of labor, fuel, raw material or machinery or technical failure where Seller has exercised ordinary care in the prevention thereof. If any contingency occurs, Seller may allocate production and deliveries among Seller's customers.

4. **TERMS AND METHODS OF PAYMENT:** Where seller has extended credit to Buyer, terms of payment shall be net thirty (30) days from date of invoice. The amount of credit or terms of payment may be changed or credit withdrawn by Seller at any time. If the articles are delivered in installments, Buyer shall pay for each installment in accordance with the terms hereof. Payment shall be made for the articles without regard to whether Buyer has made or may make any inspection of the articles. If shipments are delayed by Buyer, payments are due from the date when Seller is prepared to make shipments. Articles held for Buyer are at Buyer's sole risk and expense.

5. **TAXES:** All prices are exclusive of all federal, state and local excise, sales, use, and similar taxes. Such taxes; when applicable to this sale or to the articles sold, will appear as separate additional items on the invoice unless Seller receives a properly executed exemption certificate from Buyer prior to shipment.

6. **PATENTS:** The Buyer shall hold the Seller harmless against any expense or loss resulting from infringement of patents or trademarks arising from compliance with Buyer's designs or specifications or instructions. The sale of products by the Seller does not convey any license, by implication, estoppel, or otherwise, under patent claims covering combinations of said products with other devices or elements. Except as otherwise provided in the preceding paragraph, the Seller shall defend any suit or proceeding brought against the Buyer so far as based on a claim that any product, or any part thereof, furnished under this contract constitutes an infringement of any patent of the United States, if notified promptly in writing and given authority, information and assistance (at the Seller's expense) for the defense of same, and the Seller shall pay all damages and costs awarded therein against the Buyer. In case said product, or any part thereof, is in such suit held to constitute infringement and the use of said product or part is enjoined, the Seller, shall at its own expense, either procure for the Buyer the right to continue using said product or part, or replace same with non-infringing product, or modify it so it becomes non-infringing, or remove said product and refund the purchase price and the transportation and installation costs thereof. The foregoing states the entire liability of the Seller for patent infringement by the said products of any part thereof.

7. **ASSIGNMENT:** The Buyer shall not assign his order or any interest therein or any rights thereunder without the prior written consent of Seller.

8. **WARRANTY:** Seller warrants articles of its manufacture against defective materials or workmanship for a period of one year from date on which Seller delivers said articles. The liability of Seller under this warranty is limited at Seller's option, solely to repair, replacement with equivalent articles, or an appropriate credit adjustment not to exceed the original sales price of articles returned to the Seller provided that (a) Seller is promptly notified in writing by Buyer upon discovery of defects, (b) the defective article is returned to Seller, transportation charges prepaid by Buyer, and (c) Seller's examination of such article disclosed to its satisfaction that defects were not caused by negligence, misuse, improper installation, accident, or unauthorized repair or alteration by the Buyer. In the case of equipment articles, this warranty does not include mechanical parts failing from normal usage nor does it cover limited life electrical components which deteriorate with age. In the case of accessories, not manufactured by Seller, but which are furnished with the Seller's equipment, Seller's liability is limited to whatever warranty is extended by the manufacturers thereof and transferable to the Buyer. This Warranty is expressed in lieu of all other Warranties, expressed or implied, including the implied Warranty of fitness for a particlar purpose, and of all other obligations or liabilities on the Seller's part, and it neither assumes nor authorizes any other person to assume for the Seller any other liabilities. This Warranty should not be confused with or construed to imply free preventative or remedial maintenance, calibration or other service required for normal operation of the equipment articles. These Warranty provisions do not extend the original Warranty period of any article which has either been repaired or replaced by Seller. In no event will Seller be liable for any incidental or consequential damages.

9. **TERMINATION:** Buyer may terminate this contract in whole or from time to time in part upon 60 days written notice to Seller. In such event Buyer shall be liable for termination charges which shall include a price adjustment based on the quantity of articles actually delivered, and all costs, direct and indirect, incurred and committed for this contract together with a reasonable allowance for pro-rated expenses and profits. Any termination or back off in scheduling will not be allowed on shipments scheduled for the month in which the request is made and for the month following.

10. **GOVERNMENT CONTRACTS:** If the articles to be furnished under this contract are to be used in the performance of a Government contract or subcontract and a Government contract number shall appear on Buyer's purchase order, those clauses of the applicable Government procurement regulation which are mandatorily required by Federal Statute to be included in Government subcontracts shall be incorporated herein by reference.

11. **ORIGIN OF ARTICLES:** Seller engages in off-shore production, assembly and/or processing and makes no warranty or representation, expressed or implied, that the articles delivered hereunder are United States articles or of U.S. origin for the purpose of any statute, law, rule, regulation or case thereunder. If Buyer ships the articles hereunder out of the U.S. for assembly, then at Buyer's request in writing, Seller shall provide information applicable to identification of any articles not of U.S. origin.

Corita Kent, the cover artist, is an American whose work presents an optimistic, yet philosophical view of the world we live in. A former Catholic nun and teacher, Corita now devotes her life and energies to her artwork and the "human needs she feels transcend national and religious barriers." A true "citizen of the world," Corita's philosophy positions her "on the positive side of hope." Her depiction of the Western Digital mission . . . "Making the leading edge work for you" . . . dramatizes the spectrum of solutions we provide our customers.

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